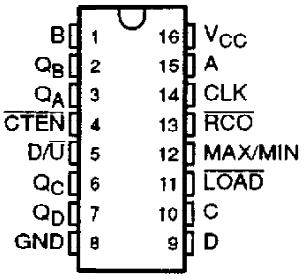
SDFS059

SN54F191A, SN74F191A
SYCHRONOUS 4-BIT UP/DOWN BINARY COUNTERS WITH RESET AND RIPPLE CLOCK

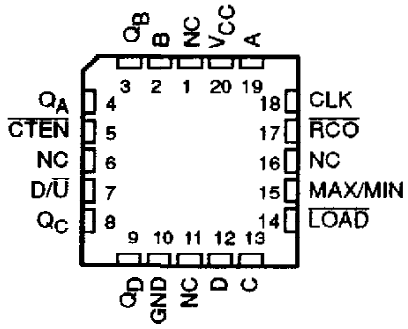
SCF3002 – DXXXX, JANUARY 1991

- **High Speed f_{MAX} of 125 MHz Typical**
- **Single Down/Up Count Control Line**
- **Look-Ahead Circuitry Enhances Speed of Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Asynchronously Presettable with Load Control**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN54F191A . . . J PACKAGE
SN74F191A . . . D OR N PACKAGE
(TOP VIEW)



SN54F191A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'F191A is a synchronous, 4-bit binary reversable up/down counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input ($\overline{CTEN}$) is low.

A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

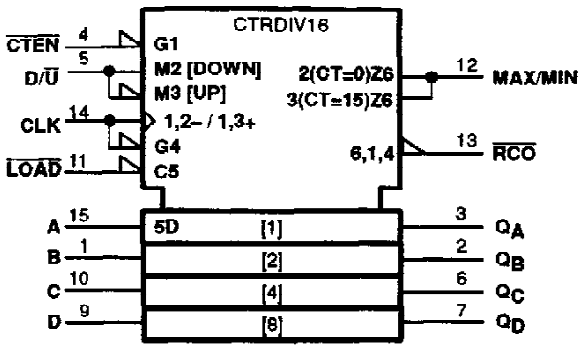
This counter features a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

This counter is fully programmable; that is, they may each be preset to any number by placing a low on the load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independently of the level of the clock input. This feature allows the counter to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9) counting up. The ripple clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions but only while the clock input is low. The counter can easily be cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

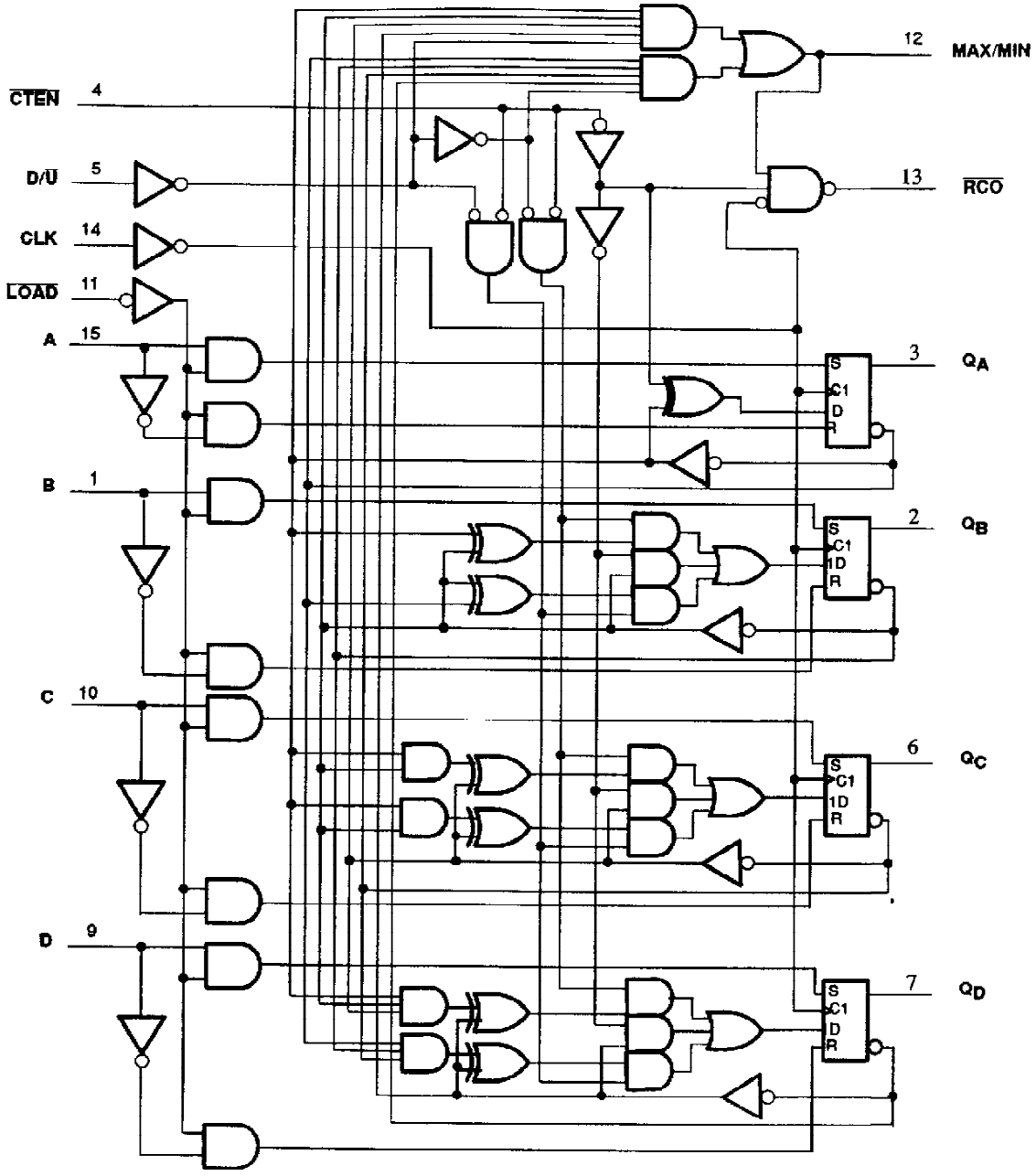
The SN54F191A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F191A is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91–1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)

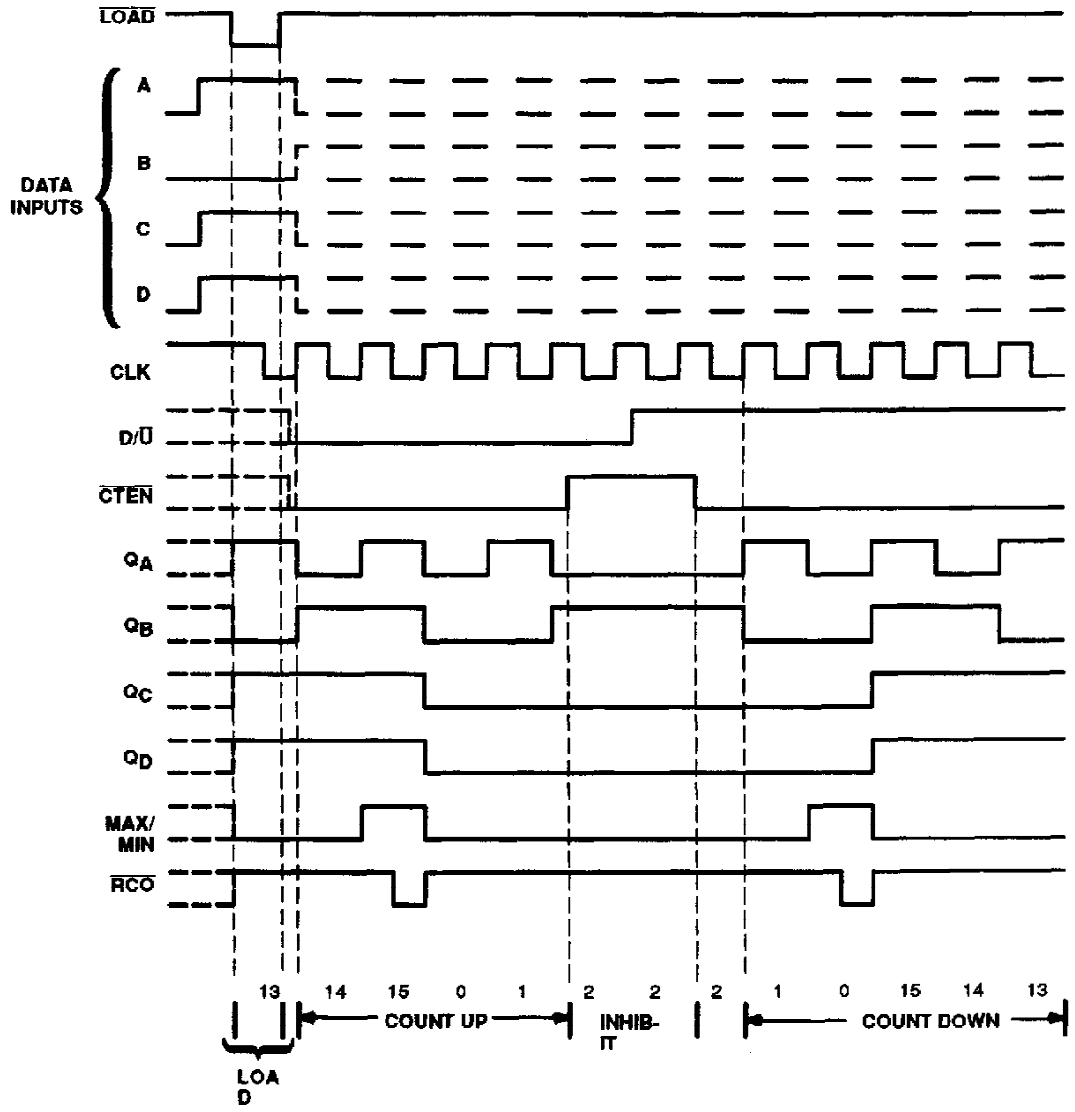


Pin numbers shown are for DW, J, and N packages.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I † . . . . . –1.2 V to 7 V
Input current range, ... – 30 mA to 5 mA
Voltage applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F190 . . . . . –55 °C to 125 °C
SN74F190 . . . . . 0 °C to 70 °C
Store temperature range . . . . . –55°C to 150°C

† The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54F191A			SN74F191A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			18			18	mA
I_{OH}	High-level output current			–1			– 1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54F191A			SN74F191A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –1 mA		2.5	3.4		2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = –1 mA					2.7			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA			0.3	0.5		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V	$\overline{CTEN}$			–1.8			–1.8	mA
			Others			–0.6			–0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_I = 2.25 V		–60		–150	–60		–150	mA
I_{CC}	V_{CC} = 5.5 V,	V_O = 0			40	55		40	55	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than out output should be shorted at a time and duration of the short circuit should not exceed one second.

timing requirements

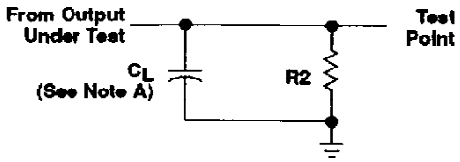
			T_A = 25°C		SN54F191A		SN74F191A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		175		175		175		MHZ
t_w	Pulse duration	$\overline{LOAD}$ low	6		6		6		ns
		CLK high or low	6		6		6		
t_{su}	Setup time	Data before $\overline{LOAD}$↑	4.5		5		5		ns
		$\overline{CTEN}$ before CLK↑	10		10		10		
		D/$\overline{U}$ before CLK↑	12		12		12		
		$\overline{LOAD}$ inactive before CLK↑	8		8		8		
t_h	Hold time	Data after $\overline{LOAD}$↑	2		2		2		ns
		$\overline{CTEN}$ after CLK↑	0		0		0		
		D/$\overline{U}$ after CLK↑	0		0		0		

switching characteristics (see Figure 1)

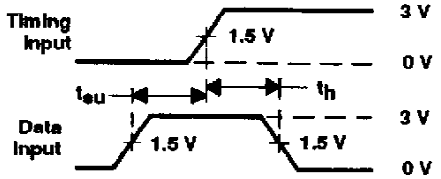
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			'F191A			SN54F191A		SN74F191A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100			100		100		MHz
t_{PLH}	$\overline{LOAD}$	Any Q	3.7	8.5	12	3.7	14	3.7	13	ns
t_{PHL}			4.7	8	11.5	4.7	13	4.7	12	
t_{PLH}	A, B, C, or D	Any Q	1.2	4	7	0.7	8.5	0.7	7.5	ns
t_{PHL}			5.7	9	12	5.7	14	5.7	13	
t_{PLH}	CLK	$\overline{RCO}$	1.7	4.5	7.5	1.7	9	1.7	8	ns
t_{PHL}			2.2	5	7.5	2.2	9	2.2	8	
t_{PLH}	CLK	Any Q	1.7	4.5	8	1.7	9.5	1.2	8.5	ns
t_{PHL}			5.2	7.5	11.5	4.2	13	4.2	12	
t_{PLH}	CLK	MAX/MIN	5.7	9	12.1	5.7	14	5.7	13	ns
t_{PHL}			4.2	8	11	4.2	13	4.2	12	
t_{PLH}	D/$\overline{U}$	$\overline{RCO}$	7.2	11	16	7.2	18	7.2	17	ns
t_{PHL}			3.7	7.5	10.5	3.2	12	3.2	11	
t_{PLH}	D/$\overline{U}$	MAX/MIN	3.2	6.6	9.5	2.2	11.5	2.2	10.5	ns
t_{PHL}			2.2	6	9.5	2.2	11	2.2	10	
t_{PLH}	$\overline{CTEN}$	RCO	1.2	4	7	1.2	8.5	1.2	7.5	ns
t_{PHL}			2.2	5	7.5	2.2	9	2.2	8	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

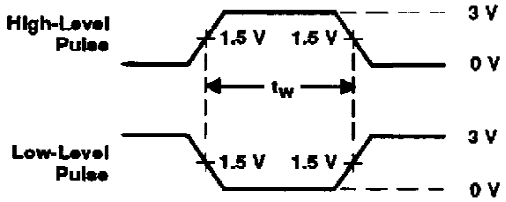
PARAMETER MEASUREMENT INFORMATION



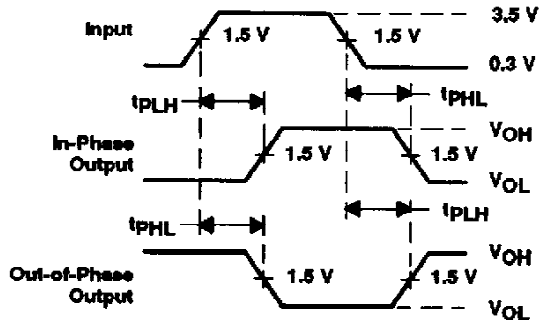
LOAD CIRCUIT



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses have the following characteristics: PRR = 1 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50 %.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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