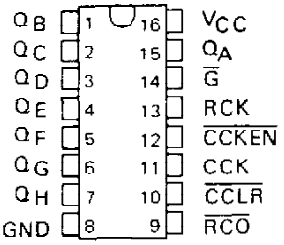
SN54LS590, SN54LS591, SN74LS590, SN74LS591
8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

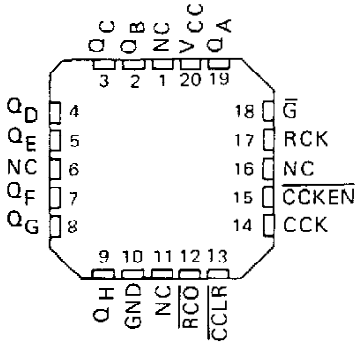
SDLS003 D2632, JANUARY 1981 – REVISED MARCH 1988

- 8-Bit Counter with Register
- Parallel Register Outputs
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency: DC to 20 MHz

SN54LS590, SN54LS591 . . . J OR W PACKAGE
SN74LS590, SN74LS591 . . . N PACKAGE
(TOP VIEW)



SN54LS590, SN54LS591 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

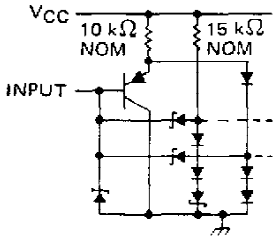
description

These devices each contain an 8-bit binary counter that feeds an 8 bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading, a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

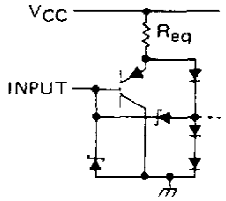
Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

schematics of inputs and outputs

EQUIVALENT OF CCK INPUT

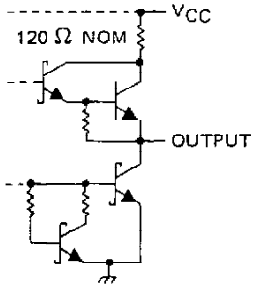


EQUIVALENT OF ALL OTHER INPUTS

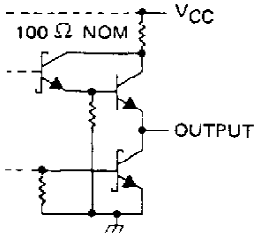


RCK: R_{eq} = 10 kΩ NOM
ALL OTHER: R_{eq} = 13 kΩ NOM

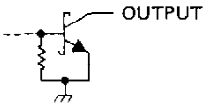
$\overline{RCO}$ OUTPUT



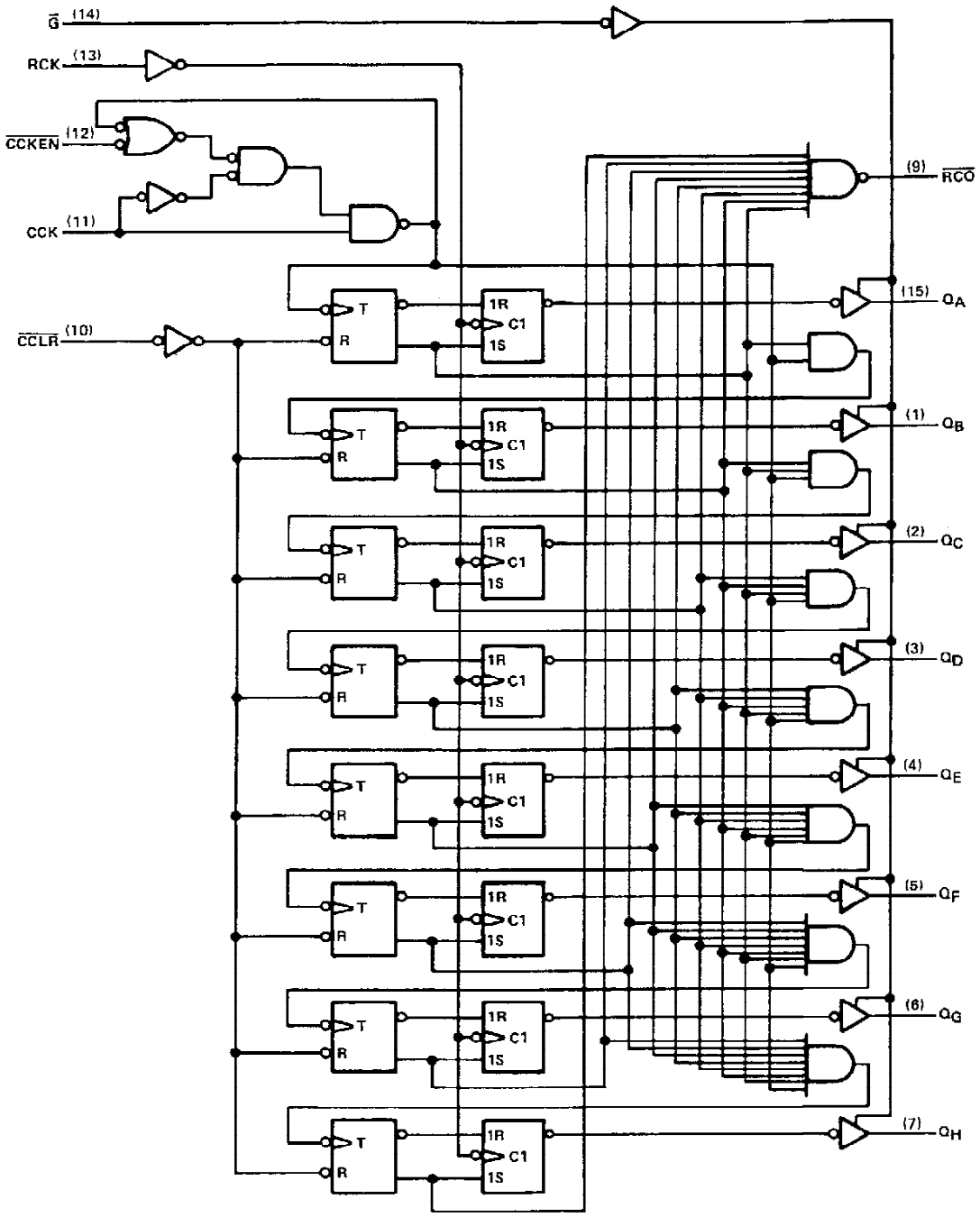
TYPICAL OF Q OUTPUTS ('LS590)



TYPICAL OF Q OUTPUTS ('LS591)

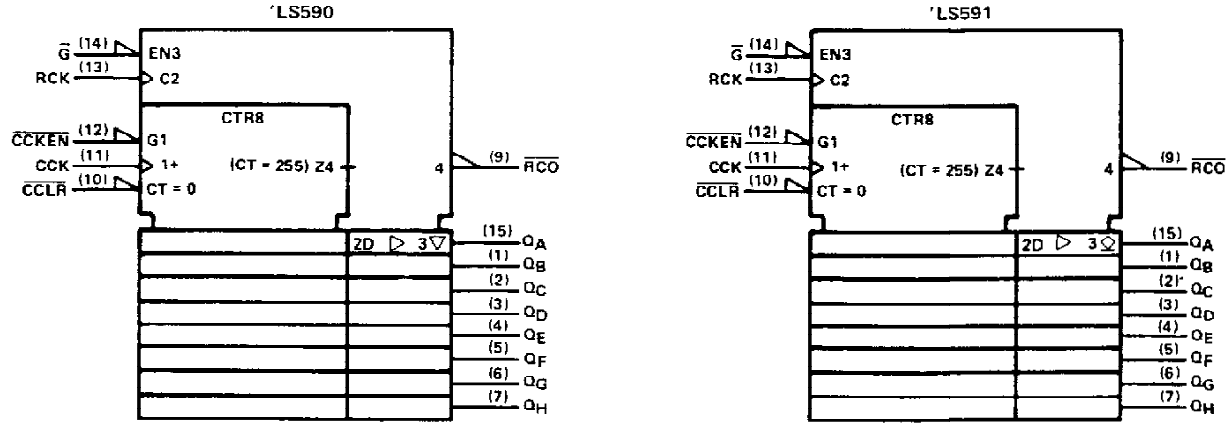


logic diagram (positive logic)



Pin numbers shown are for J, N and W packages.

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591 . . . . . −55°C to 125°C
SN74LS590, SN74LS591 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{OH}	High-level output voltage	Q, 'LS591 only			5.5			5.5	V
I_{OH}	High-level output current	$\overline{RCO}$			−1			−1	mA
		Q, 'LS590 only			−1			−2.6	
I_{OL}	Low-level output current	$\overline{RCO}$			8			16	mA
		Q			12			24	
f_{CCK}	Counter clock frequency		0		20	0		20	MHz
f_{RCK}	Register clock frequency		0		25	0		25	MHz
$t_{w(CCK)}$	Duration of counter clock pulse		25			25			ns
$t_{w(\overline{CCLR})}$	Duration of counter clear pulse		20			20			ns
$t_{w(RCK)}$	Duration of register clock pulse		20			20			ns
t_{su}	Setup time	$\overline{CCKEN}$ low before CCK↑	20			20			ns
		$\overline{CCLR}$ inactive before CCK↑	20			20			
		CCK before RCK↑ (see Note 2)	40			40			
t_h	Hold time	$\overline{CCKEN}$ low after CCK↑	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	'LS590 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		I_{OH} = −1 mA	2.4	3.2					V
				I_{OH} = −2.6 mA				2.4	3.1		
	$\overline{RCO}$			I_{OH} = −1 mA	2.4	3.2		2.4	3.2		
I_{OH}	'LS591 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
	$\overline{RCO}$			I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	'LS590 Q	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V		V_{IL} = MAX,			20			20	μA
I_{OZL}	'LS590 Q	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V		V_{IL} = MAX,			−20			−20	μA
I_I		V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	CCK	V_{CC} = MAX, V_I = 0.4 V					−0.8			−0.8	mA
	All others						−0.2			−0.2	
I_{OS}§	'LS590 Q	V_{CC} = MAX, V_O = 0 V			−30		−130	−30		−130	mA
	$\overline{RCO}$				−20		−100	−20		−100	
I_{CC}	'LS590	I_{CCH}	V_{CC} = MAX, All possible inputs grounded, All outputs open			33	55		33	55	mA
		I_{CCL}				44	65		44	65	
		I_{CCZ}				46	65		46	65	
	'LS591	I_{CCH}				35	55		35	55	
		I_{CCL}				42	65		42	65	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS590			'LS591			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	RCK	Q	R_L = 667 Ω,	C_L = 45 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 1 kΩ,	C_L = 30 pF		14	22		16	24	ns
t_{PHL}	CCK↑	$\overline{RCO}$				20	30		25	38	ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$				30	45		32	48	ns
t_{PLH}	RCK↑	Q	R_L = 667 Ω,	C_L = 45 pF		12	18		25	38	ns
t_{PHL}	RCK↑	Q				22	33		28	42	ns
t_{PZH}	$\overline{G}$↓	Q				25	38				ns
t_{PZL}	$\overline{G}$↓	Q				30	45				ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω,	C_L = 5 pF		20	30				ns
t_{PLZ}	$\overline{G}$↑	Q				25	38				ns
t_{PLH}	$\overline{G}$↑	Q	R_L = 667 Ω,	C_L = 45 pF					34	50	ns
t_{PHL}	$\overline{G}$↓	Q							32	48	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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