

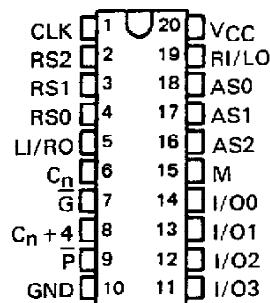
# SN54LS681, SN74LS681 4-BIT PARALLEL BINARY ACCUMULATORS

SDLS197

D2422, JANUARY 1981 — REVISED MARCH 1988

- Full 4-Bit Binary Accumulator in a Single 20-Pin Package
- Contains Two Synchronous Registers:  
Word A  
Word B Shift/Accumulator
- 16 Arithmetic Operations Including  
B Minus A and A Minus B
- 16 Logic-Mode Operations
- Expandable to Handle N-Bit Words  
with Full Carry Look-Ahead
- Bus Driving I/O Ports

SN54LS681 . . . J OR W PACKAGE  
SN74LS681 . . . DW OR N PACKAGE  
(TOP VIEW)



## description

These low-power Schottky IC's integrate a high-speed arithmetic logic unit (ALU) complete with word A and word B registers on a single chip. The ALU performs 16 arithmetic and 16 logic functions (see Tables 1 and 2). Full carry look-ahead is provided for fast carry of four-bit words. The carry input ( $C_n$ ) and propagate and generate outputs (P and G) are provided for direct use with SN54S182/SN74S182 carry look-ahead generators for optimum performance with longer words.

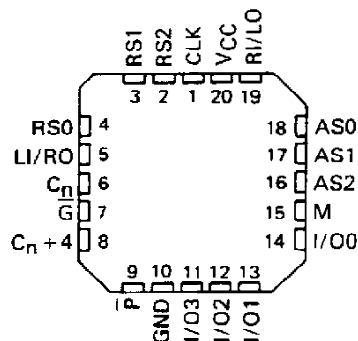
The A and B registers are controlled by three inputs (RS0, RS1, and RS2). These pins define eight distinct register modes (see Table 3). The A register is a simple storage register while the B register is a combination storage/shift/accumulator register. The contents of the A and B registers provide the A and B words for the ALU.

Four I/O ports (I/O 0 thru I/O 3) are provided for parallel loading of word A and/or word B into their respective registers. These same ports also serve as bus driving outputs for the ALU/accumulator results (Fj). Two additional I/O ports (RI/LO and LI/RO) are provided to allow expansion of the accumulator for words greater than four bits in length.

The A or B register can be parallel loaded from the four I/O ports. The B register can also be parallel loaded from the ALU as an accumulator register and in addition, the B register can be serially loaded from either the RI/LO or the LI/RO ports.

The SN54LS681 is characterized for operation over the full military temperature range from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS681 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS681 . . . FK PACKAGE  
(TOP VIEW)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

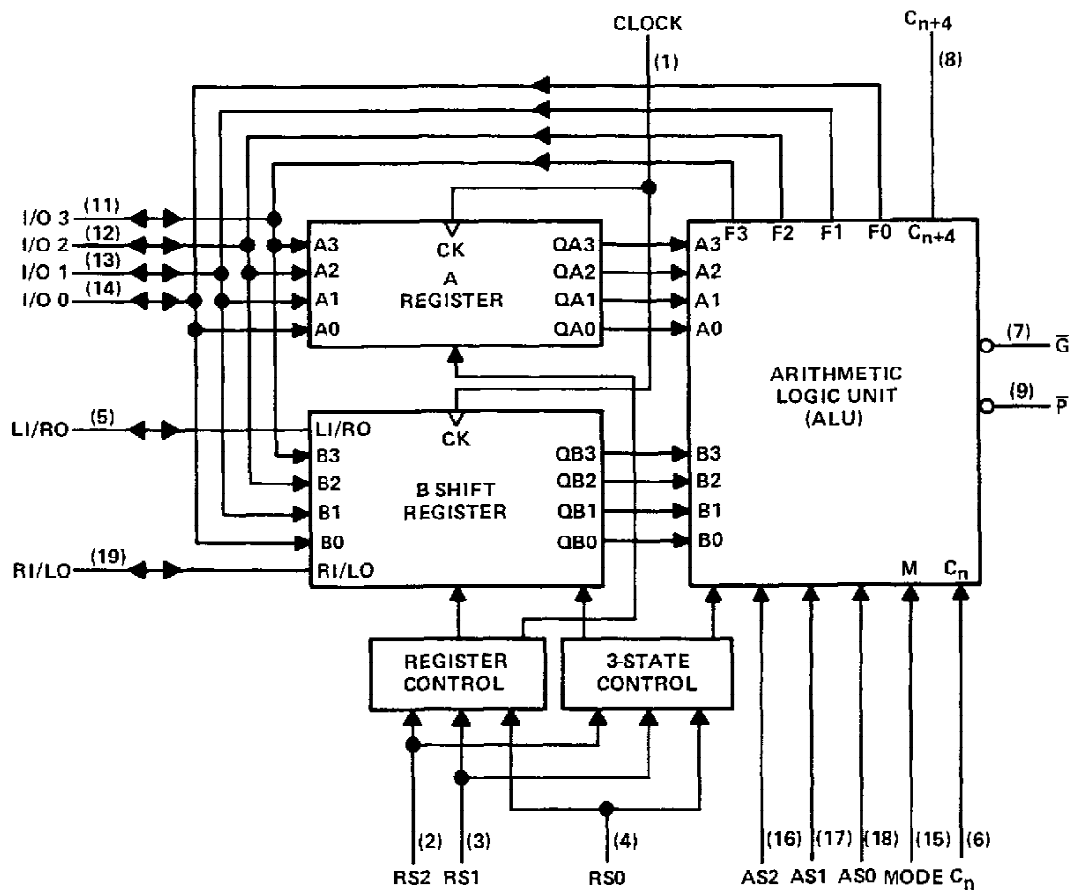
TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

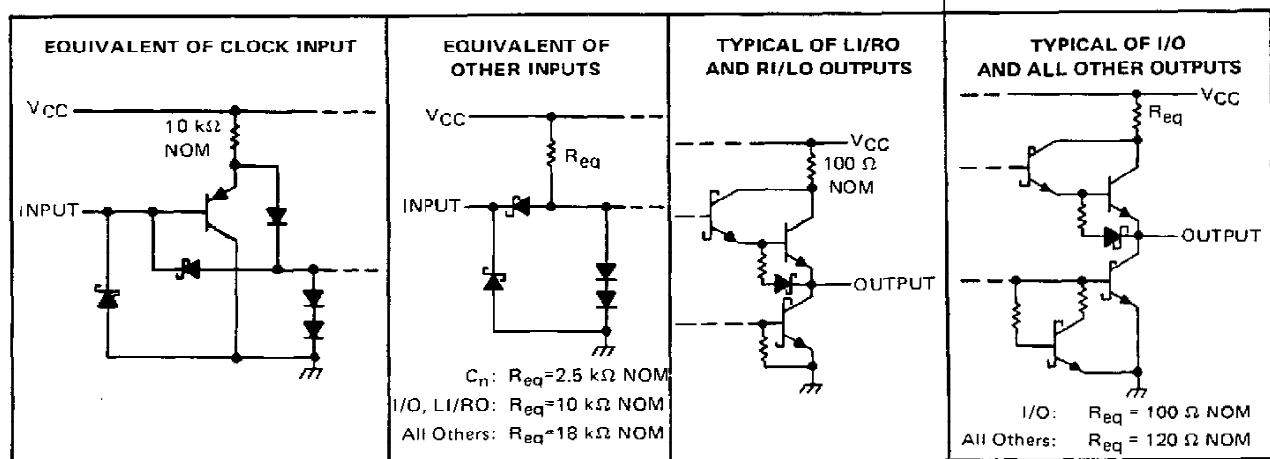
# SN54LS681, SN74LS681

## 4-BIT PARALLEL BINARY ACCUMULATORS

functional block diagram (positive logic)



schematics of inputs and outputs



TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS681, SN74LS681**  
**4-BIT PARALLEL BINARY ACCUMULATORS**

**FUNCTION TABLES**

**TABLE 1 — ARITHMETIC FUNCTIONS**

Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
			$C_n = H$ (with carry)	$C_n = L$ (no carry)
AS2	AS1	AS0		
L	L	L	$F_j = L$	$F_j = H$
L	L	H	$F = B \text{ MINUS } A$	$F = B \text{ MINUS } A \text{ MINUS } 1$
L	H	L	$F = A \text{ MINUS } B$	$F = A \text{ MINUS } B \text{ MINUS } 1$
L	H	H	$F = A \text{ PLUS } B \text{ PLUS } 1$	$F = A \text{ PLUS } B$
H	L	L	$F = B \text{ PLUS } 1$	$F_j = B_j$
H	L	H	$F = \bar{B} \text{ PLUS } 1$	$F_j = \bar{B}_j$
H	H	L	$F = A \text{ PLUS } 1$	$F_j = A_j$
H	H	H	$F = \bar{A} \text{ PLUS } 1$	$F_j = \bar{A}_j$

**TABLE 2 — LOGIC FUNCTIONS**

Mode Control (M) = High

ALU SELECTION			ACTIVE-HIGH DATA	
			$C_n = H$ (with carry)	$C_n = L$ (no carry)
AS2	AS1	AS0		
L	L	L	$F_0 = H, F_1 = F_2 = F_3 = L$	$F_j = L$
L	L	H	$F_j = A_j \oplus B_j \text{ PLUS } 1$	$F_j = A_j \oplus B_j$
L	H	L	$F_j = \bar{A}_j \oplus \bar{B}_j \text{ PLUS } 1$	$F_j = \bar{A}_j \oplus \bar{B}_j$
L	H	H	$F_j = L$	$F_j = H$
H	L	L	$F_j = A_j B_j \text{ PLUS } 1$	$F_j = A_j B_j$
H	L	H	$F_j = \bar{A}_j + \bar{B}_j \text{ PLUS } 1$	$F_j = \bar{A}_j + \bar{B}_j$
H	H	L	$F_j = \bar{A}_j \bar{B}_j \text{ PLUS } 1$	$F_j = \bar{A}_j \bar{B}_j$
H	H	H	$F_j = A_j + B_j \text{ PLUS } 1$	$F_j = A_j + B_j$

**TABLE 3 — REGISTER FUNCTIONS**

FUNCTION	INPUTS BEFORE L TO H CLOCK TRANSITION									INTERNAL OUTPUTS AFTER L TO H CLOCK TRANSITION													
	REGISTER SELECTION			DATA INPUTS						A REGISTER				B SHIFT REGISTER						ALU			
	RS2	RS1	RS0	LI/RO	I/Q 3	I/Q 2	I/Q 1	I/Q 0	RI/LO	QA3	QA2	QA1	QA0	LI/RO	QB3	QB2	QB1	QB0	RI/LO	F3	F2	F1	F0
ACCUM	L	L	L	Z	F3	F2	F1	F0	Z	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	Z	F3 <sub>n</sub>	F2 <sub>n</sub>	F1 <sub>n</sub>	F0 <sub>n</sub>	Z	F3	F2	F1	F0
LOAD B	L	L	H	Z	b3	b2	b1	b0	Z	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	Z	b3	b2	b1	b0	Z	Z	Z	Z	Z
LEFT SHIFT LOGICAL	L	H	L	li	F3	F2	F1	F0	QB0	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	li	li	QB3 <sub>n</sub>	QB2 <sub>n</sub>	QB1 <sub>n</sub>	QB1 <sub>n</sub>	F3	F2	F1	F0
LEFT SHIFT ARITH	L	H	H	li	F3	F2	F1	F0	QB0	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	li	QB3 <sub>n</sub>	li	QB2 <sub>n</sub>	QB1 <sub>n</sub>	QB1 <sub>n</sub>	F3	F2	F1	F0
RIGHT SHIFT LOGICAL	H	L	L	QB3	F3	F2	F1	F0	ri	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	QB2 <sub>n</sub>	QB2 <sub>n</sub>	QB1 <sub>n</sub>	QB0 <sub>n</sub>	ri	ri	F3	F2	F1	F0
RIGHT SHIFT ARITH	H	L	H	QB2	F3	F2	F1	F0	ri	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	QB1 <sub>n</sub>	QB3 <sub>n</sub>	QB1 <sub>n</sub>	QB0 <sub>n</sub>	ri	ri	F3	F2	F1	F0
HOLD	H	H	L	Z	F3	F2	F1	F0	Z	QA3 <sub>0</sub>	QA2 <sub>0</sub>	QA1 <sub>0</sub>	QA0 <sub>0</sub>	Z	QB3 <sub>0</sub>	QB2 <sub>0</sub>	QB1 <sub>0</sub>	QB0 <sub>0</sub>	Z	F3 <sub>0</sub>	F2 <sub>0</sub>	F1 <sub>0</sub>	F0 <sub>0</sub>
LOAD A	H	H	H	Z	a3	a2	a1	a0	Z	a3	a2	a1	a0	Z	QB3 <sub>0</sub>	QB2 <sub>0</sub>	QB1 <sub>0</sub>	QB0 <sub>0</sub>	Z	Z	Z	Z	Z

H = high level (steady state)

L = low level (steady state)

Z = high impedance (output off)

a0 ... a3, b0 ... b3 = the level of steady-state condition at I/O 0 thru I/O 3, respectively and intended as A or B Input data

F0 ... F3 = internal ALU results

QA0<sub>0</sub> ... QB0<sub>0</sub>, F0<sub>0</sub> ... F3<sub>0</sub> = the level of QA0 thru QB3 and F0 thru F3, respectively, before the indicated steady-state input conditions were established

QA0<sub>n</sub> ... QB3<sub>n</sub> = the level of QA0 thru QB3 before the most recent ↑ transition of the clock

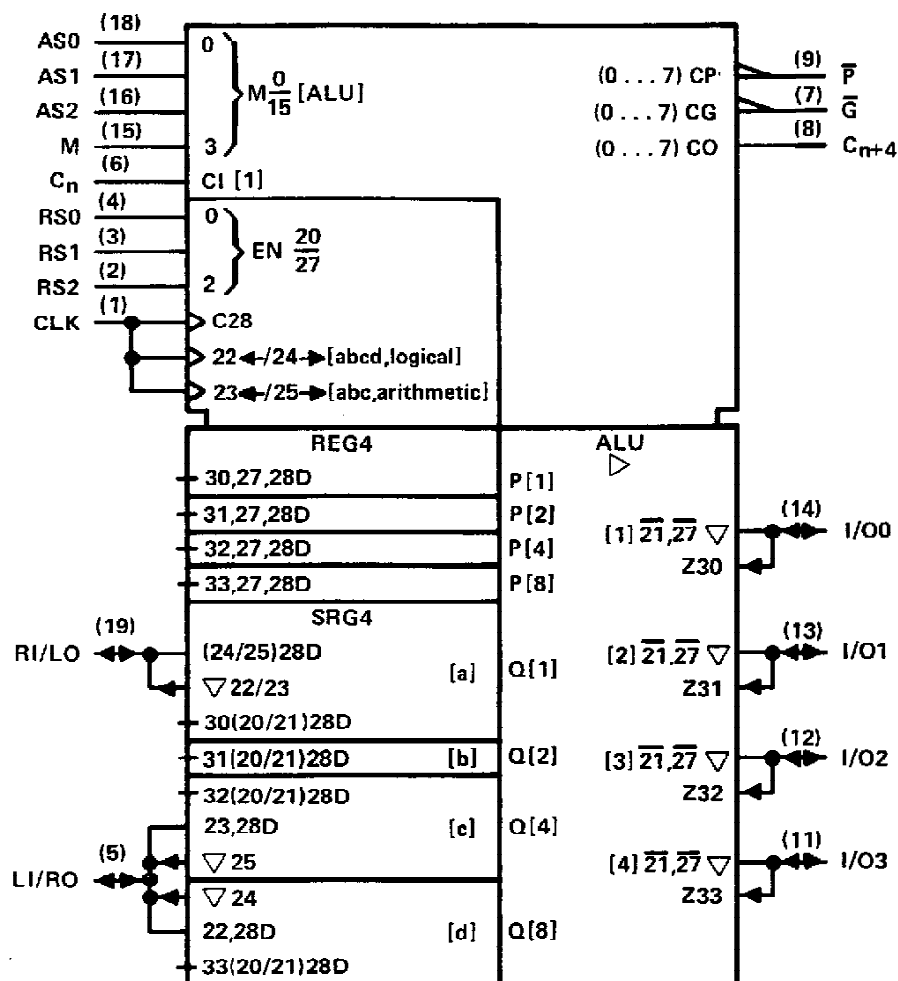
ri, li = the level of steady-state conditions at RI/LO or LI/RO, respectively

  
**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# **SN54LS681, SN74LS681** **4-BIT PARALLEL BINARY ACCUMULATORS**

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

## **absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS681	-55°C to 125°C
SN74LS681	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

**TEXAS**  
**INSTRUMENTS**

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

# SN54LS681, SN74LS681

## 4-BIT PARALLEL BINARY ACCUMULATORS

### recommended operating conditions

		SN54LS681			SN74LS681			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	LI/RO, I/O, RI/LO			-1			-2.6	mA
	$\overline{P}$ , $\overline{G}$ , $C_{n+4}$			-0.4			-0.4	mA
Low-level output current, $I_{OL}$	I/O			12			24	mA
	$C_{n+4}$ , LI/RO, RI/LO			4			8	
	$\overline{P}$			8			8	
	$\overline{G}$			16			16	
Clock frequency, $f_{clock}$		0		20	0		20	MHz
Width of clock pulse, $t_w(\text{clock})$		25			25			ns
Setup time, $t_{su}$	RS0-RS2 to CLK↑	35			30			ns
	Data I/O to CLK↑	25			25			
Hold time, $t_h$		0			0			ns
Operating free-air temperature, $T_A$		-55		125	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS681			SN74LS681			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$	High-level input voltage			2			2			V
$V_{IL}$	Low-level input voltage	$C_n$				0.7			0.7	V
		All others				0.7			0.8	
$V_{IK}$	Input clamp voltage		$V_{CC}=\text{MIN}$ , $I_I=-18\text{ mA}$			-1.5			-1.5	V
$V_{OH}$	High-level output voltage	All I/O	$V_{CC}=\text{MIN}$ , $V_{IH}=2\text{ V}$ , $V_{IL}=V_{IL\text{ max}}$ , $I_{OH}=\text{MAX}$	2.4	3.1		2.4	3.2		V
		$\overline{P}$ , $\overline{G}$ , $C_{n+4}$		2.5	3.4		2.7	3.4		
$V_{OL}$	Low-level output voltage	I/O	$V_{CC}=\text{MAX}$ , $V_{IH}=2\text{ V}$ , $V_{IL}=V_{IL\text{ max}}$	$I_{OL}=12\text{ mA}$		0.25	0.4	0.25	0.4	V
				$I_{OL}=24\text{ mA}$				0.35	0.5	
		LI/RO, RI/LO, $C_{n+4}$		$I_{OL}=4\text{ mA}$		0.25	0.4	0.25	0.4	
				$I_{OL}=8\text{ mA}$				0.35	0.5	
		$\overline{P}$		$I_{OL}=8\text{ mA}$		0.35	0.5	0.35	0.5	
		$\overline{G}$		$I_{OL}=16\text{ mA}$		0.35	0.5	0.35	0.5	
$I_{OZH}$	Off-state output current, high-level voltage applied	I/O, LI/RO, RI/LO	$V_{CC}=\text{MAX}$ , $V_{IH}=2\text{ V}$ , $V_{IL}=V_{IL\text{ max}}$ , $V_O=2.7\text{ V}$			40			40	μA
$I_{OZL}$	Off-state output current, low-level voltage applied	I/O, LI/RO	$V_{CC}=\text{MAX}$ , $V_{IH}=2\text{ V}$ , $V_{IL}=V_{IL\text{ max}}$ , $V_O=0.4\text{ V}$			-0.8			-0.8	mA
		RI/LO				-0.4			-0.4	
$I_I$	Input current at maximum input voltage	All I/O	$V_{CC}=\text{MAX}$	$V_I=5.5\text{ V}$		0.1			0.1	mA
		$C_n$		$V_I=7\text{ V}$		0.5			0.5	
		All others				0.1			0.1	
$I_{IH}$	High-level input current	$C_n$	$V_{CC}=\text{MAX}$ , $V_I=2.7\text{ V}$			100			100	μA
		All I/O				40			40	
		All others				20			20	
$I_{IL}$	Low-level input current	$C_n$	$V_{CC}=\text{MAX}$ , $V_I=0.4\text{ V}$			-4			-4	mA
		I/O, LI/RO				-0.8			-0.8	
		CLK				-0.2			-0.2	
		All others				-0.4			-0.4	
$I_{OS}$	Short-circuit output current§	I/O	$V_{CC}=\text{MAX}$	-30		-130	-30		-130	mA
		LI/RO, RI/LO, $\overline{P}$ , $\overline{G}$ , $C_{n+4}$		-20		-100	-20		-100	
$I_{CC}$	Supply current		$V_{CC}=\text{MAX}$ , RS0 at 4.5 V, All other I/O at 0 V	100	150		100	150		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operations.

‡All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TEXAS  
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

**SN54LS681, SN74LS681**  
**4-BIT PARALLEL BINARY ACCUMULATORS**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	CLOCK ↑	P̄	R <sub>L</sub> = 667 Ω,      C <sub>L</sub> = 45 pF		25	40	ns	
t <sub>PHL</sub>		30			45			
t <sub>PLH</sub>		Ḡ			26	40	ns	
t <sub>PHL</sub>		27			40			
t <sub>PLH</sub>		I/O			27	40	ns	
t <sub>PHL</sub>		29			40			
t <sub>PLH</sub>		C <sub>n</sub> +4	R <sub>L</sub> = 2 kΩ,      C <sub>L</sub> = 15 pF		36	55	ns	
t <sub>PHL</sub>		34			50			
t <sub>PLH</sub>		LI/RO			25	40	ns	
t <sub>PHL</sub>		23			35			
t <sub>PLH</sub>		RI/LO			19	30	ns	
t <sub>PHL</sub>		17			30			
t <sub>PLH</sub>	AS0-AS2	P̄	R <sub>L</sub> = 667 Ω,      C <sub>L</sub> = 45 pF		30	45	ns	
t <sub>PHL</sub>		30			45			
t <sub>PLH</sub>		Ḡ			27	35	ns	
t <sub>PHL</sub>		28			35			
t <sub>PLH</sub>		I/O			31	45	ns	
t <sub>PHL</sub>		29			45			
t <sub>PLH</sub>		C <sub>n</sub> +4	R <sub>L</sub> = 2 kΩ,      C <sub>L</sub> = 15 pF		39	55	ns	
t <sub>PHL</sub>		34			50			
t <sub>PLH</sub>	C <sub>n</sub>	P̄	R <sub>L</sub> = 667 Ω,      C <sub>L</sub> = 45 pF		9	25	ns	
t <sub>PHL</sub>		9			20			
t <sub>PLH</sub>		I/O			17	35	ns	
t <sub>PHL</sub>		13			20			
t <sub>PLH</sub>		C <sub>n</sub> +4	R <sub>L</sub> = 2 kΩ,      C <sub>L</sub> = 15 pF		20	30	ns	
t <sub>PHL</sub>		16			25			
t <sub>PLH</sub>	MODE	P̄	R <sub>L</sub> = 667 Ω,      C <sub>L</sub> = 45 pF		28	40	ns	
t <sub>PHL</sub>		29			40			
t <sub>PLH</sub>		Ḡ			21	30	ns	
t <sub>PHL</sub>		23			30			
t <sub>PLH</sub>		I/O			30	45	ns	
t <sub>PHL</sub>		28			40			
t <sub>PLH</sub>		C <sub>n</sub> +4	R <sub>L</sub> = 2 kΩ,      C <sub>L</sub> = 15 pF		40	60	ns	
t <sub>PHL</sub>		37			50			
t <sub>PZH</sub>	RS1-RS2	I/O	R <sub>L</sub> = 667 Ω	C <sub>L</sub> = 45 pF	28	45	ns	
t <sub>PZL</sub>				28	45			
t <sub>PHZ</sub>				C <sub>L</sub> = 5 pF	35	65	ns	
t <sub>PLZ</sub>				39	65			
t <sub>PZH</sub>		LI/RO	R <sub>L</sub> = 2 kΩ	C <sub>L</sub> = 15 pF	25	40	ns	
t <sub>PZL</sub>				22	40			
t <sub>PHZ</sub>				C <sub>L</sub> = 5 pF	21	40	ns	
t <sub>PLZ</sub>				34	60			
t <sub>PZH</sub>		RI/LO	R <sub>L</sub> = 2 kΩ	C <sub>L</sub> = 15 pF	22	40	ns	
t <sub>PZL</sub>				24	40			
t <sub>PHZ</sub>				C <sub>L</sub> = 5 pF	11	30	ns	
t <sub>PLZ</sub>				16	40			

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.