Texas Instruments

Advanced System Logic SPOTLIGHT

Key Features and Benefits

- Transparent Serial Addressing Protocol supports:
  - — 4/5-wire multidrop system-level TAP
  - — Separate addressing and scan operations
  - — Reuse of module-level vectors
- System-level solution provides:
  - — Design verification, system integration and manufacturing test
  - — In-situ board test and board-to-board test
- 10-bit address space
- 24-pin TSSOP package

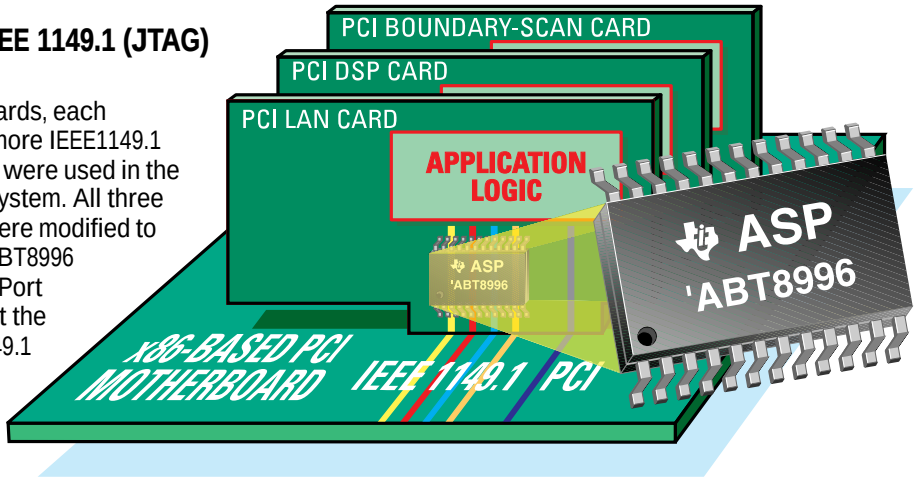
Send for your Boundary-Scan Logic IEEE Std. 1149.1 (JTAG) Data Book today!

'ABT8996 Addressable Scan Port (ASP)

Extending IEEE 1149.1 (JTAG) across system-level test solutions

How PCI and IEEE 1149.1 (JTAG) work together

Three PCI add-in cards, each containing one or more IEEE1149.1 integrated circuits, were used in the proof-of-concept system. All three PCI add-in cards were modified to include a TI SN74ABT8996 Addressable Scan Port (ASP) IC to connect the backplane IEEE 1149.1 bus to the card's internal IEEE 1149.1 bus.



The combination of a PCI local bus, IEEE 1149.1 signals on the backplane and PCI add-in cards with ASPs demonstrates a flexible, hierarchical embedded test solution.

Today, testing is one of the major challenges designers and testers of multidrop bus systems face. The new addressable scan port (ASP) from Texas Instruments meets this challenge by providing a flexible, cost-effective way to achieve IEEE 1149.1 (JTAG) testing at the system level.

System-level test solutions

Designated SN74ABT8996, the device uses a switch-based architecture that directly connects the primary test access port (TAP) to secondary TAPs using TI's addressable shadow port technology. This allows the device to provide IEEE 1149.1 (JTAG) testing across board, module and system levels. TI's addressable shadow port technology logically separates addressing operations from scan operations. Thus, it allows chip and board scan test vectors to be reused directly within a system context.

'ABT8996 features

The 'ABT8996 features a wide 10-bit address space that provides flexibility in assigning fields for physical address, logical address or module function. In addition, it allows a total of 1,021 ASPs to be placed on a multi-drop bus to be selectively addressed for individual tests or globally controlled for BIST operations.

TI's ASP device is designed for easy implementation with PCI-based systems as well as other embedded bus architectures. Combined with a PCI bus system, designers can implement a flexible, hierarchical embedded test solution. (See PCI application diagram above.)

For the ultimate in space savings, the device is available in a 24-pin TSSOP. Other package options are also available.

Broadest portfolio of IEEE 1149.1 (JTAG)

The 'ABT8996 is part of the industry's broadest portfolio of IEEE 1149.1 (JTAG) boundary-scan logic devices. In all, TI offers over 40 boundary-scan logic devices available in octal, Widebus™ and scan support functions in the ABT, ACT, BCT and LVT families. Bus hold and series resistor options are also available.

The 'ABT8996 is available today from Texas Instruments and authorized distributors. For information on pricing and availability, please contact your local TI field sales office.

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