JTAG Boundary Scan Logic

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JTAG Boundary Scan Logic Devices

TERMS

1. JTAG - Joint Test Action Group

2. SCOPE - System Controllability Observability Partitioning Environment

3. BSL - Boundary Scan Logic

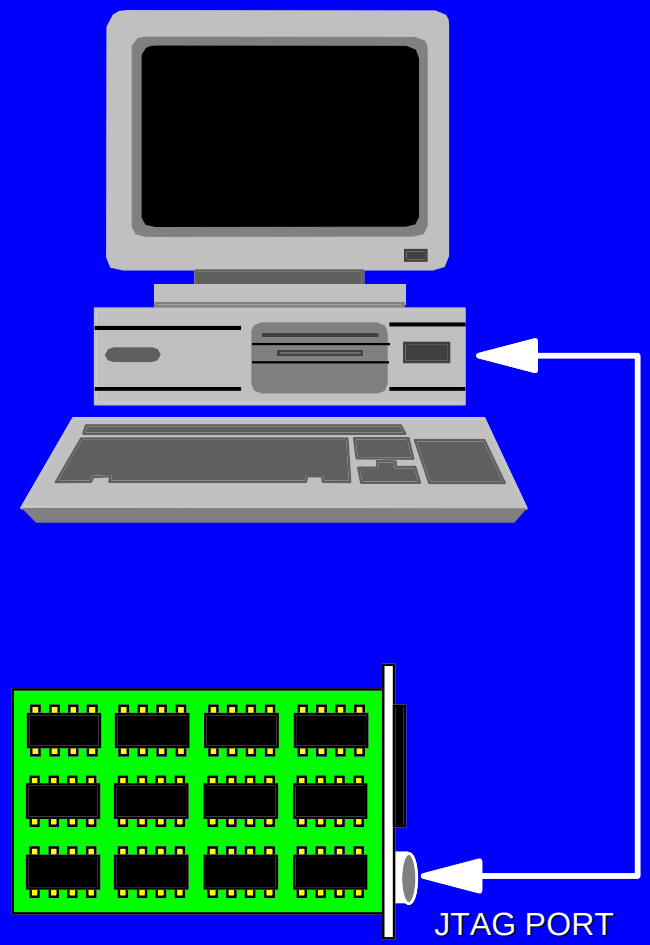
Boundary Scan Agenda

- What Is JTAG ? (5 minutes)
- The Boundary Scan Idea (25 minutes)
- Typical Applications (15 minutes)
  - Interconnect Testing
  - Logic Cluster Testing
  - Memory Testing
  - System-Level Test
- Design Considerations (20 minutes)
- TI's JTAG Boundary Scan Devices (5 minutes)
- Q & A (5 minutes)

Standard Approach To Test

- Developed by over 200 SC vendors/ATE end-equipment manufacturers in mid '80's
- Sanctioned by IEEE In 1990
- Primary focus was board-level manufacturing defects
- Solution: Place test points within the silicon
- Ensure compatibility between all IEEE 1149.1 compliant devices and tools

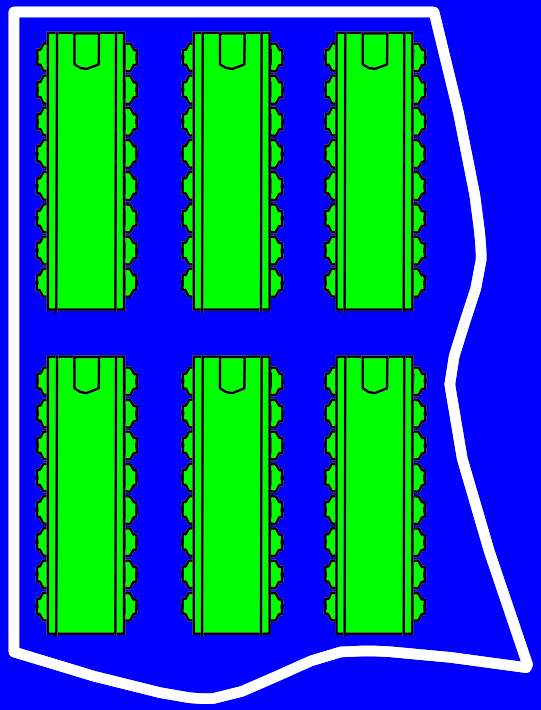
JTAG Supports Board Test . . . And More



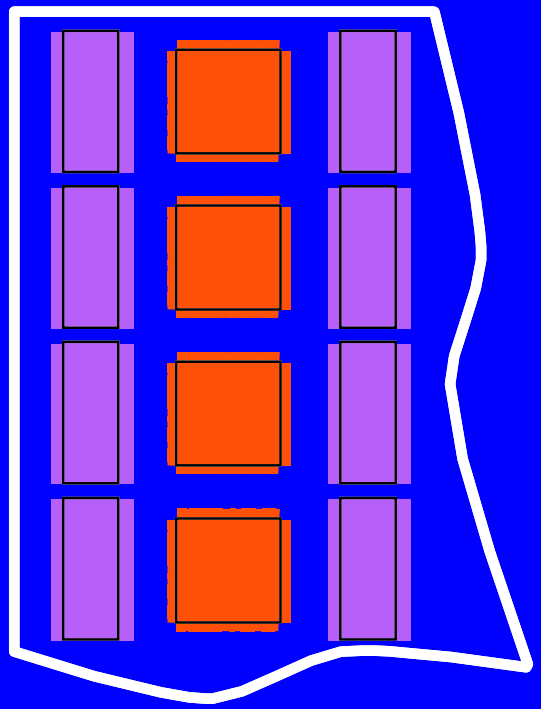
- Developed for board interconnect test
- Tester "speaks" to board via JTAG port
- Execute variety of functional tests
- Benefits all product phases
  - Design verification/debug
  - Hardware/software integration
  - Manufacturing
  - Field support
  - Tests can be reused
  - Chip, board, system

The Increasing Problem Of Board Test

- The incredible shrinking board results in loss of test access



Yesterday



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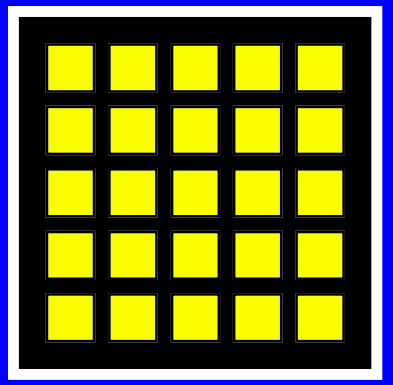
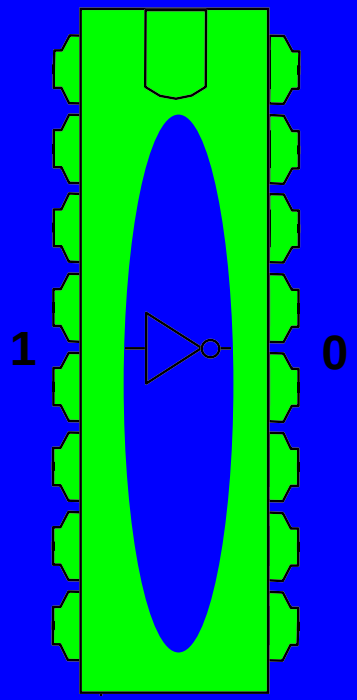


Tomorrow ?

The Increasing Problem Of Board Test

- Increasing integration at chip level complicates controllability



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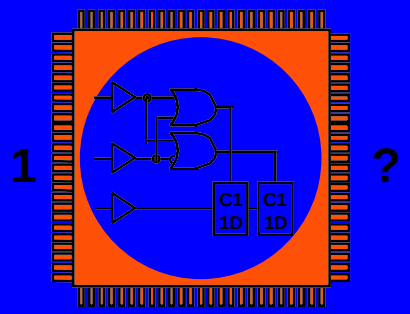
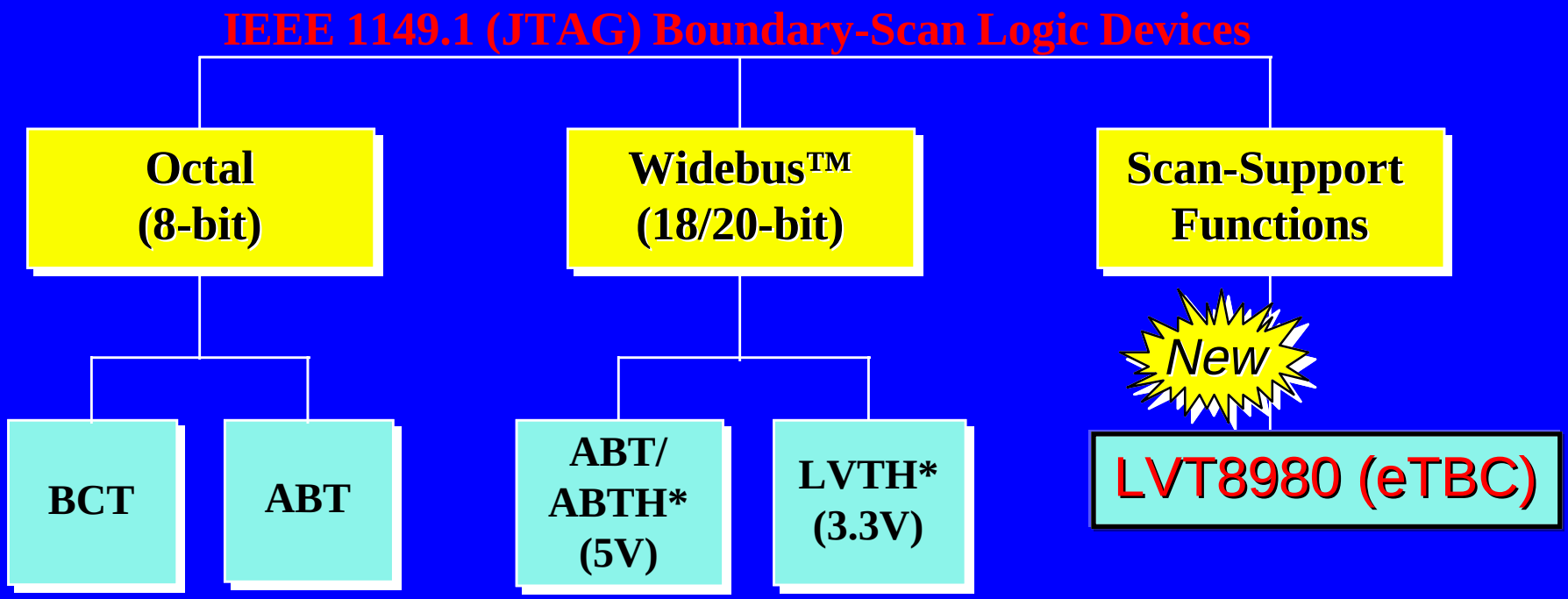


Today

What Does TI Offer in IEEE 1149.1 (JTAG) Silicon Solutions?

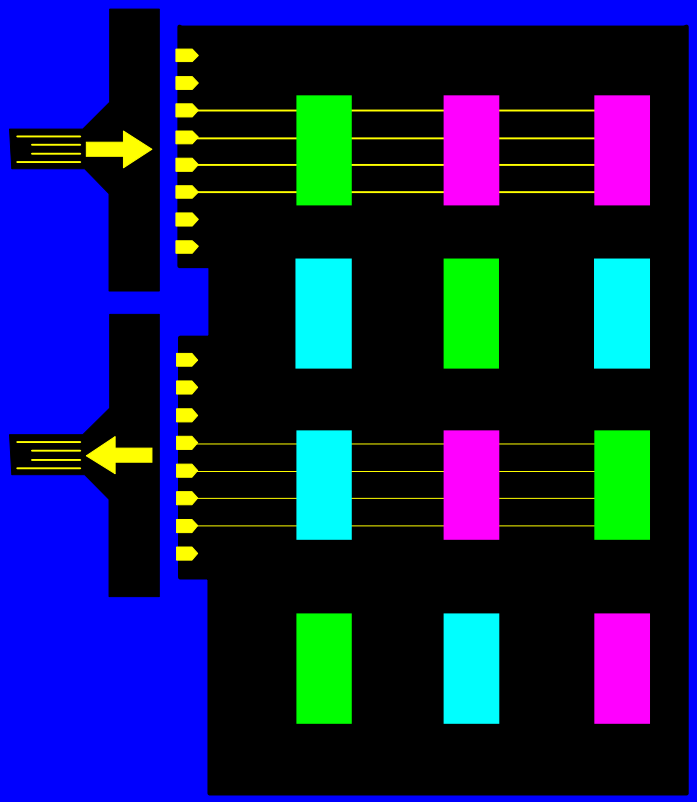
30+ commercially released devices



* Bus Hold option

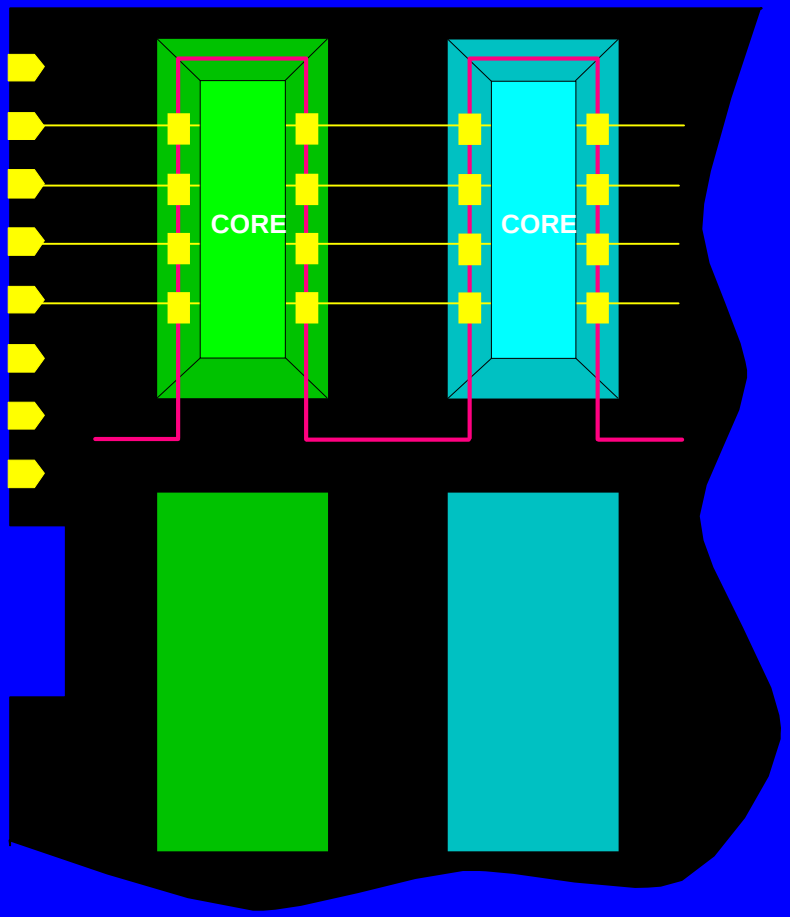
Conventional Methods of Board Test

Functional Test ('Edge-Connector' Test)



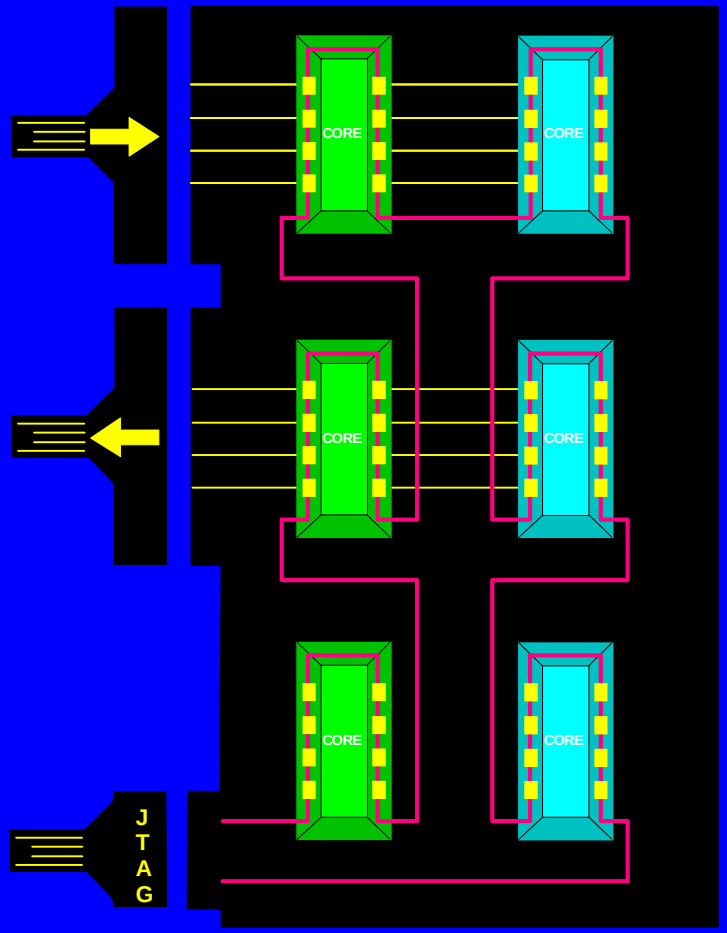
- Based on board function, rather than structure
- Test generation primarily manual
- Test access limited to primary I/O only

The Boundary Scan Idea



- Scan provides a means to arbitrarily observe test results and source test stimulus
- Scan method requires minimal on chip/board resources (pins/nets)

Boundary Scan Method of Board Test



- Based on board structure; Not limited by chip function/ complexity
- Test access is not limited by board physical factors

Benefits of Boundary Scan

- Controllability and observability w/o physical access
- Reduced number of test points needed on PCB
- Reduced number of pins needed for ‘Bed-of-Nails’ testers
- Eliminates need for ICT models for JTAG parts
- Allows for quick identification and isolation of defects
- Industry standard ensures inter-operability between vendors

Can't Afford Not To Test

Cost will increase by a factor of ten as fault finding moves from one level of complexity to the next. The result:

- *Reduced Profit Margins*
- *Delayed Product Introduction*
- *Dissatisfied Customers*

1. Device level	1 unit of cost
2. Board level	10 units of cost
3. System level	100 units of cost
4. Field level	1,000 units of cost

Boundary Scan Success Stories

- "We've (AT&T) reduced the number of test points on some boards from 40 down to four and shortened test-debug time on some products from six weeks to two days." [1]
- Hewlett Packard printers reduced drawing board to production time from four and one half years to two years. [2]
- Test program development time on Intel '386 vs. Intel '486 with JTAG: [3]

Intel '386	Intel '486
Seven weeks	Ten hours (two hours if vendor supplied BSDL)

- Controller design company using two programmable logic devices with boundary scan were able to use low cost tester with ATPG ($25K) instead of standard ATE system ($750K) that would have been used without boundary scan. [4]

1 Computer Design, January 1994, "Testing Dilemmas and Corporate Alliances Fuel Boundary Scan's Acceptance"

2 Test and Measurement World, October 1992, "Concurrent Engineering is Common Sense"

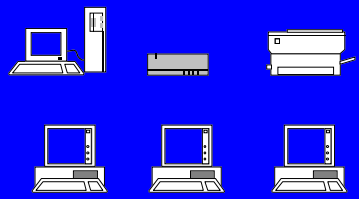
3 Computer Design, November 1992, "Design and Test Engineers Alter Rules to Facilitate Test"

4 EDN, December 3, 1992, "No 'Accounting' for Boundary Scan Test"

End Equipment Designing with JTAG Boundary-Scan

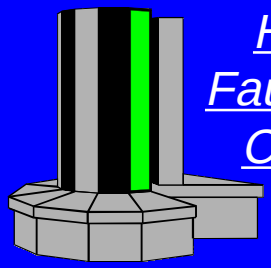
Telecom

Networking

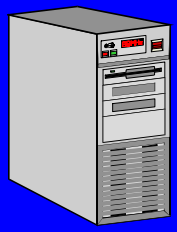


Military

High End Fault Tolerant' Computers

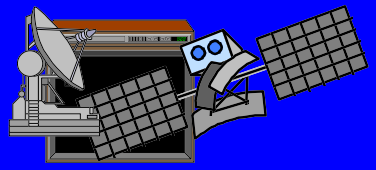


Mid-Range 'Server' Computers

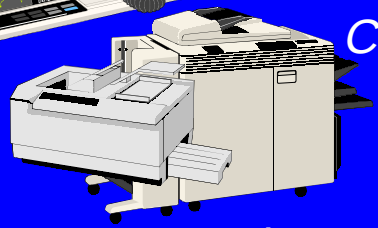


Imaging Systems

Medical

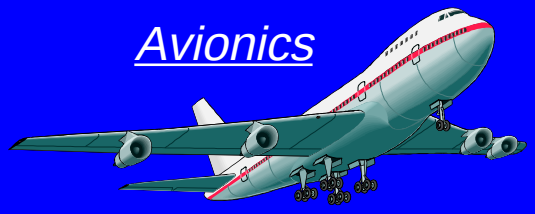


Conferencing



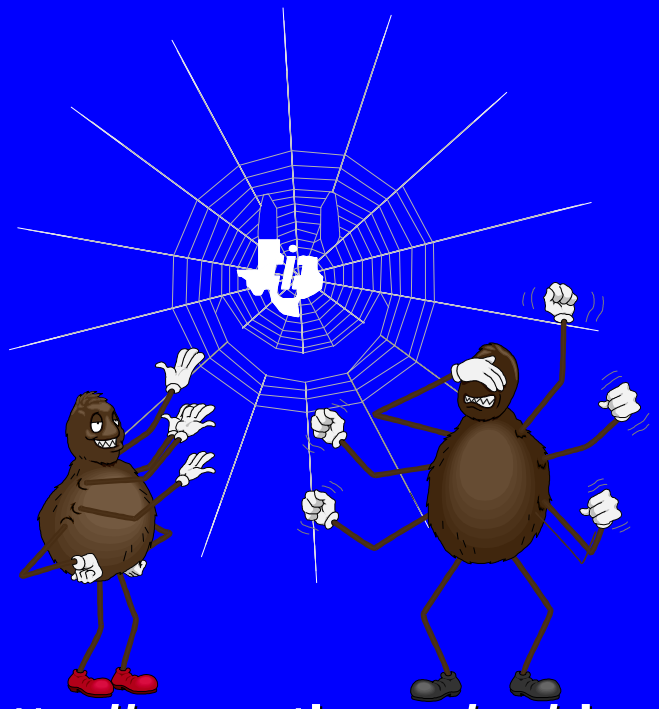
Copiers

Avionics



Consumer

Contact Us For More Information on JTAG Devices



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http://www.ti.com/sc/docs/jtag/jtaghome.htm

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