Texas Instruments

Advanced System Logic SPOTLIGHT

Low Voltage CMOS

- 5V I/O tolerant
- -24/24 mA drive
- 4.1 ns typical propagation delay; 6.5 ns max. ('244/'245)
- Ultra-low standby power (10 µA)
- Enhanced options include “bus hold” and series damping resistors

Selected devices will be available in Military versions.

Packaging options:
SOIC (D, DW)
SSOP (DB)
TSSOP (PW)
Widebus™ (DL)
Shrink Widebus™ (DGG)

LVC: 5V-tolerance
for mixed-mode systems

LVC is the ideal family for low-voltage or mixed-voltage systems. While LVC operates at 3.3V, LVC also enables interface to 5V components by providing 5V-tolerant inputs and/or outputs.

With typical propagation delays of 4.1 ns for octals (6.5 max.) and balanced drive ±24 mA, LVC delivers performance similar to that of 74F. And, with ultra-low power consumption (10 µA @ 3.6 V_{CC}), LVC hits the “sweet spot” designers need for today’s low-power/high-performance application demands.

Interfacing 3.3V devices to 5V devices requires consideration of the logic switching levels of the driver and the receiver. Figure 1 illustrates the various switching standards for 5V CMOS, 5V TTL and 3.3V LVTTL.

The switching levels for the 5V TTL and the 3.3V LVTTL are identical. This makes bidirectional level translation simple when using a 5V-tolerant 3.3V solution (LVC).

If 5V-tolerant, a 3.3V LVTTL device is also fully compatible with 5V CMOS inputs. This makes LVC an ideal unidirectional level translator. (5V CMOS → 3.3V LVTTL)

TI has a fully populated family of over 50 gate, octal, and Widebus functions to support your high volume needs NOW! That is more than any low voltage family from any supplier in the industry.

Just another reason why TI is the leading and largest supplier of low-voltage logic.

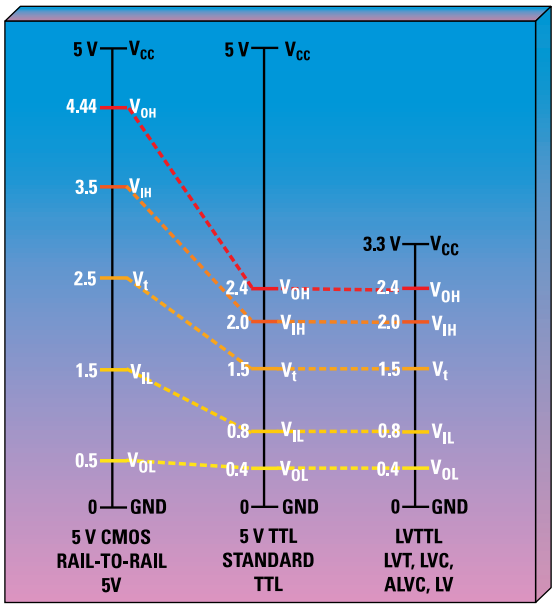

Figure 1

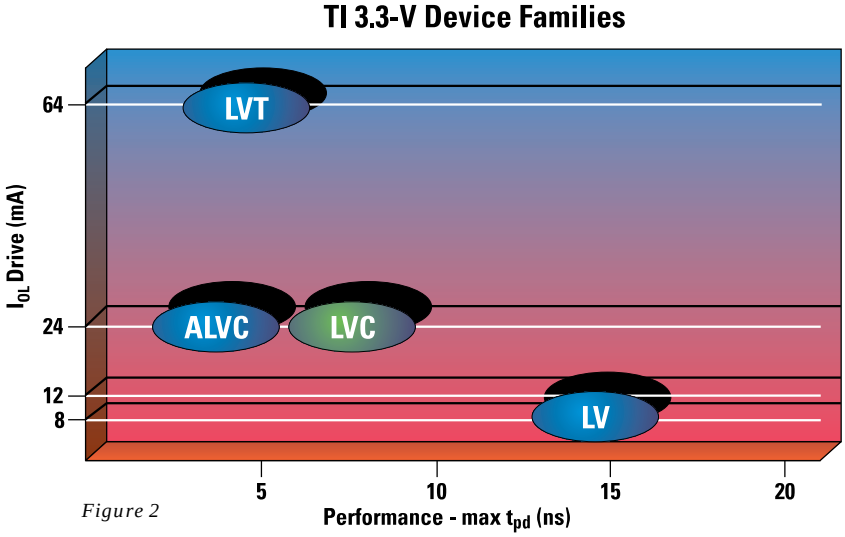

Figure 2

Printed in U.S.A. on recycled paper by Munoz Printing, Dallas, Texas