



## **Release Document**

**Xilinx  
Foundation Series  
Version 6.0.1  
July, 1996**

**Read This Before Installation**



# Versions and Compatibility

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The following master table indicates Xilinx core software with the current version numbers.

## Software Versions

Program	Windows Version	DOS Version	Workstation Version
APR	5.2.0	5.2.0	5.2.0
APRLOOP	5.2.0	5.2.0	5.2.0
CstCvt	5.2.1	5.2.1	5.2.1
Design Manager	6.0.1	N/A	N/A
Floorplanner	6.0.1	N/A	5.2.1
Flow Engine	6.0.1	N/A	N/A
Hardware Debugger	6.0.0	N/A	N/A
HM2RPM	5.2.1	5.2.1	5.2.1
LCA2XNF	5.2.1	5.2.1	5.2.1
MakeBits	5.2.1	5.2.1	5.2.1
MakePROM	5.2.1	5.2.1	5.2.1
MAP2LCA	5.2.0	5.2.0	5.2.0
MemGen	5.2.1	5.2.1	5.2.1
PPR	5.2.1	5.2.1	5.2.1
PROM File Formatter	6.0.0	N/A	N/A
Report Browser	6.0.1	N/A	N/A
SymGen	5.2.1	5.2.1	5.2.1
Timing Analyzer	6.0.0	N/A	N/A

<b>Program</b>	<b>Windows Version</b>	<b>DOS Version</b>	<b>Workstation Version</b>
XACT	5.2.1	5.2.1	5.2.1
XACT8000	1.1F	N/A	N/A
XBLOX	5.2.1	5.2.1	5.2.1
XChecker	5.2.0	5.2.0	5.2.0
XCK88	N/A	5.2.0	N/A
XDE	5.2.1	5.2.1	5.2.1
XDelay	5.2.1	5.2.1	5.2.1
XDM	N/A	N/A	5.2.1
xdm	5.2.1	5.2.1	5.2.1
XEMake	N/A	N/A	5.2.1
XEMake6	6.0.1	N/A	N/A
XKey	6.0.0	5.2.1	N/A
XMake	5.2.0	5.2.0	5.2.0
XNFBA	5.2.1	5.2.1	5.2.1
XNFCvt	5.2.0	5.2.0	5.2.0
XNFMAP	5.2.0	5.2.0	5.2.0
XNFMerge	5.2.0	5.2.0	5.2.0
XNFPrep	5.2.1	5.2.1	5.2.1
XPP	5.2.0	5.2.0	5.2.0
XPrint	5.2.1	5.2.1	5.2.1
XSimMake	5.2.1	5.2.1	5.2.1

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## Introduction

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Welcome to the Xilinx Foundation Series Package from Xilinx! This release note supports the following products:

- Xilinx Foundation Base
- Xilinx Foundation Base-VHDL
- Xilinx Foundation Standard
- Xilinx Foundation Standard-VHDL

Xilinx software products have prefixes to designate the type of products you receive:

- DS = Development System (new system)
- DX = Development System Upgrade (upgrade to current system)
- SC = Support Contract (update to current system)
- SR = Support Re-instatement (update for non-current system)
- BU = Base update (upgrade to current system)

The labels on the box indicate the product that you have received.

## Contents

The Development System (DS) product that you received contains software, documentation, hardware, or all three. New DS Base, Base-VHDL, Standard, and Standard-VHDL packages contain hardware, software, and documentation. Upgrade and update products contain software and documentation only.

## Hardware<sup>1</sup>

The hardware consists of the following items.

- JTAG Parallel Download Cable (Included in DS-560 and DS-571 for the PC and all other PC platform packages)
- XChecker Download and Readback Cable set (Included in all packages and the DS-560 for the workstation - Not included in the DS-560 and DS-571 for the PC)
- Xilinx “C” Programmable Key (a beige key included in Base and Standard packages)

## Software

The Xilinx Foundation Series provides software solutions on the following CD-ROMs:

- Xilinx Foundation Series, version 6.0.1
- Xilinx XACTstep, version 5.2.1/6.0.1
- Xilinx DS-560 XACT CPLD XC9500 Core Tools & Interfaces, version 6.0.1
- MasterClass Lite multimedia VHDL tutorial<sup>2</sup>

## Documentation

The following documentation is available in print for the Foundation Series package:

- *Third-Party Alliance Release Note*
- *Getting Started & Installation Guide for XACTstep*
- *Xilinx Foundation Series Release Note and Installation Guide*
- *Xilinx ABEL Software Design Reference Manual from Data I/O*
- *DS-560 XACT CPLD XC9500 Core Tools & Interfaces, version 6.0.1 Release Document*

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1. Included in DS packages only

2. Included in Xilinx Foundation Base-VHDL and Standard-VHDL packages

## Online Documentation

The following online documentation is included with the Foundation Series package:

- *Libraries Guide*
- *Libraries Supplement Guide*
- *X-BLOX Reference/User Guide*
- *Floorplanner Reference/User Guide*
- *Design Manager/Flow Engine Reference/User Guide*
- *Timing Analyzer Reference/User Guide*
- *Hardware Debugger Reference/User Guide*
- *PROM File Formatter Reference/User Guide*
- *Development System User Guide*
- *Development System Reference Guide, Volumes 1-3*
- *Hardware & Peripherals User Guide*
- *XEPLD Reference Guide (for Windows)*
- *XEPLD Schematic Design Guide (for Windows)*
- *Foundation Project Manager*
- *Foundation Project Editor*
- *Foundation Logic Simulator*
- *Foundation Synthesis Tools*
- *Foundation Tutorials*
- *Foundation Configuration*

## Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with a warranty<sup>1</sup>; you will receive all software and documentation updates automatically during that time. With Standard and Standard-VHDL packages, you will receive a notice at the end of the warranty period giving instructions on how to renew your maintenance contract. For Base and Base-VHDL packages, you will be contacted within a month before a new software release becomes available with instructions on how to acquire it.

## VHDL Synthesis

This section contains information about VHDL synthesis in the Foundation Series software.

### VHDL Only for Module Creation (FPGA Designs)

The VHDL functionality in Xilinx Foundation Series is for module creation only. For the initial release of Xilinx Foundation Series, XVHDL should not be used to create all-VHDL designs. (This does not apply to CPLD designs.) A design should always have a top-level schematic, which can contain modules that correspond to VHDL descriptions.

### D Latch Synthesis Template

Using the “D Latch” synthesis template, which is found in the HDL Editor Language Assistant, is not recommended in XC3000/XC4000 designs. Latches are inferred in these devices by creating a combinatorial feedback loop, which cannot be processed by the ImproveX optimizer that is used in the VHDL synthesis process. Use a D flip-flop instead.

### XVHDL State Machine Encoding

The XVHDL state machine encoding is binary by default. See the “One- Hot Encoding” section of Chapter 8, “Synthesis of VHDL Types,” in the *Synthesis Online Users Guide* for details on how to use one-hot encoding. This encoding method, which assigns one flip-flop to every state in a state machine, is preferred for Xilinx XC3000, XC4000, and XC5000 FPGAs.

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1. Three-month warranty for Base and Base-VHDL

## Inferred Primitives

XVHDL infers the design elements in the following list in the output netlist on the basis of the logic structures found by the compiler in a VHDL design:

AND	OBUF
BUF	OBUFFT
BUFG	OR
DFF	OUTFF
DLAT	OUTFFT
IBUF	TBUF
INFF	XNOR
INLAT	XOR
INV	

## Instantiated Primitives

You can instantiate some Xilinx Unified Library Primitives into a VHDL source file. Refer to

`ACTIVE\VHDL\XLNX_LIB\README.TXT`

for more information and a list of components that can be instantiated.

## Inferred X-BLOX Components

XVHDL infers the following X-BLOX components on the basis of the logic and arithmetic functions encountered by the compiler in the VHDL design:

ADD\_SUB  
COMPARE  
COUNTER  
ACCUMULATOR

## Instantiated X-BLOX Components

You can insert the following X-BLOX components into a design, if they apply to the target architecture, by explicitly instantiating them in VHDL. (See Chapter 11 of the *Synthesis Online Users Guide* for more information.)

ACCUM	MUXBUS2
ADD_SUB	MUXBUS4
ANDBUS	MUXBUS8
ANDBUS1	ORBUS
ANDBUS2	ORBUS1
CLK_DIV	ORBUS2
COMPARE	PROM
COUNTER	SHIFT
DATA_REG	SRAM
DECODE	TRISTATE
INC_DEC	XORBUS
INVBUS	XORBUS1
MUXBUS	XORBUS2

## Installation

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This chapter explains how to install Xilinx Foundation Series version 6.0.1 and the MasterClass Lite tutorial.

### Installing the Foundation Series Software

#### Minimum System Requirements

Installation of the Xilinx Foundation Series software requires the following:

- 486 or Pentium-class PC
- 130 MB free disk space
- Mouse or similar pointing device
- Free parallel port (for Xilinx security key)
- MS-DOS 6.0 or later
- Microsoft Windows 3.1, Windows 3.11, or Windows for Workgroups
- RAM memory

The following table indicates the recommended memory for implementing FPGA and EPLD designs. Memory requirements are environment- and design-dependent. The Windows operating system adds additional memory overhead, as do any active Windows applications. Some designs can be implemented using less than the specified memory, but complicated or large designs may require additional memory.

Recommended Memory	Recommended Windows Swap Space	Device Ranges
16 MB RAM	16 MB	XC2000 (all devices) XC3x20x — XC3x42x (all variants) XC7000 (all devices) XC3x64x — XC3x90x XC4002x — XC4006x (all variants) XC5202 — XC5204 XC9000 (all devices)
32 MB RAM	32 MB	XC3195x (all variants) XC4008x — XC4013x (all variants) XC5206 — XC5215 (all variants)

**Note:** When you run Xilinx Foundation Series version 6.0.1, 460 KB of free conventional memory is recommended. This number reflects the free conventional memory available while Windows is running.

## Custom Installation

A complete installation of the Xilinx Foundation Series software takes approximately 125 megabytes. If your system does not have this much free disk space, you can perform a custom installation. The following table lists approximate sizes of each installation option.

Module	Megabytes
Executables (required)	22
VHDL synthesis	7
Xilinx ABEL <sup>a</sup>	7
Online documentation	16
Device libraries	38
Sample projects	29
Tutorials	3

a.This may have already been installed by the XACTstep 6.0.1 installation program.



## Installation Instructions

Follow these instructions to install the Foundation Series software.

1. *Install the Xilinx XACTstep version 5.2.1/6.0.1 software before installing the Xilinx Foundation Series software.* Please see the *Getting Started and Installation Guide* for instructions. (If you are using the XACT-CPLD software, which is required for targeting XC9000 devices, install that package at this time. Please see the *DS-560 XACT-CPLD Release Document* for installation instructions.)

2. Insert the Xilinx Foundation Series CD-ROM into your CD-ROM drive.

3. Exit all Windows applications except for the Program Manager.

4. From the Program Manager, select **File** → **Run**.

The Run dialog box appears.

5. Type the following into the dialog box:

`R:\WIN32S\1_30\DISK1\SETUP.EXE`

where *R* is the drive letter of your CD drive.

6. Follow the instructions on the screen to install Win32s version 1.30. (It is suggested that you install the optional “Freecell” game that is included with Win32s when prompted to do so. Freecell can be used to verify that your Win32s installation has been successful.) You will have to re-boot your machine before continuing.

7. Exit all Windows applications except for the Program Manager.

8. From the Program Manager, select **File** → **Run**.

The Run dialog box appears.

9. Type the following into the dialog box:

`R:\INSTALL.EXE`

where *R* is the drive letter of your CD drive.

10. Follow the instructions as they appear on the screen. You will probably want to perform a complete installation if your machine has the disk space.

**Note:** The Xilinx ABEL application is loaded by the Complete installation option if it has not already been installed by the XACTstep installation program. If you will not be using Xilinx ABEL and wish to conserve disk space, select the Custom installation and deselect the Xilinx ABEL option. You can install this option at a later date if you find that you require it.

After you install the main Xilinx Foundation software, the installation program prompts you to press OK to begin the Adobe Acrobat document reader installation program. Xilinx does not recommend that you install this version of Acrobat, because the Acrobat version provided on this CD, a subset of the LE version, does not have the enhanced searching capabilities that LE has. Therefore, press **Cancel**, not OK. If you did not install Acrobat LE as a part of your XACTstep 5.2.1/6.0.1 installation, you can access the Acrobat LE installation program directly by inserting the XACT 5.2.1/6.0.1 CD-ROM into your drive and typing the following:

**R:\ACROBAT\DISK1\SETUP.EXE**

where *R* is the drive letter of your CD drive.

11. Select **OK** when the installation program asks if you wish to reboot your PC.
12. To get started on the Xilinx Foundation Series software, click on the Foundation Tutorial icon in the Foundation Series program group to access the QuickStart interactive tutorial. This tutorial provides descriptions, step-by-step instructions, and demonstrations of the Xilinx Foundation Series tools.

## Installing the MasterClass Lite Tutorial

### Minimum System Requirements

Installation of the MasterClass Lite tutorial requires the following:

- 486-based PC at 25 MHz running Windows 3.1
- 4 MB of RAM and 10 MB of free hard-disk space
- Double-speed CD-ROM drive local to the PC
- Mouse or similar pointing device

- 8- or 16-bit Soundblaster™-compatible sound card (optional)

## Installation Instructions

Follow these steps to install and run the MasterClass Lite tutorial on your PC.

1. Load the CD in your CD drive.
2. In Windows, choose the Program Manager.
3. Select **File** → **Run**.

The Run dialog box appears.

4. Type the following:

`R:\mcvhd1\program\setup.exe`

where *R* is the drive letter of your CD drive.

5. When the Welcome message appears, click on **Continue**.

The installation directory dialog box appears.

6. Delete the directory name suggested and enter the letter of your hard disk and a full directory name, for example, c:\mclass. You can load up to 5 MB of files.
7. Click on **Continue**.
8. When the installation is complete, click the **OK** button.
9. Further installation steps are required if you have several CD drives available on your system, or if you are using an 8-bit sound card. See the *Getting Started and Installation Guide* for further details.

## MasterClass Tutorial

This section contains release note information about the MasterClass tutorial that accompanies the Foundation Series VHDL packages.

## Networked CD Drives

MasterClass is designed to operate from the CD drive local to your PC and cannot be accessed over a network.

## Displaying Version Information

You can obtain the version number of the MasterClass executables any time that MasterClass is running by pressing Alt V.

## Keyboard Commands

You can access the MasterClass user interface from keyboard commands rather than menu commands. The keys are assigned as follows.

<b>Keystroke</b>	<b>Function</b>
Return	Next point
Right arrow	Next point
Left arrow	Previous point
Down arrow	Next topic
Up arrow	Previous topic
Alt A	Answer A
Alt B	Answer B
Alt C	Answer C
Alt D	Answer D
Alt V	Version information
Ctrl I	Index
Ctrl C	Contents
Ctrl R	Reference guide
Ctrl T	Tutorial
Ctrl O	Home
Ctrl S	Getting started
Ctrl E	Exit MasterClass
Ctrl H	Help
Ctrl P	Code “Cut and paste”
Alt 1	Display point 1
Alt 2	Display point 2
Alt 3	Display point 3

Keystroke	Function
Alt 4	Display point 4

## Selecting 8-Bit or 16-Bit Sound Files

Sound can be recorded on a PC with either 8-bit or 16-bit resolution. The tutorial offers both 8- and 16-bit files and uses the 16-bit files by default. If you cannot hear the sound on your system, it is probably because your sound card only supports 8-bit sound files.

To enable the tutorial to access the supplied 8-bit sound files, edit the following text file:

```
MC_ROOT\variable\user.var
```

where *MC\_ROOT* is the directory that you specified during the installation of MasterClass.

You will find the following two lines:

```
@AUDIO_PATH  
audio16
```

Change these lines to read as follows, then re-invoke the tutorial.

```
@AUDIO_PATH  
audio8
```

## Troubleshooting

If you have difficulty running MasterClass, consult the following list of problems and possible solutions.

### No Sound Commentary Plays During the Tutorial

Is your MCI Sound driver installed? To check this in Windows 3.1, invoke the Windows Control Panel, found in the Main program group of the Program Manager.

Double-click on the Drivers icon. Scroll down the list of installed drivers, and check for the [MCI]Sound entry. If you do not find the entry, click on the Add button, and select the [MCI]Sound option to install it. If you do not have the specific sound driver available, contact your sound card manufacturer and request the driver for the Windows 3.1 operating system.

Also, is your sound card Soundblaster-compatible? If not, use a PC that contains a Soundblaster-compatible sound card.

## **The Text Appears Distorted In a Specific Part of the Application**

The correct fonts may not be installed on your PC. The following table shows the fonts used in each part of the MasterClass display:

Arial 18-point bold	Title
Arial 14-point bold	Points
Arial 10-point regular	Exercises
Arial 11-point regular	Commentary
Arial 17-point bold	Contents page

Ensure that your PC displays each of these fonts in the specific size just given.

## **Tutorial Appears with No Graphics**

When invoking MasterClass, you receive the following message:

```
Do you wish to continue your previous session?
```

You select “Yes,” and the tutorial window appears but contains no graphics.

If this message appears when invoking the tutorial, always respond with “No.”

## **Unable to Run Setup.iw**

During installation, or when setup.iw is invoked, you receive the following message:

```
Unable to run setup.iw
```

The disk that you specified during the installation procedure is full.

Remove all of the files that were created by the installation, and ensure that at least 8 MB of free space is available before re-installing the MasterClass demonstration.

## **Display Changes Appearance**

While using MasterClass, the display behaves strangely, fonts change appearance, and so forth.

Exit MasterClass using the Windows Close command from the menu in the top left corner of the MasterClass window.

This problem occurs because all of the memory (or resources) that Windows has allocated to the graphics driver has been used up. Quit any other applications that are running, and run MasterClass again. If the problem persists, try to re-organize the way in which the memory usage is set up on your PC to optimize the memory allocated to MS-DOS. Refer to your PC's documentation or ask your system administrator to perform this operation.

## **Support**

If the solutions listed in the previous section do not correct the issues that arise in running MasterClass, please contact Xilinx technical support. Your first contact should be by e-mail or fax, specifying the following information:

- Make of PC
- Processor and speed
- Memory installed (RAM)
- Make and model of sound card (if applicable)
- Versions of Windows and DOS that you are running
- A description of the problem





# Chapter 3

## Features in This Release

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This release of the Foundation Series software offers support for new Xilinx device families XC4000E, XC8100, and XC9500.

### XC4000E and XC9500 Support

This release of the Foundation software includes support for the XC4000E and XC9500 device families. Support includes schematic entry, simulation, ABEL and VHDL synthesis, and project management. The implementation software for the XC9500 family is included in the DS-560 CD. Software for the XC4000E family is included in the XACTstep version 6.0.1 CD.

### XC8100 Support

This release of the Foundation software includes support for the XC8100 family in the Project Manager. Schematic libraries are also included for the XC8100 family.

Simulation libraries and the XC8100 place and route software were not available when this package shipped but they will be completed within one month. Please send in your registration card in order to receive a free update of the XC8100 simulation library and back-end software.

## Other Product Features

### Interactive Tutorials

The Foundation Series offers the following interactive tutorials to help you get up to speed quickly:

- Interactive Foundation tutorial, which teaches you the basics of Foundation schematic entry, simulation, and HDL text entry tools
- MasterClass Lite multimedia VHDL tutorial (included with BSV and STV packages), which teaches you the VHDL language and coding techniques for synthesis and Xilinx architectures

## **Xilinx Foundation Project Manager**

The Xilinx Foundation Project Manager features these advantages:

- Complete project management
- Support for multiple design entry methods
- Full integration of all software tools, including XACTstep, schematic entry, text entry, and simulation
- Single environment with access to all software tools

## **Multiple Design Entry Support**

The Foundation Series supports the following design entry methods:

- Schematic entry support
- Text entry support for XABEL and VHDL

## **HDL Wizard**

The Foundation Series HDL Wizard supports ABEL-HDL and VHDL, including the following:

- Text templates for cutting and pasting common functions
- Color-coded keywords for ABEL-HDL and VHDL languages
- Automatic highlighting of design language syntax errors

# Chapter 4

## Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 <sup>a</sup>	PC44, VQ64, PC68, PC84, PG84, TQ100	-33, -50, -70, -100, -130
XC2064 <sup>a</sup>	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L <sup>a</sup>	PC84, VQ64, VQ100	-10
XC2064L <sup>a</sup>	VQ64, PC68	-10
XC3020 <sup>a</sup>	PC68, PC84, PG84, CB100, CQ100, PQ100	-50, -70, -100, -125
XC3030 <sup>a</sup>	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 <sup>a</sup>	PC84, PG84, CB100, CQ100, PQ100, TQ100, PG132, PP132	-50, -70, -100, -125
XC3064 <sup>a b</sup>	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 <sup>a b</sup>	PC84, CB164, CQ164, PQ160, PG175, PP175, PQ208	-50, -70, -100, -125
XC3020A	PC68, PC84, PG84, CB100, PQ100	-6, -7
XC3030A	PC44, VQ64, PC68, PC84, PG84, PQ100, VQ100	-6, -7
XC3042A	PC84, PG84, CB100, PQ100, VQ100, PG132, PP132, TQ144	-6, -7
XC3064A <sup>b</sup>	PC84, PG132, PP132, TQ144, PQ160	-6, -7
XC3090A <sup>b</sup>	PC84, CB164, PC84, PG175, PP175, TQ176, PQ160, PQ208	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, VQ100, TQ144	-8

Device	Packages	Speed Grades
XC3064L <sup>b</sup>	PC84, TQ144	-8
XC3090L <sup>b</sup>	PC84, TQ176	-8
XC3120 <sup>a</sup>	PC68, PC84, PG84, CB100, PQ100	-3, -4, -5
XC3130 <sup>a</sup>	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 <sup>a</sup>	PC84, PG84, CB100, PQ100, TQ100, PG132, PP132, TQ144	-3, -4, -5
XC3164 <sup>a b</sup>	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 <sup>a b</sup>	PC84, PQ160, CB164, PG175, PP175, PQ208	-3, -4, -5
XC3195 <sup>a b</sup>	PC84, PQ160, CB164, PG175, PP175, PQ208, PG223	-3, -4, -5
XC3120A	PC68, PC84, PG84, CB100, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, VQ64, PC68, PC84, PG84, PQ100, VQ100	-1, -2, -3, -4, -5
XC3142A	PC84, PG84, CB100, PQ100, VQ100, PG132, PP132, TQ144	-1, -2, -3, -4, -5
XC3164A <sup>b</sup>	PC84, PG132, PP132, TQ144, PQ160	-1, -2, -3, -4, -5
XC3190A <sup>b</sup>	PC84, PQ160, CB164, PG175, PP175, TQ176, PQ208	-1, -2, -3, -4, -5
XC3195A <sup>b</sup>	PC84, PQ160, CB164, PG175, PP175, PQ208, PG223	-1, -2, -3, -4, -5
XC4003	PC84, P100, PG120	-4, -5, -6
XC4005 <sup>b</sup>	PC84, PQ100, PG156, PQ160, CB164, PQ208	-4, -5, -6, -6B, -10
XC4006 <sup>b</sup>	PC84, PG156, PQ160, PQ208	-4, -5, -6
XC4008 <sup>b</sup>	PC84, PQ160, PG191, MQ208, PQ208	-4, -5, -6
XC4010 <sup>b</sup>	PC84, PQ160, PG191, CB196, MQ208, PQ208, BG225	-4, -5, -6, -10
XC4013 <sup>b</sup>	PQ160, MQ208, PQ208, PG223, BG225, CB228, PQ240, MQ240	-4, -5, -6, -10
XC4002A	PC84, PQ100, VQ100, PG120	-5, -6
XC4003A	PC84, CB100, PQ100, VQ100, PG120	-4, -5, -6, -10
XC4004A <sup>b</sup>	PC84, PG120, TQ144, PQ160,	-5, -6
XC4005A <sup>b</sup>	PC84, TQ144, PG156, PQ160, PQ208, BG225	-4, -5, -6
XC4010D <sup>b</sup>	PC84, PQ160, PQ208	-5, -6
XC4013D <sup>b</sup>	PQ160, PQ208, BG225, PQ240	-5, -6
XC4003E	PC84, PQ100, VQ100	-3, -4
XC4005E <sup>b</sup>	PC84, PQ100, TQ144, PQ160, CB164, PQ208	-3, -4

Device	Packages	Speed Grades
XC4006E <sup>b</sup>	PC84, PG156, PQ160, PQ208, TQ144	-3, -4
XC4008E <sup>b</sup>	PC84, PQ160, PG191, PQ208	-3, -4
XC4010E <sup>b</sup>	PC84, PQ160, PG191, CB196, PQ208, BG225	-3, -4
XC4013E <sup>b</sup>	PQ160, PQ208, HQ208, PG223, CB228, BG225, PQ240, HQ240	-3, -4
XC4020E <sup>b</sup>	HQ208, PG223, HQ240	-3, -4
XC4003H	PG191, PQ208	-5, -6
XC4005H <sup>b</sup>	PG223, MQ240, PQ240	-5, -6
XC5202	PC84, PQ100, VQ100, TQ144, PG156,	-5, -6
XC5204	PC84, PQ100, VQ100, TQ144, PG156, PQ160,	-5, -6
XC5206 <sup>b</sup>	PC84, PQ100, VQ100, TQ144, PQ160, PG191, PQ208	-5, -6
XC5210 <sup>b</sup>	PC84, TQ144, PQ160, PG223, PQ208, BG225, PQ240	-5, -6
XC5215 <sup>b</sup>	HQ208, HQ240, PG299, HQ304	-5, -6
XC7236A <sup>a</sup>	PC44	-16, -20, -25
XC7318 <sup>a</sup>	PC44, PQ44	-5, -7
XC7336 <sup>a</sup>	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 <sup>a</sup>	PC44, PC68	-7, -10, -12, -15
XC7372 <sup>a</sup>	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q <sup>a</sup>	PC44, PQ44, VQ44	-10, -12, -15
XC73108 <sup>a</sup>	PC84, PQ100, PG144, PQ100, PQ160, BG225	-7, -10, -12, -15, -20
XC73144 <sup>a</sup>	PQ160, BG225	-7, -10, -12, -15
XC8100 <sup>c</sup>	PC44, VQ44	-1
XC8101 <sup>c</sup>	PC84, PQ100	-1
XC8103 <sup>c</sup>	PC84, PQ100	-1
XC8106 <sup>c</sup>	PC84, PQ100	-1
XC8109 <sup>b,c</sup>	PC84, PQ160, BG225	-1

a. Not Supported in X-BLOX

b. Not supported in Base Packages

c. XC8100 schematic libraries are included with the Foundation CD. Please complete and fax or mail the enclosed registration card to receive the XC8100 place and route software at no additional charge.



## Known Issues

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This chapter describes the known issues in this release.

### Software

This section lists the work arounds for the software. They are presented in the order that they occur in the design process.

#### Software Configuration

##### **Library Access Errors Occur When Using Software on a Network**

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

You must place the Read Only attribute on libraries that are on a network and used simultaneously by multiple users, or you must protect the entire library directory with the Read Only attribute.

Libraries that are on a local drive or are only accessed by a single user do not require this protection.

## Changing Default Title Block Information

Platform: PC  
Architecture: All  
Design Step: Software Configuration  
Reference Number: 28216

The default schematic title block (displayed in the lower right-hand corner of each schematic page) contains Aldec company information.

To change this information to reflect your company, add the following lines to the c:\windows\susie.ini file:

```
[sc_config]
Firm Name=your_company_name
Table Data 1=address_or_other_text
Table Data 2=address_or_other_text
```

## Design Entry

### Pins on Memory Symbol Are Not in Numerical Order

Platform: PC  
Architecture: XC4000/A/D/E/H  
Design Step: Design Entry  
Reference Number: 29001

Symbols created by the memory generator have pins in alphabetical order (D1, D10, D2, ... D9) instead of numerical order (D1, D2, ... D9, D10).

Check the Use Bus Pins check box to create a bus pin instead of individual pins.

### Warnings about Empty Symbols During Viewlogic Import

Platform: PC  
Architecture: XC4000/A/D/E/H  
Design Step: Design Entry  
Reference Number: 28984

While importing a Viewlogic schematic, messages about empty symbols may appear. If a symbol is attached to a MEM file, Foundation does not run MemGen to generate an XNF file, resulting in an empty symbol.



After importing the schematic, select **Applications** → **Memory Generator** in the Project Manager. Click on Select and select the MEM file. In the Block field, enter the symbol name (usually the same as the name of the MEM file). Check the Use Bus Pins check box if you want a bus pin, and click Generate to create the XNF file. The software issues a warning that the symbol already exists. This is the old, empty symbol. You can safely overwrite it.

## **HDL Editor Will Not Start**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 28234

If there are not enough Windows resources available when you invoke the HDL Editor, the Editor will not start. No messages appear in the Project Manager window.

Close other applications and invoke the HDL Editor again. You may need to exit Windows and restart it to free the Windows resources.

## **Some Buses Are Renamed during Viewlogic Import**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 28147

Xilinx Foundation Series bus names cannot contain characters after the indexes. Viewlogic schematics containing bus names such as DATA[7:0]\_O are renamed to DATA\_O[7:0]. This information is reported in the Foundation Project Manager window and is also recorded in the Viewlogic Import report, vlexport.log.

## **Do Not Instantiate I/O Buffers in a VHDL Design**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 28253

When you compile a VHDL design as a chip, the synthesizer automatically inserts I/O buffers on all top-level entity ports. If you instantiate a special-purpose I/O buffer in your design like a BUFG,

the synthesizer inserts an IBUF in front of it, producing an invalid netlist. Instantiating I/O buffers and compiling the design as a macro also produces invalid results.

To specify a BUFG on the MY\_CLOCK port, use the Metamor Xilinx\_BUFG attribute, for example:

```
attribute Xilinx_BUFG : boolean;  
attribute Xilinx_BUFG of MY_CLOCK : signal is true;
```

To specify an XC7000 BUFFOE (fast output enable) on the MY\_FOE port, use the following syntax:

```
attribute Xilinx_BUFG: boolean;  
attribute Xilinx_BUFG of MY_FOE : signal is true;  
attribute property : string;  
attribute property of MY_FOE : signal is  
"SCHNM=BUFFOE";
```

To specify other special-purpose I/O buffers, registers, or latches, compile the design as a macro, instantiate its symbol into a schematic, and use the schematic editor to add all the I/O components.

## Creating XABEL Macro Symbols with Bus Pins

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 28030

The Foundation Schematic Editor normally writes bus signals into the netlist as BUS<0>, BUS<1>, and so forth. However, XABEL writes bus signals as BUS0, BUS1, and so forth.

To make sure that the signal names match, declare the bus in the XABEL code with the following syntax:

```
BUS0...BUS7 pin;
```

Then add the \$DEF=XABEL attribute to the macro symbol on the schematic to cause the Foundation software to remove the angle brackets.

## Translation to XNF

### Flip-Flop Signal Names May Change after VHDL Compilation

Platform: PC  
Architecture: All  
Design Step: Translation to XNF  
Reference Number: 28254

In general, the VHDL compiler preserves the names of signals driven by flip-flops. Preserving these names allows you to refer to flip-flop output signals when defining timing specifications and provides easy access to signals during simulation.

If an instantiated component has no entity defined, such as a Xilinx library component, all signals connected to that component are renamed.

## Implementation

### XACTstep Project Manager Error: Cannot Find Data File “xc9500.bos” in the XACT Path

Platform: PC  
Architecture: All  
Design Step: Implementation  
Reference Number: Not Available

The XC9500 fitters are installed into a separate directory than the XC7300 fitters and the FPGA place and route tools. The XACTstep variable should only point to one of these directories. If XACTstep variable is set to the wrong directory, the above error is displayed.

Exit Windows, set the XACTstep variable to point to the appropriate directory and restart Windows.

### XNFPrep Error 3520: Invalid Primitives in Design

Platform: PC  
Architecture: All  
Design Step: Implementation  
Reference Number: Not Available

XNFPrep may issue error 3520 on designs that were created for one Xilinx family but applied to a different Xilinx family. The Xilinx Foundation Series schematic capture tool automatically adds libraries to the project if components are not found in the current project libraries. It may create a schematic containing components from multiple libraries.

To prevent this situation, select the **View → Preferences → General** command. In the dialog box, deselect the **Add Libraries to Project** check box. Exit the schematic editor and restart. When the design is loaded, a message is reported for each part not found in the current library. These symbols must be replaced with the closest equivalent from the current Xilinx library.

### **Series 8000 Software Not Included**

Platform: PC  
Architecture: XC8100  
Design Step: Implementation  
Reference Number: N/A

XC8100 simulation libraries and the XC8100 place and route software were not available when this package shipped but they will be completed within one month. Please send in your registration card in order to receive a free update of the XC8100 simulation library and back-end software.

### **Simulation Application Error - SIMUL Caused a Page Fault**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 28990

A page fault can occur if there is not enough space available on the hard disk. Increase available hard disk space.

## **New Macros Not Listed in Run/Edit Macro File Windows**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 28914

Newly created macro files are not listed when **Utilities** → **Macro** → **Run** or **Utilities** → **Macro** → **Edit** are selected.

Click on the Browse button to select the new macro file. It will be added to the list.

## **Error: Signal Is Already Assigned to a Vector - Ignored**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 28971

If a signal is listed in multiple vector commands in a macro file, the simulator issues the above error. When using macro files, make sure each signal is only referenced in one vector command.

## **Cannot Place Simulation Probes on X-BLOX Buses in Schematic**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 27260

Simulation probes cannot be placed onto X-BLOX buses from the schematic editor.

To view simulation values on X-BLOX buses, add the signals to the waveform viewer from the simulator.

## Documentation

### Selecting ABEL Reference or Metamor Reference Gives “Cannot Open Help File”

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 29232

From the HDL Editor, selecting **Help** → **Help Topics**, and selecting ABEL Reference or Metamor Reference may result in a Windows Help Error: “Cannot open Help file”.

This happens if the current project resides on a different drive than the Foundation software. It also occurs if the Foundation software is installed in a directory other than \ACTIVE.

Use the **File** → **Open** command to open the help files. The ABEL reference is in *Install\_Directory*\EXE\ABEL.HLP. The Metamor Reference is in *Install\_Directory*\EXE\VHDL\_MUG.HLP.

# Xilinx Customer Support Information

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## Technical Support

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