



Release Document

XACT^{step} Version 5.2/6.0
OrCAD

October 1995

Read This Before Installation

XACT 6.0 Install for Windows

The following information supersedes the instructions in the *Getting Started & Installation Guide* for installing XACTstep 6.0 software on PCs running Microsoft Windows. These steps minimize XACTstep 6.0 problems caused by PC resource issues and Microsoft Windows configurations that are not optimal.

Note: After installation is complete, the install program will present you with required environment variable settings for your autoexec.bat program. In some cases this may include multiple paths to the PROSeries tools. The duplicate entry will not prevent the software from running, and can be deleted.

For complete configuration instructions, please see the “Setting Up the Xilinx Environment” chapter of the *Getting Started & Installation Guide*.

1. Before starting the XACTstep 6.0 installation process, Xilinx recommends that you make backup copies of the win.ini and system.ini files located in your Windows directory.
2. Before starting Windows, run a batch file called rmwin32s.bat in DOS to remove any previous version of the Microsoft WIN32S driver that may be installed on your PC.

The latest version (v1.25.142.0) is necessary for use with XACTstep 6.0 and is compatible with all previous versions. If you are not sure if WIN32S is installed on your PC, you can still run this program. If the driver is not installed, rmwin32s.bat tries to delete certain files and then reports that these files could not be found.

To run `rmwin32s.bat`, first identify the CD-ROM drive letter, for example, `D:\`.

From the DOS command prompt, type the following:

```
d:\xbbs\utils\rmwin32s.bat
```

If the WIN32S driver is found, all associated files are removed from your system, and you are prompted to manually remove `winmm16.dll` and `device=...W32S.386` from your `system.ini` file.

3. Next, start Microsoft Windows.
4. In Windows, select **File** → **Run** from the Program Manager.
5. In the command line box, type the following:

```
d:\win32s\disk1\setup.exe
```

This step installs the latest version of the Microsoft WIN32S driver needed for XACTstep 6.0 applications.

6. Select **File** → **Run** from the Program Manager.
7. In the command line box, type the following:

```
d:\xbbs\utils\xinfo\xinfo.exe
```

XINFO is a Xilinx utility that analyzes your computer's system resources for compatibility with the XACTstep software. Review the "Hints" page for suggestions on changes that you should make to your PC configuration to allow XACTstep 6.0 to run more efficiently on your PC.

8. Select **File** → **Run** from the Program Manager.
9. To begin the installation of the XACTstep 6.0 toolset, type the following in the command line box:

```
d:\setup.exe
```

Note: Preliminary calculations of disk space requirements may be inaccurate, depending on how your hard disk is formatted. To identify required disk space accurately, the Install program must calculate disk space on the basis of the selected products list. Using Custom Install, you can correctly calculate the required disk space by turning on the Analyze Disk Space option after making your selections. Using Quick Install, simply continuing the installation process by selecting the Install button correctly calculates the available disk space.

10. After installation is complete, exit from Windows.

11. Using a text editor, load c:\autoexec.bat.

Certain *XACTstep* tools require that the temporary variable be set. If you do not see a line such as “set temp=c:\temp” in your autoexec.bat file, add it to this file. (The location of the temporary directory is not important; only the existence of the variable and a valid path are important.)

12. Next, reboot your PC to ensure that all environment variables have been set correctly.

Refer to the *Getting Started & Installation Guide* for information on other topics, such as environment variables and disk space requirements.

Versions and Compatibility

The following master table indicates Xilinx core software with the current version numbers.

Software Versions

Program	Windows Version	DOS Version	Workstation Version
APR	5.2	5.2	5.2
APRLOOP	5.2	5.2	5.2
CstCvt	5.2	5.2	5.2
Design Manager	6.0	N/A	N/A
Floorplanner	6.0	N/A	5.2
Flow Engine	6.0	N/A	N/A
Hardware Debugger	6.0	N/A	N/A
HM2RPM	5.2	5.2	5.2
LCA2XNF	5.2	5.2	5.2
MakeBits	5.2	5.2	5.2
MakePROM	5.2	5.2	5.2
MAP2LCA	5.2	5.2	5.2
MemGen	5.2	5.2	5.2
PPR	5.2	5.2	5.2
PROM File Formatter	6.0	N/A	N/A
Report Browser	6.0	N/A	N/A
SymGen	5.2	5.2	5.2
Timing Analyzer	6.0	N/A	N/A

Program	Windows Version	DOS Version	Workstation Version
XACT	5.2	5.2	5.2
XBLOX	5.2	5.2	5.2
XChecker	5.2	5.2	5.2
XCK88	N/A	5.2	N/A
XDE	5.2	5.2	5.2
XDelay	5.2	5.2	5.2
XDM	N/A	N/A	5.2
xdm	5.2	5.2	5.2
XEMake	N/A	N/A	5.2
XEMake6	6.0	N/A	N/A
XKey	5.2	5.2	N/A
XMake	5.2	5.2	5.2
XNFBA	5.2	5.2	5.2
XNFCvt	5.2	5.2	5.2
XNFMAP	5.2	5.2	5.2
XNFMerge	5.2	5.2	5.2
XNFPrep	5.2	5.2	5.2
XPP	5.2	5.2	5.2
XPrint	5.2	5.2	5.2
XSimMake	5.2	5.2	5.2

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Introduction

Welcome to the OrCAD Interface from Xilinx!

Xilinx software products have prefixes to designate the type of products you receive.

- DS = Development System (new system)
- DX = Development System Upgrade (upgrade to current system)
- SC = Support Contract (update to current system)
- SR = Support Reinstatement (update for non-current system)
- BU = Base Update (update to current system)

The labels on the box indicate the product you have received.

This release note supports the following products.

- OrCAD Interface and Libraries (DS-35)
- OrCAD Base Development System (DS-OR-BAS)
- OrCAD Standard Development System (DS-OR-STD)

Contents

The Development System (DS) product you received contains software, documentation, and/or hardware. New DS Base and Standard packages contain hardware, software, and documentation. Interface and Update products have software and documentation only.

Hardware¹

The hardware consists of the following items.

- XChecker Download and Readback Cable Set (included in STD packages)
- Parallel Download Cable (included in BASE packages)
- Xilinx “C” Programmable Key (a beige key, included in STD PC packages)

Software

Xilinx software for all platforms is provided on CD-ROM. It consists of the following.

- Installation Program
- FPGA Core Implementation Tools (DS-502 and STD packages only)
- FPGA Base Implementation Tools (included in DS-OR-BAS only)
- XEPLD Translator Core Tools (DS-550)
- ORCAD Interfaces and Libraries (DS-35)
- X-BLOX (DS-380 included in STD packages only)

Documentation

The following documentation is available in print for OrCAD products.

- *Getting Started & Installation Guide*
- *Additional Products & Services Packet*
- *OrCAD Interface/Tutorial Guide*²

1. Included in DS packages only.

2. Included in DS, SR, and BU products only.

Online Documentation

The following online documentation is included with your OrCAD products.

- *Libraries Guide*
- *Libraries Supplement Guide*
- *X-BLOX Reference/User Guide*
- *Floorplanner Reference/User Guide*
- *Design Manager/Flow Engine Reference/User Guide*
- *Timing Analyzer Reference/User Guide*
- *Hardware Debugger Reference/User Guide*
- *PROM File Formatter Reference/User Guide*
- *Development System User Guide*
- *Development System Reference Guide, Vols 1-3*
- *Hardware & Peripherals User Guide*
- *XEPLD Reference Guide (for Windows)*
- *XEPLD Schematic Design Guide (for Windows)*

Note: Xilinx Core FPGA and EPLD documentation for Sun and PC platforms is available online via CD-ROM. Some documentation for product updates and for other workstation platforms is included on the basis of product configuration.

Selected Xilinx manuals are available in printed form. See the “Documentation Order Form” in the *Additional Products & Services Packet*.

Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with one year of maintenance¹; you will receive all software and documentation updates automatically during that time. You will receive a notice at the end of the year giving instructions on how to renew your maintenance contract.

1. Not included with DS-OR-BAS.

Chapter 2

Features in This Release

The following features are enhancements supported in the XACTstep 5.2/6.0 release.

OrCAD SDT and VST V1.2

The existing version of the OrCAD schematic editor and simulator, SDT and VST Version 1.2, is provided with enhanced library support.

Library Support

The XACTstep 6.0 CD-ROM includes libraries that have been compiled to support Version 1.2 of SDT and VST, the latest DOS version of the OrCAD software. Also available on the XACTstep 6.0 CD-ROM are the uncompiled libraries. These libraries allow you to easily compile the Xilinx libraries to any version of the OrCAD software tools. They can be found in XBBS\SWHELP\ORCSRC.ZIP.

Interface and Libraries

The following changes have been made to the interface and libraries for this release.

Library Support for XC5200

New schematic library is available to support the XC5200 device family. For more information on this family, see *The Programmable Logic Data Book*.

XNF Version 6 Support

The translation program SDT2XNF has been updated to support the latest version of the XNF file, Version 6. This version of the XNF file supports the new XC5200 Xilinx product family.

X-BLOX Support

This section discusses new and upgraded X-BLOX features. X-BLOX supports the XC5200 device family for all platforms.

Increased Clock-to-Clock Performance

This section describes changed criteria for merging flip-flops into IOBs.

Platform: All

Architecture: XC4000A/D, XC3000A/L, XC3100A

The default criteria for merging registers into IOBs have changed to improve CLOCK to CLOCK performance. If you do not specify otherwise, X-BLOX pushes a flip-flop into an IOB where it improves the CLOCK to OUT performance according to the following rules.

- X-BLOX merges a flip-flop into an OUTFF in an IOB if one or both of the following conditions apply.
 - The flip-flop D pin is sourced (either directly or indirectly) by *non-combinational* logic. The indirect case occurs where one or more buffers and/or inverters, and no other logic, are found between the non-combinational source and the D pin.
 - The source X-BLOX symbol (if the flip-flop was generated from an X-BLOX symbol) has a parameter that indicates it should be implemented in an IOB, for example, STYLE=IOB.
- Criteria for merging flip-flops into INFFs in an IOB have not changed.

Note: In a design compiled with a previous version of X-BLOX, the clock-to-clock timing might be faster if STYLE is not specified. However, in some cases the clock-to-pad speed might be slower. If clock-to-pad speed is critical in your design, use registers in the IOB. For example, use the STYLE=IOB or STYLE=-OFD definitions for DATA_REG.

Reduced Memory Usage

For all platforms and architectures, memory saving enhancements made to the X-BLOX functional simulation mode lead to significant reductions in memory usage, by as much as 50 percent for certain styles of designs.

X-BLOX Reference/User Guide Changes

The following modules have changed to support the XC5200 architecture. Modules which are not included are valid as described in the *X-BLOX Reference/User Guide*. The XC5200 attribute information in this section will be incorporated in the next revision of the *X-BLOX Reference/User Guide*.

ACCUM

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

ADD_SUB

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

ANDBUS

Attribute: STYLE is not supported.

BIDIR_IO

Attribute: NODELAY attribute can now be attached.

COMPARE

Attribute: STYLE may be set to ARITH, TREE, or RIPPLE.
STYLE=WIRED is not supported.

DATA_REG

Attribute:
STYLE=FD is added for implementation using CLB flip-flops.
STYLE=LD is added for implementation using CLB latches.

STYLE=CLB is not supported, use STYLE=FD or STYLE=LD.

STYLE=IOB is not supported.

STYLE=ILD is not supported.

STYLE=IFD is not supported.

STYLE=OFD is not supported.

Note: For XC3000 and 4000 designs, the NODELAY attribute can be added to the DATA_REG symbol. For XC5200 designs, attach the NODELAY attribute to either the INPUTS or BIDIR_IO symbols.

INC_DEC

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

INPUTS

Attribute: The NODELAY attribute can now be attached.

SHIFT

Attributes: remain unaffected.

TRISTATE

Attribute: FLOAT_VAL is not supported.

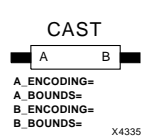
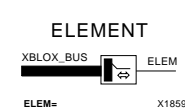
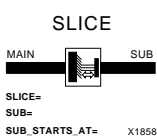
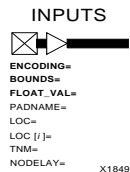
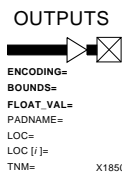
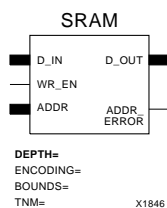
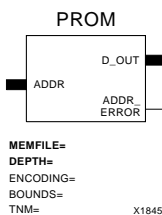
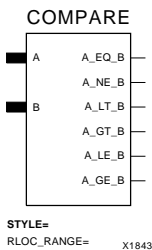
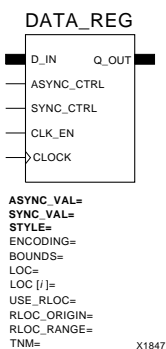
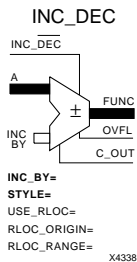
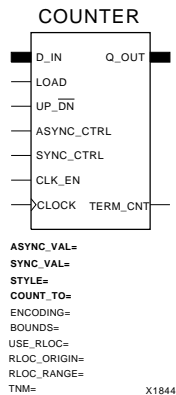
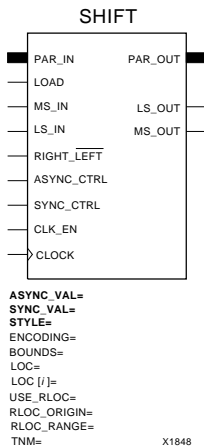
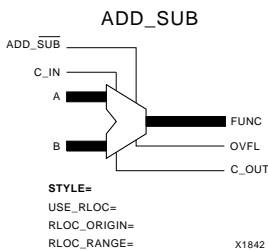
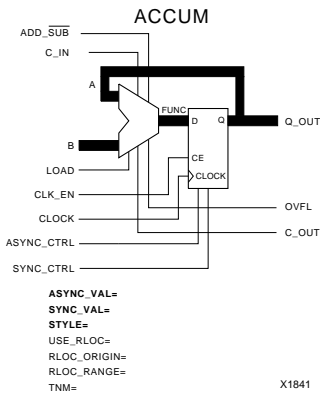
SRAM

The SRAM symbol is not supported for XC5200.

Summary of X-BLOX Symbols

Attributes that appear on schematic symbols are in bold type.

Optional attributes appear in plain text. The X-BLOX symbols that are not displayed are valid as shown on the X-BLOX Symbols Reference Card.





Chapter 3

Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 ^a	PC44, PC68, PC84, PG84, TQ100, VQ64	-33, -50, -70, -100, -130
XC2064 ^a	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L ^a	PC84, VQ64, VQ100	-10
XC2064L ^a	PC68, VQ64	-10
XC3020 ^a	CB100, CQ100, PC68, PC84, PG84, PQ100	-50, -70, -100, -125
XC3030 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 ^a	CB100, CQ100, PC84, PG84, PG132, PP132, PQ100, TQ100	-50, -70, -100, -125
XC3064 ^{a b}	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 ^{a b}	CB164, CQ164, PC84, PG175, PP175, PQ160, PQ208	-50, -70, -100, -125
XC3020A	CB100, PC68, PC84, PG84, PQ100	-6, -7
XC3030A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-6, -7
XC3042A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-6, -7
XC3064A ^b	PC84, PG132, PP132, PQ160, TQ144	-6, -7
XC3090A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, TQ144, VQ100	-8
XC3064L ^b	PC84, TQ144	-8

Device	Packages	Speed Grades
XC3090L ^b	PC84, TQ176	-8
XC3120 ^a	CB100, PC68, PC84, PG84, PQ100	-3, -4, -5
XC3130 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 ^a	CB100, PC84, PG84, PG132, PP132, PQ100, TQ100, TQ144	-3, -4, -5
XC3164 ^{a b}	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 ^{a b}	CB164, PC84, PG175, PP175, PQ160, PQ208	-3, -4, -5
XC3195 ^{a b}	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-3, -4, -5
XC3120A	CB100, PC68, PC84, PG84, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-1, -2, -3, -4, -5
XC3142A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-1, -2, -3, -4, -5
XC3164A ^b	PC84, PG132, PP132, PQ160, TQ144	-1, -2, -3, -4, -5
XC3190A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-1, -2, -3, -4, -5
XC3195A ^b	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-1, -2, -3, -4, -5
XC4003	PC84, PG120, PQ100	-4, -5, -6
XC4005 ^b	CB164, PC84, PG156, PQ100, PQ160, PQ208	-3, -4, -5, -6, -6B, -10
XC4006 ^b	PC84, PG156, PQ160, PQ208	-3, -4, -5, -6
XC4008 ^b	MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6
XC4010 ^b	BG225, CB196, MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6, -10
XC4013 ^b	BG225, CB228, MQ208, MQ240, PG223, PQ160, PQ208, PQ240	-3, -4, -5, -6, -10
XC4002A	PC84, PG120, PQ100, VQ100	-5, -6
XC4003A	CB100, PC84, PG120, PQ100, VQ100	-4, -5, -6, -10
XC4004A ^b	PC84, PG120, PQ160, TQ144	-5, -6
XC4005A ^b	PC84, PG156, PQ160, PQ208, TQ144	-4, -5, -6
XC4010D ^b	BG225, PC84, PQ160, PQ208	-5, -6
XC4013D ^b	BG225, PQ160, PQ208, PQ240	-5, -6
XC4003H	PG191, PQ208	-5, -6
XC4005H ^b	MQ240, PG223, PQ240	-5, -6
XC5202	PC84, PG156, PQ100, TQ144, VQ100	-5, -6

Device	Packages	Speed Grades
XC5204	PC84, PG156, PQ100, PQ160, TQ144, VQ100	-5, -6
XC5206 ^b	PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100	-5, -6
XC5210 ^b	BG225, PC84, PG223, PQ160, PQ208, PQ240, TQ144	-5, -6
XC5215 ^b	HQ304, PG299, PQ208, PQ240	-5, -6
XC7236A ^a	PC44	-16, -20, -25
XC7318 ^a	PC44, PQ44	-5, -7
XC7336 ^a	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 ^a	PC44, PC68	-7, -10, -12, -15
XC7372 ^a	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q ^a	PC44, PQ44, VQ44	-10, -12, -15
XC73108 ^a	BG225, PC84, PG144, PQ100, PQ160	-7, -10, -12, -15, -20
XC73144 ^a	BG225, PQ160	-7, -10, -12, -15

a. Not supported in X-BLOX.

b. Not supported in Base packages.

Known Issues

This chapter describes the known issues in this release.

Software

Installation

Use New VSTLIB for Old Library Designs

Platform: PC

Architecture: All

Design Step: Installation

Reference Number: Not Available

V5.0 of the OrCAD Interface includes a new version of the VSTLIB simulation directory. This simulation directory contains new simulation models for the V4.x (pre-Unified) library symbols. To simulate a design created with the V4.x libraries using the V5.0 interface, you must reference the new VSTLIB directory in your vst.cfg file. The simulation models in the V4.x VSTLIB directory do not support simulation of carry logic.

Software Configuration

Reduce Conventional Memory Usage During Design Translation

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

To reduce the amount of conventional memory used during design translation, Xilinx recommends that you reconfigure the Annotate and Inet programs using Phar Lap's `cfg386` utility program, shipped by OrCAD. The `cfg386.exe` utility is located in the ORCADEXE directory along with all the other OrCAD executables.

To reconfigure the programs, follow these steps:

1. Make a backup of the original Annotate and Inet programs in case you need to restore them.
2. Go to the ORCADEXE directory.
3. To reconfigure the Annotate program and reduce its conventional memory requirement by 64 K, type the following:

```
cfg386 annotate -callb 0
```

4. To reconfigure Inet and reduce its conventional memory requirement by 64 K, type the following:

```
cfg386 inet -callb 0
```

By reducing the amount of conventional memory used during design translation, you also reduce the chance of having the Design Manager crash during the design translation process due to insufficient free conventional memory.

OrCAD Might Not Appear in XDM Menu

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

You might find that OrCAD does not appear in your XDM Design Entry menu.

If OrCAD does not appear in the menu, check the AUTOEXEC.BAT file. Verify that the ORCADEXE directory appears in your path, with the correct drive designator. If the ORCADEXE directory is in your search path, but OrCAD does not appear in the Design Entry menu, XDM might not know where to look for it. Select Utilities → Scandisk from the XDM menus; XDM scans your system for supported software.

Always Run XDrafter to Configure SDT and VST

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

The XDrafter program configures your sdt.cfg and vst.cfg files for Xilinx designs. Running XDrafter should always be your first step after creating a new design directory.

To run XDrafter, cd to the design directory and type `xdrafter n-l`, where n is one of 2, 3, 4, 5, or 7, to configure for the designated product family.

XDrafter Configures SDT for New “O” Libraries

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

In addition to one of the Unified Libraries, XC2000, XC3000, XC4000, or XC7000, XDrafter places a library called XC2000O, XC3000O, XC4000O, or XC7000O in your library search path.

These libraries contain symbols with the same names as old library elements that no longer exist in the new Unified Libraries. When you attempt to place one of these components, a symbol appears warning you not to use the element. Most of these obsolete elements have equivalent symbols with different names in the Unified Libraries. Refer to the *Libraries Guide* for tables showing the names of equivalent elements for obsolete components.

You can remove this library from your search path if you wish.

To Use Old Libraries, Copy to New Interface Directory Before Running XDrafft

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: 16885

The XDrafft program configures your sdt.cfg and vst.cfg files for Xilinx designs. The -l option (lowercase L) specifies that the old (pre-Unified) libraries be used. XDrafft -l works properly only if the old library directories, SDT2, SDT3, SDT4, and/or SDT7, are located in a directory containing the OrCAD interface executables sdt2xnf.exe, xnf2vst.exe, and xdrafft.exe. If these executables are not present, the following message appears:

```
*** DS35-XCFG-ERROR-003: The XACT path
*** 'xact_path' is not set up properly or the
*** Xilinx DS35 OrCAD interface is not installed
*** in the XACT path.
```

The simplest solution is to copy the old libraries into the new interface area before running XDrafft. The executables are then present, XDrafft functions properly, and as a bonus all of your OrCAD interface software is in one convenient location.

Use -L Option to Configure for Old Libraries

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

By default, XDrafft now configures your project directory to use the Unified Libraries.

To use the OrCAD V4.x libraries (x4k.lib, x3k.lib, x2k.lib or xepld.lib), run XDrafft with the -l option (lowercase L).

XDrafter Overwrites User Macro Specifications in Sdt.cfg File

Platform: PC
Architecture: All
Design Step: Software Configuration
Reference Number: Not Available

XDrafter edits your sdt.cfg file to use the Xilinx-supplied macro file, macro3.mac, and inserts DIM='I' as the initial macro.

If you wish to use your own macro file, edit sdt.cfg to modify the macro name and remove the initial macro line.

OrCAD Local Configuration Might Run Out of Memory Under XDM

Platform: PC
Architecture: All
Design Step: Software Configuration
Reference Number: Not Available

OrCAD's configuration programs are memory intensive. If you call OrCAD from XDM and then attempt to perform a local configuration, you might receive the message Could not find the .EXE, or not enough memory to load \orcadexe\SDT_CLC.EXE or VST_CLC.EXE.

If this message appears, exit OrCAD and XDM, then invoke OrCAD directly from the DOS prompt. The additional base memory released by XDM should be sufficient to allow local configuration.

SDT2XNF Looks for Xilinx Libraries in XACT Directory

Platform: PC
Architecture: All
Design Step: Software Configuration
Reference Number: Not Available

SDT2XNF V5.0 looks in the XACT directory, as defined by the XACT environment variable, to find the Xilinx libraries. If multiple directories are specified in the XACT variable, all are checked. SDT2XNF does not at any time check the OrCAD configuration file, sdt.cfg, to determine the value of PLIB, or look in the PLIB directory for the libraries.

Do not move the Xilinx libraries from the XACT directory in which they are placed by the Install program, or, if you must move them, add the new location to the definition of the XACT environment variable. Specify multiple XACT directories using the syntax shown in the following example:

```
SET XACT=C:\XACT;D:\XACT;E:\XLIBS
```

Only OrCAD 386+ Is Supported

Platform: PC
Architecture: All
Design Step: Software Configuration
Reference Number: Not Available

The Unified Libraries are only available in OrCAD 386+ format. With this release, you may continue to use the old OrCAD V4.x libraries provided in earlier versions of this software, or the OrCAD 386+ versions of these older libraries.

Design Entry

Limited Capture Support

Platform: PC
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

Capture, OrCAD's Windows schematic entry tool, is supported by mimicking the OrCAD 386+ feature set. This path also requires two executables available from OrCAD. For more information on how to use the Capture tool with the Xilinx interface, see XDOCS #26121 or contact the Xilinx technical Support hotline at 1 (800) 255-7778.

Using the Old Libraries with the V5.x Interface

Platform: PC

Architecture: XC4000/A/D/H, XC3100/A, XC3000/A/L, XC2000/L

Design Step: Design Entry

Reference Number: Not Available

You may have existing designs that use the V4.x libraries.

Specify the -l option (lowercase L) to XDrafter and XMake, and the -o option (lowercase O) to XSimMake, to process your OrCAD V4.x design. Refer to the *OrCAD Interface/Tutorial Guide* for more detailed instructions if necessary.

OSC5 and CK_DIV Macros Are Not Supported for Orcad

Platform: PC

Architecture: XC5200

Design Step: Design Entry

Reference Number: Not Available

The OrCAD schematic entry interface does not support parameterized attributes and is therefore incapable of supporting the OSC5 and CK_DIV macros defined in the *Libraries Guide*.

In order to make use of the internal oscillator in the XC5200 family, you must use the OSC52 primitive in your designs. This primitive provides the capabilities of both the OSC5 and the CK_DIV macros.

To use the OSC52 as a clock divider, that is CK_DIV, ensure that you follow the rules described below:

1. Connect your clock net to the C input pin of the OSC52.
2. Define at least one of the DIVIDE1_BY=n1 and DIVIDE2_BY=n2 attributes, as described in the *Libraries Guide*.
3. Set the OSC= attribute to USER_CLK.

To use the OSC52 to divide the internal oscillator, that is OSC5, be sure to follow the rules described below:

1. Leave the C input pin of the OSC52 unconnected.

2. Define at least one of the DIVIDE1_BY=n1 and DIVIDE2_BY=n2 attributes as described in the *Libraries Guide*.
3. Set the OSC= attribute to INTERNAL.

BUFE Elements Might Require Logic Level for Inversion

Platform: PC

Architecture: XC4000/A/D/H, XC3100/A, and XC3000/A/L

Design Step: Design Entry

Reference Number: 8910, 14336

For convenience, the Unified Libraries include 3-state buffer elements with both active-Low enable (the BUFT elements) and active-High enable (the BUFE elements). The actual 3-state buffers in the XC4000- and XC3000-based architectures have active-Low enables that are not directly invertible. If a BUFE element is sourced by a gate, the inversion of the enable signal is performed at the source and no extra delay is incurred. However, if a BUFE element is sourced by a flip-flop or by another element without a dedicated output inversion, the inversion of the enable signal is implemented in an additional function generator, adding an extra level of delay to the path.

When an inverter cannot be absorbed at the source or load pins, XNFPrep issues a message similar to the following:

```
XNFPREP: WARNING 4037
```

```
These inverters could not be absorbed and each will be  
implemented in a single function generator. This will  
introduce additional delay and use resources  
inefficiently. (Note that some of the symbols listed  
below may have been reduced to inverters by earlier  
trimming.)
```

```
Inverter Name = inverter_name
```

```
Output Signal = signal_name/T
```

The presence of “/T” at the end of the output signal name indicates that the inverter might be part of a BUFE component. If the delay on a 3-state enable path is important, and the enable signal is sourced by a non-invertible output, avoid using a BUFE component if possible.

Translation to XNF

INET Might Drop Attributes from Your Schematic

Platform: PC

Architecture: All

Design Step: Translation to XNF

Reference Number: Not Available

If you have more than one text attribute in your schematic, SDT2XNF might not see some of the attributes. If you check the INF netlist file read by SDT2XNF, the attributes are missing. The reason is that INET V1.10 drops the first line of each text group after the first text group encountered on the schematic. OrCAD is aware of the problem and plans to fix it in a future release. Since the first text group is read correctly, any schematic with only one text group, such as a PART-TYPE attribute, is handled properly.

If you have INET V1.10, place an extra text string above each group of text in your schematic, consisting of a single pipe character (|) aligned with the pipe characters in the rest of the text. INET deletes the first line and retains all of your attribute text.

Pin Numbers on Symbols Cause Internal Program Error

Platform: PC

Architecture: All

Design Step: Translation to XNF

Reference Number: 14809

SDT2XNF issues an internal program error if library symbol pins have an assigned pin number of zero. This is because INET V1.10 drops the pin description in the generated INF file if the library symbol pin has assigned pin number zero, but still produces the pin in the Join statement. This is a known problem in INET V1.10.

To correct the problem, edit the library symbol and change the pin number to any integer greater than zero. Alternatively, you can delete the symbol and re-create it following the procedure detailed in the *OrCAD Interface/Tutorial Guide*. Rerun XMake using the -r option to force re-execution of all programs, or rerun Annotate, INET, and SDT2XNF.

Stimulus and Trace Data on Buses Is Not Supported

Platform: PC
Architecture: All
Design Step: Translation to XNF
Reference Number: 12271

If you place stimulus or trace data on buses, SDT2XNF issues a warning message stating that the data was ignored.

Add bus stimulus using the Test Vector Editor within VST. To place stimulus and trace data in the schematic, break out individual signals from the bus and place stimulus or trace data on the wires.

Label All Nets with Stimulus or Trace Data

Platform: PC
Architecture: All
Design Step: Translation to XNF
Reference Number: Not Available

If you place stimulus or trace data on an unlabeled net, INET treats the stimulus or trace as though it was on the pin instead of the unlabeled net. SDT2XNF issues a warning asking you to label the net to which the stimulus or trace is attached.

Label each net to which you attach stimulus or trace data.

EPLD Designs Using the Old Library

Platform: PC
Architecture: XC7000
Design Step: Translation to XNF
Reference Number: Not Available

If the SDT2XNF translator complains that it cannot find any symbols for an existing design using the old XEPLD V4.x library, check the following:

1. Ensure that the old library file, XEPLD.LIB, is located in the sdt7 directory.
2. Ensure that the XACT environment variable points to the XACT directory containing sdt7.

3. Your SDT configuration should include only the sdt7\Xepld.lib library. You can automatically configure OrCAD to access the XEPLD V4.x library by typing the following.

```
xdraft 7 -L
```

EPLD Designs Use XNF Netlists

Platform: PC

Architecture: XC7000

Design Step: Translation to XNF

Reference Number: Not Available

EPLD schematics are translated to XNF netlist format for design entry using SDT2XNF. Previous versions of XEPLD read only EDIF-formatted netlists.

Implementation

Do Not Use “HM” as Reference Designator Prefix in Unified Libraries Designs

Platform: PC

Architecture: XC4000/A/D/H

Design Step: Implementation

Reference Number: Not Available

If your Unified Libraries design contains any Reference Designator prefix beginning with the characters HM, XNFPrep terminates with an error indicating that the design has a mixture of old and new library elements.

In designs using the old pre-unified libraries, hard macros were identified by reference designators starting with the letters “HM.” Since the V5.0 software still supports designs with the old libraries, “HM” still designates a hard macro, so XNFPrep thinks it is an old library element.

If your Unified Libraries design contains symbols with “HM” reference designators, change them to U? and re-annotate, or use another unique reference designator that does not start with HM.

Simulation

Release Global Reset at Start of Simulation

Platform: PC

Architecture: XC4000/A/D/H, XC3100/A, XC3000/A/L, XC2000/L

Design Step: Simulation

Reference Number: Not Available

When the simulator is initialized, the global reset signals are active. GR is Low for XC3100, XC3000 and XC2000 family designs, and GSR is High for XC4000 family designs. All flip-flop output values are in the Reset state: all XC3000 and XC2000 flip-flop outputs are Low, and XC4000 flip-flops are either High or Low, depending on whether they are Set or Reset flip-flops.

Edit your stimulus file to set GR High or GSR Low after some time interval, such as 100 ns. You cannot place this stimulus in the schematic, as GR and GSR do not appear in the schematics.

Do Not Change Global Reset and Clock Simultaneously

Platform: PC

Architecture: XC4000/A/D/H, XC3100/A, XC3000/A/L, XC2000/L

Design Step: Simulation

Reference Number: Not Available

When any two signals, such as the global reset signal (GR or GSR) and a clock, change at the same time, VST may see either of the two signals as switching first. If your global reset signal goes inactive at the same time that your clock changes, your counters may increment/decrement, or they may not. When you update your OrCAD simulator from VST V4.x to VST 386+, the change in software may change the chance behavior of your design. Test vectors that previously ran without errors may fail due to the change in timing.

Edit your test vectors so the two edges do not change simultaneously.

EPLD Functional Simulation

Platform: PC
Architecture: XC7000
Design Step: Simulation
Reference Number: Not Available

You can represent a 3-state output on an EPLD device by connecting a BUFE or BUFT to an OBUF in the schematic. During functional simulation, however, the OBUF model produces an undefined (U) output when it receives a high-Z input signal. Post-fitting timing simulation conveys the correct 3-state output waveform.

EPLD Functional Simulation Support

Platform: PC
Architecture: XC7000
Design Step: Simulation
Reference Number: Not Available

The new XC7000 EPLD library now supports functional simulation before fitting for completely schematic-based designs. Post-fitting timing simulation is still available for all designs, including those containing equation-based PAL symbols.

V_{CC} and GND Signals in Subsheets

Platform: PC
Architecture: XC7000
Design Step: Simulation
Reference Number: Not Available

Wires labeled V_{CC} or GND are not recognized as global names when XNF netlists are flattened. If V_{CC}/GND labeled wires are used in subsheets (schematics below the top-level), they may be treated as undriven wires causing DRC warnings.

Use the V_{CC} and GND symbols from the Xilinx library to drive a constant High or Low signal.

ROM Outputs Remain Unknown Until Address Changes

Platform: PC
Architecture: XC4000/A/H
Design Step: Simulation
Reference Number: 6301

When simulating an XC4000 design containing ROM elements, the ROM outputs remain unknown until one or more address lines is toggled. This behavior is due to a limitation in the VST simulator.

In your stimulus file, drive the ROM address lines to any value other than the correct initial value, then apply the initial value.

VST386+ Requires Write Permissions on MODEL Files

Platform: PC
Architecture: All
Design Step: Simulation
Reference Number: Not Available

When invoking the OrCAD VST386+ simulator, the following error might occur:

```
Unable to Open Model File
```

The MODEL.DAT and MODEL.NDX files in any of the library directories must actually allow write access before you invoke the OrCAD simulator. The simulator does not change the contents of these library files, but it does update their modification dates.

If you receive this error, remove any read-only attributes from the library model files using the following DOS command:

```
attrib -r \xact\cxxxxx\model.*
```

where \xact\cxxxxx is the path to the Xilinx library for the applicable family.

Simulation File Creation

XSimMake Does Not Use XDM Profile Options

Platform: PC
Architecture: All
Design Step: Simulation File Creation
Reference Number: Not Available

XSimMake does not read the xdm.pro file and always uses the same options for each program for a given flow. Setting options for subprograms in the XDM Profile menu has no effect.

You should not need to use any options other than the defaults when preparing simulation input files. However, if necessary, you can run XSimMake once, then use the xsimmake.log file as a template to create your own batch file.

Always use XSimMake when performing a functional simulation of a Xilinx ABEL or an X-BLOX design.

XSimMake Does Not Support Designs with CLB or IOB Primitives

Platform: PC
Architecture: XC3100/A, XC3000/A/L, XC2000/L
Design Step: Simulation File Creation
Reference Number: Not Available

Neither the functional flow nor the timing flow of XSimMake supports designs containing CLB or IOB primitives.

For information on simulating designs with CLB or IOB primitives, see the “Manual Translation” chapter of the *OrCAD Interface/Tutorial Guide*.

Tie All Control Pins to V_{CC} or GND

Platform: PC
Architecture: All
Design Step: Simulation File Creation
Reference Number: Not Available

When left unconnected, control pins such as CE, CLR, PRE, and R on Xilinx library macros can cause unknown output values during func-

tional simulation. Therefore, XNF2VST issues a warning message when unconnected control pins are encountered.

Tie unused CE pins to V_{CC} , and unused CLR, PRE, and R pins to the inactive values. The logic is later trimmed during the implementation process, so the extra V_{CC} and GND nets do not use any additional routing resources. As a result of this trimming, this problem does not occur during timing simulation.

XNFBA Produces Error When LCA File from Makebits 4.x Is Used as Input

Platform: PC

Architecture: XC4000/A/D/H, XC3100/A, XC3000/A/L, XC2000/L

Design Step: Simulation File Creation

Reference Number: 16848

Prior to XACT 5.0, MakeBits -w was the processing step that incorporated routing delays into a routed LCA file. Beginning with the XACT 5.0 release, XDelay -w performs this function.

If MakeBits V4.x was used to incorporate routing delays, XNFBA V5.0 might issue one or more error messages similar to the following:

```
ERROR 301: Delay 1.5 on PIN 0 of symbol_type
symbol_name is not annotated.
The pin is connected to the signal signal_name.
```

To process LCA files annotated by MakeBits V4.x, run XDelay -w V5.0 prior to running XNFBA.

ASCTOVST 386+ V1.0 Might Run Out of Memory Under XDM

Platform: PC

Architecture: All

Design Step: Simulation File Creation

Reference Number: Not Available

ASCTOVST is a memory-intensive program. If you call ASCTOVST from XDM, it might fail with the error message Insufficient conventional memory for data buffers.

If this message appears, exit XDM. Type `asctovst calc.ast` at the DOS prompt to convert the stimulus file, or `asctovst`

`calc.attr` to convert the trace file. The additional base memory released by XDM should be sufficient to allow ASCTOVST to run.

Documentation

OrCAD Interface/Tutorial Guide

Attributes

Platform: All
Architecture: All
Design Step: Not Available
Reference Number: 10620

The X-BLOX Tutorial in the *OrCAD Interface/Tutorial Guide* only talks about using BUS_DEF to specify the ENCODING and BOUNDS. It should also point out that for the Q_BLX bus, these attributes can be placed on the DATA_REG module as well.

UART Receiver

Platform: All
Architecture: All
Design Step: Not Available
Reference Number: 10589

The description of the tutorial design (an UART receiver) indicates that it operates on data frames consisting of a start bit, 8 data bits (including one parity bit) and two stop bits for a total of 11 bits per frame. The design only has 7 data bits (including one parity bit) for a total of 10 bits per frame. In Session 5 of this chapter, “Simulating the Design,” the waveforms in the text differ slightly from the waveforms in the actual simulation. The tutorials are usable with these problems, but they may cause confusion to novice users.

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