



Release Document

**XACTstep Version 5.2.1/6.0.1
Core Tools
Known Issues, Work Arounds,
and Helpful Hints**

July, 1996

Read This Before Installation

Versions and Compatibility

The following master table indicates Xilinx core software with the current version numbers.

Software Version

Program	Windows Version	DOS Version	Workstation Version
APR	5.2.0	5.2.0	5.2.0
APRLOOP	5.2.0	5.2.0	5.2.0
CstCvt	5.2.1	5.2.1	5.2.1
Design Manager	6.0.1	NA	NA
Floorplanner	6.0.1	NA	5.2.1
Flow Engine	6.0.1	NA	NA
Hardware Debugger	6.0.0	NA	NA
HM2RPM	5.2.1	5.2.1	5.2.1
LCA2XNF	5.2.1	5.2.1	5.2.1
MakeBits	5.2.1	5.2.1	5.2.1
MakePROM	5.2.1	5.2.1	5.2.1
MAP2LCA	5.2.0	5.2.0	5.2.0
MemGen	5.2.1	5.2.1	5.2.1
PPR	5.2.1	5.2.1	5.2.1
PROM File Formatter	6.0.0	NA	NA
Report Browser	6.0.1	NA	NA
SymGen	5.2.1	5.2.1	5.2.1
Timing Analyzer	6.0.0	NA	NA

Program	Windows Version	DOS Version	Workstation Version
XACT	5.2.1	5.2.1	5.2.1
XBLOX	5.2.1	5.2.1	5.2.1
XChecker	5.2.0	5.2.0	5.2.0
XCK88	N/A	5.2.0	N/A
XDE	5.2.1	5.2.1	5.2.1
XDelay	5.2.1	5.2.1	5.2.1
XDM	N/A	N/A	5.2.1
xdm	5.2.1	5.2.1	5.2.1
XEMake	NA	NA	5.2.1
XEMake6	6.0.1	NA	NA
XKey	6.0.0	5.2.1	NA
XMake	5.2.0	5.2.0	5.2.0
XNFBA	5.2.1	5.2.1	5.2.1
XNFCvt	5.2.0	5.2.0	5.2.0
XNFMAP	5.2.0	5.2.0	5.2.0
XNFMerge	5.2.0	5.2.0	5.2.0
XNFPrep	5.2.1	5.2.1	5.2.1
XPP	5.2.0	5.2.0	5.2.0
XPrint	5.2.1	5.2.1	5.2.1
XSimMake	5.2.1	5.2.1	5.2.1
Cadence-Related Beta Versions			
X2Vprep	NA	NA	9504-5.2c
XNF2Verilog	NA	NA	9504-1.30w
funcnetx	NA	NA	5.5.b
timenetx	NA	NA	5.2.1.b

Contents

Software Version.....	iii
Chapter 1 Device and Package Support	
Chapter 2 Known Issues	
Software	2-1
Installation.....	2-1
Installer Indicates that Newer Files Exist on Machine When Installing XACTstep 6.0	2-1
Software Configuration	2-2
Programs Missing from XDM Menus	2-2
The Use of Upper Case Names Is Not Supported.....	2-2
Design Entry	2-3
XDM Appears to Hang When SymGen Is Invoked	2-3
Translation	2-3
Design Manager Doesn't Accept Speeds with Non-numeric Characters.....	2-3
Retranslation of XC7000 Design Does Not Pick Up Design Changes	2-4
XDM Crashes on Saveprofile	2-4
Run XMake with -L Option for Designs Using Non-Unified Libraries	2-4
XMake Requires WIR File Input for Viewlogic Designs	2-5
Implementation	2-5
Unhandled Exception from Design Manager If Network Drive Doesn't Exist	2-5
Small Talk Error: Video Driver out of Memory	2-6
Mouse with Left-handed Settings May Not Work in Design Manager/Flow Engine.....	2-6
Opening Design Manager on Projects Deleted outside Design Manager Gives Unhandled Exception	2-6

XBLOX Counters Can Not Be Larger than 31 Bits Wide	2-7
Opening Design Manager Gives Unhandled Exception: Subscript out of Bounds.....	2-7
Manually Deleting Project Directories and Files Leads to System Errors in the Design Manager.....	2-8
Renaming the Project Generates a System Error	2-8
Specifying a Guide Design in the Design Implementation Dialog When Also Specifying a Guide File Using Flow Engine Advanced Dialog Is Misleading.....	2-9
Clicking On a Report in the Report Browser Generates the Error Message: "The Report File Is Missing"	2-9
Customize Templates Do Not Allow Spaces in Parameters	2-10
PCs With No Math Co-Processor Require a Manual Installation of PPR	2-10
Optimize Step Must Be Run to Read in XACT-Performance Changes to Constraints File	2-11
Register Ordering Takes Precedence over BLKNM Attribute	2-11
BLKNMs Do Not Pass Down Levels of Hierarchy	2-12
Cancel During Translate in Design Manager Causes Memory Leaks	2-12
Design Manager Fails to Find Input Design File and Work Directory on Abbreviated PC-NFS Directory	2-12
Flow Engine Does Not Rerun Timing Step after Changing an Optional Timing Target.....	2-13
Target Family Cannot Be Changed for a Design Manager Project.....	2-14
Stack Overflow Error While Running Design Manager	2-14
GROSTUB Caused a General Protection Fault in Module "pointer.dll"	2-15
Diamond Multimedia Viper Graphics Driver Causes Screen to Go Blank.....	2-15
After Dark v3.0 Screen Saver Can Cause Screen to Hang	2-16
Reserved Net Labels "XIN" and "XOUT"	2-16
Default TBUF Placement in the XC5200	2-16
TIMESPEC Does Not Support Mode Pins as Start or End Points	2-17
Unconnected CI Input Causes XNFPprep Error	2-17
PPR Does Not Enforce Locking of All CLB Pins on XC3000A and XC3000L Devices.....	2-17
XDM Does Not Function while XDE Is Invoked from It.....	2-18

XDM Appears to Hang when MEMGEN Is Invoked with a Non-Existent File	2-18
XMake -L and -X Options Cannot be Selected at the Same Time	2-19
Run XMake with the -X Option for Designs with Xilinx ABEL Modules	2-19
Does Not Accept Upper-Case Input File Names	2-20
Removes DOUBLE Parameter from XC4000 BUF Longline Pull-Ups	2-20
For X-BLOX Designs, Use Ignore_Timespec Options for Both Runs or Not at All	2-21
Warning 4037, Unabsorbed Inverters, Generated Due to BUFE Components.....	2-21
Errors 351 and 312 Issued on Guided Design	2-22
Although -I Option Is Not Selected, PPR May Use DI Pins on CLBs	2-23
Using Both Edges of a Clock Signal with XACT-Performance	2-24
Dual Phase IOB Clocking	2-25
Handling of Unspecified Paths	2-25
Clock Skew Is Not Considered	2-26
Specifying TIMEGRP and TIMESPEC in CST File	2-27
Performance of Designs with No Specifications.....	2-28
IOB Latch and IOB Flip-Flop Controlled by Same Clock.....	2-29
V _{CC} and Ground Signals Are Not Guided	2-30
Interpreting Report File when Guide Routing Is Unlocked ..	2-30
Comparing PPR Delay Reports with XDelay and Timing Simulation.....	2-31
Interaction Between Constraints and Guide Design.....	2-32
Understanding Route_thru_blks and Guide_thru_routes Options	2-33
Placer_effort > 4 May Degrade Designs with 5+ BUFGs	2-34
Constraining RPMs via the CST File	2-34
Internal Program Error: ...Can't Allocate Memory.....	2-35
LCA Files with Unroutes	2-36
Floorplanning	2-36
Unexpected Menus May Be Displayed When Using the Ratsnest Dialog	2-36
The Floorplan Window May Scroll Slowly	2-37
Online Tutorial Displays Using "Large Fonts" Clip the Screen	2-37

The Function Keys Do Not Work When the 'Num Lock'	
or 'Caps Lock' is On.....	2-37
PPR May Fail Due to Invalid Floorplanner Placement.....	2-38
Warning 12926 Occurs When Floorplanner Reads	
a Constraints File That Contains Wild Cards.....	2-38
Multiple Periods Are Not Supported in File Names	2-39
Printing Hangs the System if No Default Printer Selected..	2-39
The Floorplanner Will Not Load a File from a Directory	
that Only Has Group Write Permission	2-39
Saving a File to a Write-Protected Floppy Results	
in a System Error	2-40
Page Fault May Be Caused by Having 32-bit File	
Access Turned On	2-40
The Floorplanner Does Not Optimally Place Counter	
Macros	2-40
Simulation File Creation	2-41
IFD Hold and Delay on D Pin Are Not Modeled	
Correctly for Simulation	2-41
LCA2XNF -v Option Is Not Supported	2-42
Timing Analysis.....	2-42
The Timing Analyzer Show Settings Window Does	
Not Always Push to the Top	2-42
XDelay/Timing Analyzer Reported Setup Value on	
Carry Logic Path Appears Erroneous	2-43
XDelay/Timing Analyzer Does Not Accept Valid	
-ToIOB Option from Template File.....	2-43
Printing World in XACT Causes OpenWin to Crash.....	2-44
-Maxpaths Is Ignored when Performing TimeSpe	
Analysis; Use -TSmaxpaths.....	2-44
Delay from T Pin to Stable Long Line May Be	
Longer Than Reported.....	2-45
Correlating Delays Through BUFTs with Data Book Values	2-46
Does Not Read IGNORE TimeSpecs from PPR	2-46
Analyze Mode Does Not Account for Clock Skew	2-47
OUTFF Feeding INFF in an Unbonded IOB Not	
Included in Clock-to-Setup Analysis	2-47
Configuration.....	2-48
Tie Option Accepted through Implementation Template	
but Not Configuration Template	2-48
Downloading, Configuration, and Verification	2-48
MakeBits Should Configure TTL Inputs by Default.....	2-48

Help Button in the New Group Name Dialog Does Not Invoke Help	2-49
Hardware Debugger May Issue an EMM386 Error or Hang on Invocation	2-49
XChecker Confuses Mouse for XChecker Cable	2-49
Logic Level of Pins Command Is Not a Continuous Probe	2-50
Cannot Delete a Group from the Signal Group Dialog Box	2-50
Viewing Waveforms Textually Prohibits Copying Snapshots and Signals	2-51
Cannot Modify a Group Using the Signal Group Command	2-51
Help is Disabled if Help File is on a Network Drive	2-52
Printing a Graphic Waveform Using the Landscape Orientation Does Not Rotate the Waveform	2-52
Once a Signal or Group Is Selected in a Graphical Waveform, It Cannot Be Deselected	2-53
Double-clicking on the Close Box in a Window Title Bar Does Not Close the Window	2-53
Nets That Have Been Split during Implementation Appear as Split Nets in the Available Signals List Box	2-53
Time-out After X Seconds Option in Trigger Settings Dialog Is Only for External Triggers	2-54
Clicking on No in the Press Enter to Start Readback Dialog Box Displays Failed Readback Message	2-54
Selecting the Print Command from the File Menu without Having a Printer Installed Gives an Internal Warning	2-55
The Hardware Debugger Can Crash if Too Many Waveform Windows Are Opened at Once	2-55
Once a Macro Has Been Issued, It Cannot be Interrupted..	2-56
When a Macro is Saved, Invalid Macro Commands Are Not Flagged	2-56
Non-consecutive Lines in the Console Window Can Not Be Selected Using the CTRL Key	2-56
Printing Only Prints the Currently Displayed Waveform Portions	2-57
Clicking on the Run Macro Toolbar Icon Generates an Error if a Macro is not in Focus	2-57
Console and Macro Windows Can Not Be Printed from the Hardware Debugger	2-57
More than 500 Snapshots Will Not Be Displayed	2-58

An Empty Readback Text File Is Created if There Is Insufficient Disk Space	2-58
Textually Saved Waveforms Cannot Be Re-opened into the Hardware Debugger.....	2-58
Can Not Download Using the Hardware Debugger if Running from an Executable CD-ROM.....	2-59
The Hardware Debugger Can Not Readback at 9600 Baud on Some Machines.....	2-59
The First Read-back Attempt May Fail after a Verify Has Been Performed in the Middle of Several Read Backs	2-60
The Save Readback Command in the File menu Is De-activated When a Waveform is Minimized	2-60
Text Waveforms Cannot Be Printed from the Hardware Debugger	2-60
Warning 001 Is Misleading	2-61
XC2000 Bit Streams May Have Pin Conflicts in Peripheral Mode	2-61
Corrupted .il Files On CD-ROM	2-62
CAE Tools	2-63
Cadence.....	2-63
Negative Timing Delay Errors on Designs Containing XC4000E Synchronous and Dual-Port RAMs	2-63
XC5200 OSC52/OSC5 Behavior Can Not Be Simulated Using the Verilog Library Model.....	2-64
Pulse Width Checks on the CLK Signal Should Be Performed for Both CLock High and Clock Low Times	2-64
XNF2Verilog Error: Symbol Does Not Have Corresponding Entry in the PIN File	2-65
Cadence Verilog-XL: Driving GSR, GR and GTS in Verilog Simulation.....	2-67
XNF2VERILOG V9502-1.21G ERROR: 'Could not find primitive...does_pin_have	2-67
Some Xilinx Unified Library Components Renamed.....	2-69
Primitives with Underscore Ones ("_1") in the Unified Library for Verilog Have Been Renamed.....	2-69
Verilog-XL: How to Handle Upper/Lower Case Conversion of Verilog Signal Names	2-70
Functional Simulation of Pre-Route, Post-Synthesis XNF Netlists from Synopsys (Improved Work Around).....	2-71
Documentation	2-72
Online Documentation	2-72
Hardware & Peripherals User Guide.....	2-72

Group Command Description Does Not Explain	
Signal Order	2-72
Libraries Guide	2-73
RLOC_ORIGIN Required On BUFT RLOCs	2-73
XC4000 CLB Carry Logic Illustration Correction	2-73
ACLK, GCLK Description Corrections	2-73
STARTUP Symbol Correction	2-73
Development System Reference Guide	2-74
XMake -I Option Description Is Incomplete	2-74
XMake Now Reads in a Viewlogic WIR File	2-74

Chapter 3 Xilinx Customer Support Information

Registration, Authorization, and Customer Service	3-1
Technical Support	3-1
Hotline Access	3-1
Training	3-2

Chapter 1

Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 ^a	PC44, VQ64, PC68, PC84, PG84, TQ100	-33, -50, -70, -100, -130
XC2064 ^a	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L ^a	PC84, VQ64, VQ100	-10
XC2064L ^a	VQ64, PC68	-10
XC3020 ^a	PC68, PC84, PG84, CB100, CQ100, PQ100	-50, -70, -100, -125
XC3030 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 ^a	PC84, PG84, CB100, CQ100, PQ100, TQ100, PG132, PP132	-50, -70, -100, -125
XC3064 ^{a b}	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 ^{a b}	PC84, CB164, CQ164, PQ160, PG175, PP175, PQ208	-50, -70, -100, -125
XC3020A	PC68, PC84, PG84, CB100, PQ100	-6, -7
XC3030A	PC44, VQ64, PC68, PC84, PG84, PQ100, VQ100	-6, -7
XC3042A	PC84, PG84, CB100, PQ100, VQ100, PG132, PP132, TQ144	-6, -7
XC3064A ^b	PC84, PG132, PP132, TQ144, PQ160	-6, -7
XC3090A ^b	PC84, CB164, PC84, PG175, PP175, TQ176, PQ160, PQ208	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, VQ100, TQ144	-8

Device	Packages	Speed Grades
XC3064L ^b	PC84, TQ144	-8
XC3090L ^b	PC84, TQ176	-8
XC3120 ^a	PC68, PC84, PG84, CB100, PQ100	-3, -4, -5
XC3130 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 ^a	PC84, PG84, CB100, PQ100, TQ100, PG132, PP132, TQ144	-3, -4, -5
XC3164 ^{a b}	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 ^{a b}	PC84, PQ160, CB164, PG175, PP175, PQ208	-3, -4, -5
XC3195 ^{a b}	PC84, PQ160, CB164, PG175, PP175, PQ208, PG223	-3, -4, -5
XC3120A	PC68, PC84, PG84, CB100, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, VQ64, PC68, PC84, PG84, PQ100, VQ100	-1, -2, -3, -4, -5
XC3142A	PC84, PG84, CB100, PQ100, VQ100, PG132, PP132, TQ144	-1, -2, -3, -4, -5
XC3164A ^b	PC84, PG132, PP132, TQ144, PQ160	-1, -2, -3, -4, -5
XC3190A ^b	PC84, PQ160, CB164, PG175, PP175, TQ176, PQ208	-1, -2, -3, -4, -5
XC3195A ^b	PC84, PQ160, CB164, PG175, PP175, PQ208, PG223	-1, -2, -3, -4, -5
XC4003	PC84, P100, PG120	-4, -5, -6
XC4005 ^b	PC84, PQ100, PG156, PQ160, CB164, PQ208	-3, -4, -5, -6, -6B, -10
XC4006 ^b	PC84, PG156, PQ160, PQ208	-3, -4, -5, -6
XC4008 ^b	PC84, PQ160, PG191, MQ208, PQ208	-3, -4, -5, -6
XC4010 ^b	PC84, PQ160, PG191, CB196, MQ208, PQ208, BG225	-3, -4, -5, -6, -10
XC4013 ^b	PQ160, MQ208, PQ208, PG223, BG225, CB228, PQ240, MQ240	-3, -4, -5, -6, -10
XC4002A	PC84, PQ100, VQ100, PG120	-5, -6
XC4003A	PC84, CB100, PQ100, VQ100, PG120	-4, -5, -6, -10
XC4004A ^b	PC84, PG120, TQ144, PQ160,	-5, -6
XC4005A ^b	PC84, TQ144, PG156, PQ160, PQ208, BG225	-4, -5, -6
XC4010D ^b	PC84, PQ160, PQ208	-5, -6
XC4013D ^b	PQ160, PQ208, BG225, PQ240	-5, -6
XC4003E	PC84, PQ100, VQ100	-3, -4
XC4005E ^b	PC84, PQ100, TQ144, PQ160, CB164, PQ208	-3, -4

Device	Packages	Speed Grades
XC4006E ^b	PC84, PG156, PQ160, PQ208, TQ144	-3, -4
XC4008E ^b	PC84, PQ160, PG191, PQ208	-3, -4
XC4010E ^b	PC84, PQ160, PG191, CB196, PQ208, BG225	-3, -4
XC4013E ^b	PQ160, PQ208, HQ208, PG223, CB228, BG225, PQ240, HQ240	-3, -4
XC4020E ^b	HQ208, PG223, HQ240	-3, -4
XC4005H ^b	PG223, MQ240, PQ240	-5, -6
XC5202	PC84, PQ100, VQ100, TQ144, PG156,	-5, -6
XC5204	PC84, PQ100, VQ100, TQ144, PG156, PQ160,	-5, -6
XC5206 ^b	PC84, PQ100, VQ100, TQ144, PQ160, PG191, PQ208	-5, -6
XC5210 ^b	PC84, TQ144, PQ160, PG223, PQ208, BG225, PQ240	-5, -6
XC5215 ^b	HQ208, HQ240, PG299, HQ304	-5, -6
XC7236A ^a	PC44	-16, -20, -25
XC7318 ^a	PC44, PQ44	-5, -7
XC7336 ^a	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 ^a	PC44, PC68	-7, -10, -12, -15
XC7372 ^a	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q ^a	PC44, PQ44, VQ44	-10, -12, -15
XC73108 ^a	PC84, PQ100, PG144, PQ100, PQ160, BG225	-7, -10, -12, -15, -20
XC73144 ^a	PQ160, BG225	-7, -10, -12, -15
XC8100 ^c	PC44, VQ44	-1
XC8101 ^c	PC84, PQ100	-1
XC8103 ^c	PC84, PQ100	-1
XC8106 ^c	PC84, PQ100	-1
XC8109 ^{b,c}	PC84, PQ160,	-1

a. Not supported in X-BLOX.

b. Not supported in Base packages.

c. XC8100 schematic libraries are included with the Foundation CD. Please complete and fax or mail the XC8100 Foundation update card located*in the Additional Products & Services Packet.

Known Issues

This chapter describes the known issues in this release for software installation, software configuration, the Xilinx design steps, and user documentation.

Software

This section lists the work arounds for the software. They are presented in the general order that they occur in the design process.

Installation

Installer Indicates that Newer Files Exist on Machine When Installing XACTstep 6.0

Platform: PC
Architecture: All
Design Step: Installation
Reference Number: 26484, 27111

When installing the *XACTstep 6.0* software, the Installer may give a warning and indicate that newer files exist in the path. This can occur on systems which have never had Xilinx software installed, as well as on systems which have had the XACT 5.1.1 software installed. The warning can be safely ignored and the installation can proceed by selecting the option to overwrite the newer files.

Software Configuration

Programs Missing from XDM Menus

Platform: All
Architecture: All
Design Step: Software Configuration
Reference Number: 8147

You might find that some programs you installed do not appear in the XDM menus.

Verify that the directory that contains the programs appears in your path variable, then select the Scandisk command from the Utilities menu from in XDM. XDM scans the path variable for supported software.

Run Scandisk after installing any software package.

The Use of Upper Case Names Is Not Supported

Platform: Workstation
Architecture: All
Design Step: All
Reference Number: 24298

Any design which uses upper case letters in the file name will have the name changed to lower case. The tools will also look for a input design names in lower case even if the input name was in upper case. This will cause the tools to error with a message similar to the following:

To enforce case-insensitive data, design names are represented in lower case. Your name "FILE_NAME" is being changed to "file_name." On some operating systems, output file names will change in the same way. See the following example:

```
+ xnfmxn2 @ 1995/05/26 13:29:56 [00:00:06]
+ Parameters
-----
infile      = FILE_NAME
parttype    = ***
outfile     = file_name
```

PPR: ERROR 5603: Unable to open “FILE_NAME.xtf” (for XC4000 family designs) or “FILE_NAME.map” (for XC3000/A/L and 3100A family designs).

Check to make sure this file has been created, and that it is in the current directory. The problem is that although the design was specified as FILE_NAME the tools are looking for file_name.

The solution to this situation is to not use upper case characters in the design file name.

Design Entry

XDM Appears to Hang When SymGen Is Invoked

Platform: Workstation

Architecture: All

Design Step: Design Entry

Reference Number: 14656

When running SymGen with the -v option from XDM on a workstation, XDM can appear to hang because SymGen encountered an error. SymGen enters interactive mode and requires user input; however, the message requesting user input is not printed in the display window.

In this case, terminate SymGen with a Ctrl-C in the XDM window, then run it at the system prompt outside XDM.

Translation

Design Manager Doesn't Accept Speeds with Non-numeric Characters

Platform: PC

Architecture: XC4000E

Design Step: Translation

Reference Number: 28662

Advanced speed grades may come with speed grade labels similar to “-2ADV”. The Design Manager does not translate designs with non-numeric characters in the speed grade name.

Process the design from DOS using the XMake command.

xmake *design name* **-p** *parttype, package, speed grade with non-numeric characters*

Retranslation of XC7000 Design Does Not Pick Up Design Changes

Platform: PC
Architecture: All
Design Step: Translation
Reference Number: 28652

*The Viewlogic netlist translator, *wir2xnf*, writes out *xnf* files to the *primary directory\xnf directory*. The translator executable, *xnfmerge*, first looks in the *primary directory* for the *xnf* file and then the *primary directory\xnf*. If a copy of the *xnf* file exists in the *primary directory*, the translator uses this version instead of the newer version in *primary directory\xnf*.

To translate the newer *xnf* file, delete or rename the *xnf* file in the *primary directory*.

XDM Crashes on Saveprofile

Platform: All
Architecture: All
Design Step: Translation
Reference Number: 27491

XDM crashes on the *Saveprofile* command if an *xdm.pro* file does not exist in the *\$XACT/data* directory and a 'No' response is given to the question: "Do you want to force the profile into the current directory (Y/N)?"

Create an empty *sdm.pro* in your current directory or the *\$XACT/data* directory.

Run XMake with -L Option for Designs Using Non-Unified Libraries

Platform: All
Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H
Design Step: Translation
Reference Number: 15714

XMake does not determine if you used old (pre-Unified Libraries) or Unified Libraries to create your design. XMake defaults to the Unified Libraries.

Run XMake with the `-l` option if you used old libraries to create your design.

XMake Requires WIR File Input for Viewlogic Designs

Platform: All

Architecture: All

Design Step: Translation

Reference Number: 19594

To facilitate ViewSynthesis users, XMake now reads a WIR file instead of a schematic file.

If you only have a Viewlogic schematic file, run the Check command with the `-p` option on the schematic file to recreate the WIR files.

Implementation

Unhandled Exception from Design Manager If Network Drive Doesn't Exist

Platform: PC

Architecture: All

Design Step: Implementation

Reference Number: 28681

If a project exists on a network drive, then the network connection must exist before pointing the Design Manager to the project or before opening the Design Manager with it pointing to the project on the network. If the Design Manager doesn't detect the network drive on opening a project, it produces the following error:

```
---System Error---
```

```
Unhandled exception: Invalid file name, 'k:\83903\sch\motion.1'
```

```
PCFilename class>>getFileSystem
```

```
PCFilename class>>getFileSystem
```

```
PCFilename class>>concreteClassFor:
```

```
PCFilename class>>createInstanceNamed:
```

```
Filename class>>named:
```

Make sure the network connection exists before opening the project, or ignore the message and open a project on a drive that is defined.

Small Talk Error: Video Driver out of Memory

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 28365

If your video drive uses a large number of colors (16 million), the Design Manager may report a Small Talk Error: Out of Memory when starting and the XACTstep logo appears.

Reduce the amount of colors used by the video drive and restart the Design Manager.

Mouse with Left-handed Settings May Not Work in Design Manager/Flow Engine

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 28353

Some pull-down menus in the Design Manager and the Flow Engine may not respond to mice with left-handed settings.

To switch to right-handed settings, in Windows go to the Control Panel in the Main Group, click on the Mouse icon and the Swap Left/Right box.

Opening Design Manager on Projects Deleted outside Design Manager Gives Unhandled Exception

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 27815

If Design Manager attempts to open a project that has been deleted through DOS or Windows, it issues the following error message:

Unhandled exception: No space available to allocate this object

```
IdentityDictionary class(Behavior)>>newNoRetry;  
IdentityDictionary class(Behavior)>>handleFailedNew.size;  
IdentityDictionary class(Behavior)>>new;  
IdentityDictionary class(Set Class)>>new;  
BinaryObjectStorage>>initialize
```

All project management should be done through the Design Manager.

XBLOX Counters Can Not Be Larger than 31 Bits Wide

Platform: All

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Implementation

Reference Number: 27665

The largest allowable value the COUNT_TO property on the XBLOX counter can take is 16#7FFFFFFF#. If a larger value is submitted the following error message occurs:

```
***XBLOX: ERROR 20224:
```

```
INTERNAL ERROR
```

```
Please contact Xilinx Technical Support. Please  
provide the following details to the support  
personnel. This information is needed by the software  
developers.
```

```
1.
```

```
representation_erttot(is(_529,+(*(268435455,16),15)),  
2,'interger overflow')
```

Opening Design Manager Gives Unhandled Exception: Subscript out of Bounds

Platform: PC

Architecture: All

Design Step: Implementation

Reference Number: 27650

Invoking the Design Manager may elicit the following error message:

Unhandled exception: Subscript out of bounds:

```
TwoByteString(Object)>>subscriptBoundsError:  
TwoByteString(Object)>>basicAt:  
TwoByteString(Object)>>at:  
ISO8859L1 String class(ByteEncodeString class)>>decode:  
Win32Interface>>getDosEnvironmentAsArrayOfStrings
```

This error is caused because there are control or escape characters in the environment variables, such as:

```
PROMPT $p $e[1mp$g$e[0m$e[32m$w[k
```

Remove all control or escape characters from environment variables.

Manually Deleting Project Directories and Files Leads to System Errors in the Design Manager

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 27268

If you manually delete files or directories associated with a Design Manager project, it is possible for system errors to occur in the Design Manager for that project. The Design Manager tracks the project files and directories as they are being created and assumes that they will be there when needed. If you manually delete project data from DOS or the Windows File Manager, the Design Manager is not aware of the changes and may issue errors when it tries to access the data.

If you need to delete project data, you should use the Delete command from the Design menu in the Design Manager. This allows the Design Manager to keep track of data being removed and helps prevent such system errors.

Renaming the Project Generates a System Error

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 27274

The project name cannot be renamed or deleted from the Project View in the Design Manager. Attempting to do this will generate a - System Error - dialog complaining of an “Unhandled exception”.

Simply closing the system error dialog will clear the error and leave the system unaffected.

Specifying a Guide Design in the Design Implementation Dialog When Also Specifying a Guide File Using Flow Engine Advanced Dialog Is Misleading

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 27328

It is possible to specify the use of a guide file in two ways within the Design Manager environment. You can specify a previous design implementation using the pull-down menu in the Design Implementation Dialog. You can also specify a guide file outside the Design Manager environment using the Advanced command under the Flow Engine Setup menu. If different guide files are selected in these two locations, the Flow Engine will use the guide file specified in the Advanced dialog, however both the Design Implementation dialog and the status bar in the Flow Engine will indicate that the design specified in the Design Implementation Dialog will be used. This is wrong. You can verify exactly what command will be issued by using the Preview command and selecting the Command Line view mode.

Clicking On a Report in the Report Browser Generates the Error Message: “The Report File Is Missing”

Platform: PC
Architecture: All
Design Step: Implementation
Reference Number: 26876

This message is generated when the Report Browser cannot find the report associated with the selected icon. A common cause of this error is that the revision or version names have been changed causing the Report Browser to lose track of the file's location. To fix this problem, simply copy the revision using the Copy Revision command under the Design Menu. Specify the new name in the dialog which appears, then click OK. All of the design data will be copied to the new revision and now will be accessible from the Report Browser.

Customize Templates Do Not Allow Spaces in Parameters

Platform: Windows 3.1/3.11
Architecture: All
Design Step: Implementation
Reference Number: 26469

When you create a customized template for the Flow Engine, you must not put spaces before or after the equals sign (=). Spaces will cause the option to be ignored.

Do not include spaces between the option name, the equals sign and the value.

PCs With No Math Co-Processor Require a Manual Installation of PPR

Platform: PCs
Architecture: All
Design Step: Implementation
Reference Number: Not Available

If your PC is configured without a math co-processor, you must use a version of PPR, which is available on the XACT 6.0 CD-ROM, that is compiled to emulate the co-processor. If you run PPR on such a configuration, the following message is displayed:

```
80X87 required but not present!
```

Note: You may want to save the standard PPR.exe file before installing the emulator version, though it is always available from the CD-ROM in D:\XACT\PPR.EXE.

You can install the emulator version of PPR by following these steps: (with these assumptions: the CD-ROM is drive D:, the installed drive is drive C: and the XACT path is \XACT)

1. Insert the XACT 6.0 CD.
2. Go to the top-level, installed XACT directory.
3. Enter the following command string:

```
COPY D:\XACT\EMUL\PPR.EXE C:\XACT\PPR.EXE
```

Most PCs have math co-processors, so the special version of PPR is not needed. The exceptions include, the 486 SX, most laptop machines, and some clones.

If you are not sure whether you have a math co-processor, you can find out on most PCs by running the “msd” program, and checking the value of “Math Co-processor” under “Computer”.

Optimize Step Must Be Run to Read in XACT-Performance Changes to Constraints File

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100A, XC4000/A/D/E/H, XC5200

Design Step: Implementation

Reference Number: 13039

If you change the timing requirements in a constraints file and do not rerun the Optimize step, the new timing requirements will be ignored and the old timing requirements will be used.

If you are designing with XC5200, XC4000, or XC3000A parts, and you are using a constraints file to specify XACT-Performance requirements, run the Optimize step in the Flow Engine anytime you modify the timing requirements in a constraints file.

Register Ordering Takes Precedence over BLKNM Attribute

Platform: All

Architecture: XC3000/A/L

Design Step: Implementation

Reference Number 21882

If two flip-flops have consecutively labeled nets on their Q outputs, such as Q0 and Q1, it is possible that XNFMAP will map the flip flops into the same CLB, even when they have different BLKNM or HBLKNM attributes.

Change the name of one of the output nets to a different, non-consecutive label to avoid this possibility.

BLKNMs Do Not Pass Down Levels of Hierarchy

Platform: All
Architecture: All
Design Step: Implementation
Reference Number: 20476

BLKNM and HBLKNM attributes must be placed on Xilinx primitives rather than on the hierarchical symbols (with the intent of passing them down to the primitives). XNFMerge does not pass these attributes from the hierarchical symbols down to the underlying primitives.

Place BLKNM and HBLKNM attributes directly on the Xilinx primitives.

Cancel During Translate in Design Manager Causes Memory Leaks

Platform: Windows 3.1/3.11
Architecture: All
Design Step: Implementation
Reference Number: 26257

When translating a design file into the Design Manager, a Cancel button is available to terminate the process. Avoid using this button when the translate process is initializing, as it can result in allocated memory not being released upon termination.

If you want to cancel a translate command, wait until some processing has occurred before clicking the Cancel button. If you suspect memory has been lost due to this sequence, you can recover the memory by quitting the Design Manager and restarting.

Design Manager Fails to Find Input Design File and Work Directory on Abbreviated PC-NFS Directory

Platform: Windows 3.1/3.11
Architecture: All
Design Step: Implementation
Reference Number: 25958

When using PC-NFS, any file or directory name which contains upper case letters or which violates the MS DOS "8.3" convention gets abbreviated with control characters. For example, the name in

UNIX LongNameDir may appear in DOS via PC-NFS as longn^le. These control characters are not understood by the Design Manager. If you use a file or directory name with these characters when you are creating a project in the Design Manager, one of the following errors will occur:

Cannot find input design. Please specify an existing design.

or

Cannot find work directory. Please specify an existing directory.

If the input design file contains PC-NFS abbreviations, the work around is to rename the design file so that it conforms with the DOS "8.3" standard.

If the input design directory or work directory contains PC-NFS abbreviations, the work around is to rename the offending directories so that they do not exceed eight characters and contain no upper case letters.

Note: The input and work directory have the additional restriction of being strictly alphanumeric as referenced in next known issue, "Design Manager Requires Strictly Alphanumeric Characters for Input Design Directory and Work Directory."

Flow Engine Does Not Rerun Timing Step after Changing an Optional Timing Target

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 25635

In the design implementation options dialog, there are optional targets you can select to Produce Timing Simulation Data and to Produce Timing Report. If you select only one of the timing options, run the flow to complete timing, and then select the other timing option, the Flow Engine will not detect the selection of the second timing option. The Flow Engine will indicate that the Timing step is completed, despite the second timing target not being completed.

The work around is to use the Backup command and rerun the Timing step.

Target Family Cannot Be Changed for a Design Manager Project

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 25142

Once a project is created in the Design Manager, it is not possible to change the Target Family. If you select the wrong Target Family when creating a project, you must delete the erroneous project and create a new one.

If you have an existing project which you have been working with and you wish to retarget to a new family, you must make the appropriate changes to the input design and create a new project specifying the new Target Family.

Stack Overflow Error While Running Design Manager

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 26019

You may encounter the following error while running the Design Manager:

APPLICATION ERROR: STACK OVERFLOW

Two potential work arounds have been identified for this error. One is to change the STACKS setting in your config.sys. Typically, the default setting is STACKS=9,256. If so, change it to STACKS=0,0 to disable stack swapping, which can slow the system enough to cause some high-speed communications programs to fail.

The second work around is to increase your virtual memory size. The virtual memory can be changed by using the 386 Enhanced command from the Control Panel under the Main Windows group. For further details on the minimum memory requirements, refer to the *Getting Started and Installation Guide*.

GROSTUB Caused a General Protection Fault in Module “pointer.dll”

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 25964

You may encounter the following error when running programs under Windows:

GROSTUB Caused a General Protection Fault in Module
“pointer.dll”

This is a known Microsoft bug. It is caused by the Microsoft Mouse driver 9.01 GROWSTUB component. To correct this problem, do one of the following:

- Remove POINTER.EXE from the LOAD= line in the win.ini file and then restart Windows.
- Upgrade to the Mouse IntelliPoint software version 1.0.
- Install the Microsoft Mouse driver version 9.01b POINTER.DLL file.

The above information is from a Microsoft application note, HD1061.

Diamond Multimedia Viper Graphics Driver Causes Screen to Go Blank

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 25046

A problem exists in the Diamond Multimedia Viper graphics driver which causes the display monitor to go blank when calling a DOS program from within a Windows application. Since some of the Xilinx Windows applications do call DOS programs, you may encounter this problem.

Try a lower resolution display mode.

After Dark v3.0 Screen Saver Can Cause Screen to Hang

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Implementation

Reference Number: 25697

It has been observed that while running the Design Manager, the After Dark v3.0 Screen Saver can cause the display to hang.

Disable the After Dark screen saver.

Reserved Net Labels “XIN” and “XOUT”

Platform: All

Architecture: XC3000/A

Design Step: Implementation

Reference Number: 18003

The net label “XIN” and “XOUT” are reserved key words which indicate that those I/O nets should be placed on the dedicated crystal input and output. Whether these nets are constrained to any other I/O locations, XNFMAP will ignore those constraints and still place these nets on the dedicated crystal input and output pins.

Do not use these reserved key works for I/O net labels.

Default TBUF Placement in the XC5200

Platform: All

Architecture: XC5200

Design Step: Implementation

Reference Number: 21504

For small XC5200 designs PPR, by default, will try to spread logic out in order to reduce the number of signals routed in and out of a given versablock. The reason for this is that there is a limit of only 24 nodes that can be used as I/O as well as general purpose routing thru the GRM for a given tile. A result of this logic spreading is that TBUFs which do not have locations constraint will not be placed in TBUF location 0.

For example: in a group of 4 TBUFs with the same control signal, the first 3 TBUFs would be placed in logic cell 1,2,3 of one CLB and the fourth would be placed in logic cell 1 of another CLB. In a more dense

design, PPR will use all four TBUFs in a versablock where feasible. This is being done deliberately to avoid congestion in routing. PPR will use the 4th TBUF only when it is forced to with location constraint or in high-density designs.

TIMESPEC Does Not Support Mode Pins as Start or End Points

Platform: All
Architecture: XC4000
Design Step: Implementation
Reference Number: 24025

When using one of the mode pins in an XC4000 device for either an input or an output, the software doesn't allow you to place timing specifications on the mode pads. If you put a TNM on the MD0, MD1, or MD2 pads then XNFMERGE gives you an error saying that there is a TNM on an illegal symbol of type "Mdx."

Do not use I/O pins MD0, MD1, or MD2 in a critical timing path.

Unconnected CI Input Causes XNFPrep Error

Platform: All
Architecture: XC4000/A/D/E/H, XC5200
Design Step: Implementation
Reference Number: 21855

When using an arithmetic macro from the Unified Libraries, the CI input pin must be attached to a signal. If CI is left unconnected, XNFPrep will issue Error 4022.

If your design does not use the CI input, connect CI to either V_{CC} or ground, as appropriate for your application.

PPR Does Not Enforce Locking of All CLB Pins on XC3000A and XC3000L Devices

Platform: All
Architecture: XC3000/A/L
Design Step: Implementation
Reference Number: 18508

The "P" attribute (pin lock) on pins of CLBMAP or CLB symbols in the XC3000A/XC3000L family is used to indicate that the associated

net be “locked” onto the given pin. The MAP=PLC attribute on CLBMAP symbols applies the pin lock to ALL pins. This feature is not supported by PPR in the case where the pin to be locked is the data input of a flip flop and CLBMAP primitives are used to define the mapping.

The solution is to use a CLB primitive to define the configuration required (instead of using a CLBMAP/Logic combination) and attach pin lock properties to its pins.

PPR supports pin locking if the input is from a logic gate and the CLB pin being locked to is the A, B or C pin. In the case of locking an input to the D or E pins of the CLB, the actual pin used is determined by the pin swaps performed by the router. In this case the input will either be on D or E, but you cannot control which.

Again, use a CLB primitive to define the configuration required (instead of using a CLBMAP/Logic combination) with pin lock properties on its pins.

Note: CLB primitives cannot be functionally simulated.

XDM Does Not Function while XDE Is Invoked from It

Platform: Workstation
Architecture: All
Design Step: Implementation
Reference Number: 14587

XDM does not function while XDE or any other application or process is invoked from it.

Wait until the spawned process terminates before using XDM again.

XDM Appears to Hang when MEMGEN Is Invoked with a Non-Existent File

Platform: Workstation
Architecture: XC4000/A/H
Design Step: Implementation
Reference Number: 16671

When MemGen is called with a new, non-existent file, it tries to create the new file by going into interactive mode and asking a number of questions. This is a valid MemGen operation and is supported by XDM.

However, on workstations, these questions or prompts are not printed until after you have typed in the correct number of responses. MemGen and XDM appear to be hung.

In this case, terminate MemGen with a Ctrl-C in the XDM window, then run MemGen at the system prompt outside XDM.

XMake -L and -X Options Cannot be Selected at the Same Time

Platform: All

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16454

The -l option tells XMake to run the translators MemGen and ABL2XNF with their Use Old Library option to generate XNF files.

The -x option tells XMake to start from XNF files.

Therefore, specifying the two options together is meaningless, and if XMake is run at the system prompt with both options selected, it prints this message.

```
>>> Option '-L' is ignored when '-X' is specified.
```

To avoid this situation, the XMake Option menu in XDM does not allow you to select the -l and -x options at the same time.

Run XMake with the -X Option for Designs with Xilinx ABEL Modules

Platform: HP7000 and RS6000

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16711

On the HP700 and RS6000 platforms, automatic translation of Xilinx ABEL modules using ABL2XNF is not supported. When run on these platforms, XMake tries to run ABL2XNF on the ABL files in the design but does not find ABL2XNF. It removes the XNF files that correspond to the ABL files and issues an error.

Manually translate the ABL files on a platform that supports Xilinx ABEL or ABL2XNF, then move the file onto the HP700 or RS6000 platform. Run XMake with the `-x` option. If you are using `pld_xmake` (Mentor users), then remove or rename the ABL files before running `pld_xmake`. `Pld_xmake` runs XMake without the `-x` option.

Does Not Accept Upper-Case Input File Names

Platform: Sun, HP

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 10353

All output files created by Xilinx software are in lower case. Since the implementation procedure begins with running XNFMerge, and the input to XNFMerge might be created by third-party tools, XNFMerge accepts upper-case letters in input file names. XNFPrep, which can only read XNFMerge output, does not.

Always run XNFMerge before XNFPrep. Do not rename your XNFMerge output files to names containing upper-case letters.

Removes DOUBLE Parameter from XC4000 BUFT Longline Pull-Ups

Platform: All

Architecture: XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 14504

In XC4000 family devices, the BUFT-driven horizontal longlines can be split in the middle of the device to form two half-length longlines. Since the pull-up resistors on the horizontal longlines are at either edge of the device, the directive to use two pull-ups would prevent PPR from using half-edge longlines and would complicate BUFT placement.

Since the timing characteristics of a half-longline with a single pull-up is comparable to the timing of a whole longline with two pull-ups, PPR selects between a whole and a half longline in the placement stage. If a whole longline is used, PPR activates both pull-ups; if a half-longline is used, PPR activates only one pull-up. (Of course, if

the design does not indicate pull-ups on the longline signal, PPR does not activate any of them.)

Because this decision is made in PPR, XNFPprep removes any DOUBLE parameters, or more than one pull-up symbol, from BUFT-driven signals in XC4000 designs.

For X-BLOX Designs, Use Ignore_Timespec Options for Both Runs or Not at All

Platform: PC

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16833

The flow for processing X-BLOX designs includes two runs of XNFPprep. If you use the XNFPprep Ignore_timespec option to ignore any or all TIMESPEC/TIMEGRP statements when processing an X-BLOX design, you must set the option to the same value for both runs of XNFPprep.

For example, using Ignore_timespec=design with only the post-X-BLOX run of XNFPprep does not properly ignore the design specifications. The pre-X-BLOX run of XNFPprep must also use the Ignore_timespec=design option.

This restriction is automatically satisfied if you process your design with XMake, because XMake uses the same option value for both runs of XNFPprep.

Warning 4037, Unabsorbed Inverters, Generated Due to BUFE Components

Platform: All

Architecture: XC3000/A/L, XC3100/A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 14336

For convenience and compatibility with EPLD devices, the Unified Libraries include 3-state buffer elements with both active-Low enable (the BUFT elements) and active-High enable (the BUFE elements). The actual 3-state buffers in the XC4000- and XC3000-based architectures have active-Low enables that are not directly invertible. If a BUFE element is sourced by a gate, the inversion of the enable signal is performed in the same function generator used to implement the

gate and no extra delay is incurred. However, if a BUFE element is sourced by a flip-flop, or by another element without a dedicated output inversion, the inversion of the enable signal is implemented in an additional function generator, adding an extra level of delay to the path.

When an inverter cannot be absorbed at the source or load pins, XNFPrep issues a message similar to the following.

```
XNFPREP: WARNING 4037
```

```
These inverters could not be absorbed and each will be  
implemented in a single function generator. This will  
introduce additional delay and use resources  
inefficiently. (Note that some of the symbols listed  
below may have been reduced to inverters by earlier  
trimming.)
```

```
Inverter Name = inverter_name  
Output Signal = signal_name/T
```

The presence of “/T” at the end of the output signal name indicates that the inverter might be part of a BUFE component.

If the delay on a 3-state enable path is important, and the enable signal is sourced by a non-invertible output, you may need to re-think the relevant portion of the design to avoid using a BUFE component.

Errors 351 and 312 Issued on Guided Design

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 14898

When using an XNF file generated by LCA2XNF (and renamed to design.PGF) as a guide for a new design, XNFMAP might issue one or several error messages similar to the following example.

```
ERROR 351: Guide symbol 'symbol_name' tried to map  
symbol_type 'symbol_name' into a new CLB, but it has  
already been assigned to a CLB by guide symbol  
'symbol_name' .
```

```
ERROR 312: Cannot map GUIDE file symbol 'symbol_name' as  
directed. Refer to error messages listed above.
```

These messages reflect the fact that PPR uses through-block routing (feed-throughs), and new net names are generated by PPR for this routing. The new net names are carried into the XNF file generated by LCA2XNF. Therefore, XNFMAP is reading a guide file with nets that are not on the CLBMAP pins in the original design.

In this case, XNFMAP traces back through the network to find gates to include in a CLB because it does not recognize the nets on the input pins to the CLBMAP (they are the through-block net names). XNFMAP finally reaches a net that has already been mapped, and issues the above error messages.

XNFMAP does not stop on errors with GUIDE file CLBMAPs, and does produce a valid MAP file for the design. You can therefore continue with your design; however, the symbols referenced in the error messages are not guided.

Whenever possible, use the PGF file from the original run of XNFMAP as a guide, rather than using LCA2XNF to create a PGF file.

Although -I Option Is Not Selected, PPR May Use DI Pins on CLBs

Platform: All

Architecture: XC3000, XC3100

Design Step: Implementation

Reference Number: 16370

XNFMAP does not use the DI (direct flip-flop input) pin on XC3000 family CLBs unless called with the -I option. However, PPR may use DI pins with XC3000A/L and XC3100A designs.

The reason for this discrepancy is that although XNFMAP does not use DI pins, PPR sometimes swaps pins to improve routing and places a signal on this pin. Unlike the other input pins, the DIN pin has a positive hold time, but this is rarely a problem as routing generally introduces sufficient delay to meet the requirement.

Using Both Edges of a Clock Signal with XACT-Performance

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 13826

With path-type C2S or DC2S TIMESPEC statements, PPR automatically controls paths between flip-flops clocked by different edges of the same clock at half of the specified delay (or a different fraction, if the `high_time` parameter is specified).

Since the FROM:TO TIMESPEC statement explicitly specifies the path endpoints and the maximum delay between them, no automatic adjustment for dual-phase clocks occurs. If you are using both edges of the same clock signal, use the RISING and FALLING constructs of the TIMEGRP statement to define the appropriate specifications.

For example, assume that the 20MHz signal CLK20 sources both rising and falling edge flip-flops, and that the parameter `TNM=CLK20` is attached to that clock signal. The following TIMESPEC is not enough to control all paths properly.

```
TS01=FROM:CLK20:TO:CLK20=50NS
```

To control the paths between opposite-edge flip-flops properly, first define the following TIMEGRP statements.

```
POS_EDGE=RISING:CLK20
NEG_EDGE=FALLING:CLK20
```

The previous TIMESPEC statements separate the flip-flops in CLK20 into two subgroups, POS_EDGE and NEG_EDGE, on the basis of the polarity of their clock pins. Then, add the following TIMESPEC statements.

```
TS02=FROM:POS_EDGE:TO:NEG_EDGE=25NS
TS03=FROM:NEG_EDGE:TO:POS_EDGE=25NS
```

While TS01 applies to all paths clocked by CLK20, TS02 and TS03 are faster and override the 50ns specification on those paths between opposite-edge flip-flops. For example, if there are no paths from falling edge to rising edge, TS03 is superfluous.

Dual Phase IOB Clocking

Platform: All
Architecture: XC3000, XC3100
Design Step: Implementation
Reference Number: Not Available

APR V5.x cannot handle an XC3000 or XC3100 design in which two IOB flip-flops on the same edge of the device are clocked by different polarities of the same clock signal. Unless such pins are constrained to different edges of the chip, APR stops and issues the following message.

```
dual-phase IOB clocking is not supported.
```

Assign each IOB flip-flop controlled by one edge of a dual-phase clock to a specific pin location, so that the two phases of the clock are located on different edges of the device. An edge constraint (T, B, L, or R) is not sufficient; a specific pin location is required.

If the LCA file input to APR already has the IOBs correctly placed and the -l (lower-case L) option is used to lock placement, APR might still issue a message about dual-phase IOB clocking. In this case, include the LOCK IOBS constraint in the CST file and rerun APR -l.

Note: PPR does support dual phase IOB clocking for XC3000A, XC3100A, and XC3000L devices.

Handling of Unspecified Paths

Platform: All
Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H
Design Step: Implementation
Reference Number: 13826

Prior to PPR V5.x, a default specification was applied to every path in the design that was not explicitly specified or ignored. These defaults were either (1) a user-specified delay from a DC2S, DC2P, DP2S or DP2P statement, or (2) a delay assigned automatically by PPR.

PPR V5.x adds default specifications only when there are no user-assigned specifications on paths of that type. For example, if no paths that begin at I/O pads and end at flip-flops are explicitly specified, PPR adds a specification of the following form.

```
DEFAULT_FROM_PADS_TO_FFS=FROM:PADS:TO:FFS=AUTO
```

Specifying paths beginning and ending at flip-flops does not stop PPR from applying the previous default. However, if even one path from a pad to a flip-flop is specified, PPR does not apply the above default, and the timing of all other pad-to-flip-flop paths is uncontrolled.

In general, if you apply any specifications to the design, you should ensure that all important paths of that type are fully specified. Using predefined groups, such as PADS or FFS, can make this task easier. For more information, see the “Using Predefined Groups” section and the “When Multiple Specifications Apply to the Same Path” section in the “XACT-Performance” chapter of the *Development System Reference/User Guide*.

Clock Skew Is Not Considered

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 5226

In analyzing path delays to meet XACT-Performance requirements, PPR V5.x assumes that there is no skew between clock pins on flip-flop to flip-flop paths. All path delay calculations are made relative to the clock-pin on the flip-flop rather than the source of the clock signal.

For a clock signal distributed through a global buffer (BUFG, BUFGP, BUFGS, GCLK, or ACLK), the skew between clock pins is negligible. However, if a clock signal does not go through a global buffer, the skew between clock pins can be significant. A TIMESPEC requirement from the source of the clock signal to the appropriate flip-flops can enforce a maximum allowable delay, but some delays may be less than this maximum. Xilinx recommends that you use a global buffer to clock flip-flops that belong to timing-critical paths.

Specifying TIMEGRP and TIMESPEC in CST File

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: Not Available

As an alternative to the TIMESPEC and TIMEGRP schematic symbols, specifications, and group definitions can be placed in the CST file. However, the documentation is somewhat unclear on how to place these in the CST file.

The CST file can be used to specify parameters that would otherwise be attached to a TIMESPEC or TIMEGRP symbol. (It is not possible to use the CST file to specify TNM parameters that would otherwise be attached to symbols or signals.) The basic syntax is as follows.

```
TIMESPEC="timespec_parameter" ;
```

```
TIMEGRP="timegrp_parameter" ;
```

The `timespec_parameter` is the same text that would be attached to a TIMESPEC symbol. The `timegrp_parameter` is the same text that would be attached to a TIMEGRP symbol. See the "XACT-Performance" chapter of the *Development System Reference Guide* for more information on these parameters.

After adding or changing TIMESPEC or TIMEGRP statements in the CST file, you **MUST** rerun the XNFPrep program for the changes to take effect. If your design contains XBLOX symbols, you must return to the first run of XNFPrep. Although PPR also reads the CST file, it processes only the placement constraints. To verify that TIMESPEC and/or TIMEGRP changes have been incorporated, examine the Timing Specification Summary section of the XNFPrep (design.prp) report.

Several examples of TIMESPEC and TIMEGRP CST file statements are shown following.

```
TIMEGRP="updata_io=PADS(updata<*>)" ;  
TIMESPEC="TS04=FROM:LATCHES:TO:updata_io=50ns" ;  
TIMEGRP="CLK40_POS=ISING:CLK40" ;  
TIMEGRP="CLK40_NEG=FALLING:CLK40" ;  
TIMESPEC="TS02=FROM:CLK40_POS:TO:CLK40_POS=20MHz" ;  
TIMESPEC="TS03=FROM:CLK40_POS:TO:CLK40_NEG=40MHz" ;
```

Performance of Designs with No Specifications

Platform: All

Architecture: XC3000/A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16262

If no XACT-Performance requirements are specified in a design, PPR V5.x attempts to apply reasonable delay targets. However, it may be possible to improve the performance of the design markedly by adding a few simple specifications. This performance improvement is particularly true of designs that have more than one clock signal and/or flip-flops clocked by opposite edges of the same clock.

For best results, use the following table to determine the minimum XACT-Performance specifications you should place on your design.

Specifying the correct clock period, high_time and low_time, as shown in the table, ensures that PPR applies the most effort to those paths that must run fast, rather than applying its efforts to optimizing all paths.

Clock Signals		Minimum XACT-Performance Specification
More than One?	Both Edges Used?	
No	No	Add the following TIMESPEC statement: <i>TSid=FROM:FFS:TO:FFS=period</i>
No	Yes	Add the following TIMEGRP statements: <i>pos=RISING:FFS</i> <i>neg=FALLING:FFS</i> Add the following TIMESPEC statements: <i>TSid=FROM:pos:TO:neg=high_time</i> <i>TSid=FROM:neg:TO:pos=low_time</i> <i>TSid=FROM:FFS:TO:FFS=period</i>
Yes	No	For each clock signal: attach <i>TNM=name</i> to clock signal add the following TIMESPEC statement: <i>TSid=FROM:name:TO:name=period</i>
Yes	Yes	For each clock signal: attach <i>TNM=name</i> to clock signal add the following TIMEGRP statements: <i>name_p=RISING:name</i> <i>name_n=FALLING:name</i> add the following TIMESPEC statements: <i>TSid=FROM:name_p:TO:name_n=high_time</i> <i>TSid=FROM:name_n:TO:name_p=low_time</i> <i>TSid=FROM:name:TO:name=period</i>

IOB Latch and IOB Flip-Flop Controlled by Same Clock

Platform: All

Architecture: XC3000/A/L, XC3100A

Design Step: Implementation

Reference Number: 14401

In the XC3000 architecture, there are two I/O clock lines on each edge of the device. Since the IOB clock inputs cannot be individually inverted, any one I/O clock line can drive either (1) rising-edge flip-flops and/or transparent-Low latches; or (2) falling-edge flip-flops

and/or transparent-High latches. (In the Unified Libraries, the transparent-High latch is called ILD; in the older libraries, it is called INLAT.)

However, PPR is unable to handle a mixture of IOB flip-flops and IOB latches controlled by the same clock signal, even if the above rules are followed. If you have such a situation in your design, you might see the following message in MakeBits.

```
IOB clock(s) inverted inconsistently, run DRC.
```

The work around for this problem is to constrain flip-flops and latches on the same clock so that they are placed on different edges of the device. For example, use LOC=L (left edge) on the IOB flip-flops and LOC=T (top edge) on the IOB latches. Because two different I/O clock lines are used, PPR is able to route the design properly.

V_{CC} and Ground Signals Are Not Guided

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 15161, 16184

PPR does not mimic the routing of V_{CC} and ground signals that are found in the guide LCA file. Since the timing of these static signals is irrelevant, the routing resources they use in the guide design may be better used to route signals that have been added or changed since the last iteration. All V_{CC} and ground signals are routed at the end of the routing process.

Be aware that a design created with the Guide_only=true option or the Route=false option has all V_{CC} and ground signals unrouted and sourceless, as shown in XDE and XDelay reports. The V_{CC} and ground load pins are also reported by PPR as being unrouted.

Interpreting Report File when Guide Routing Is Unlocked

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16735

The Lock_routing option in PPR controls which guided signals are allowed to be rerouted by PPR. If Lock_routing is set to Whole_sigs, changed signals can be rerouted; if set to None, any signal can be rerouted. Unlocking the guide routing allows PPR to improve the overall performance of the design.

When Lock_routing is set to None or Whole_sigs, the guide chapters of the PPR report file may list some logic that was matched between the guide design and the new design as unguided. The guide information in the report file is based on a comparison of the guide design with the newly created LCA file. As such, changes in unlocked guide routing are reflected in this report.

Signals that were rerouted by PPR appear in the report file chapter titled “Unguided Signals from Input Design.” For example, if the rerouting of a signal causes an output pin to be swapped (the XQ and YQ flip-flops are swapped to better route their output signals), the source elements appear in the “Unguided Blocks from Input Design” chapter of the report file.

Comparing PPR Delay Reports with XDelay and Timing Simulation

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 5139, 5633

The path delays reported by PPR may occasionally differ from the timing reported by XDelay or by timing simulation (the delays for timing simulation are calculated by the LCA2XNF program). Such discrepancies occur for two reasons: (1) PPR does not trace certain paths the same way that XDelay does; and (2) PPR calculates some delays incorrectly.

In all cases, the delays reported by XDelay and timing simulation (LCA2XNF) should be considered definitive. If there is a discrepancy in the delay for a particular path, use the timing reported by XDelay or LCA2XNF.

You should consider the path delays reported by PPR as estimates only. *Always run XDelay or use timing simulation to determine the actual design performance.*

Interaction Between Constraints and Guide Design

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 16509, 16609, 15259

In the PPR guided design process, placement constraints in a schematic or CST file take precedence over placement information in the guide design. The impact of this rule depends on whether CLB or BUFT logic is involved, as described following. Edge decode logic is also a special case, as discussed in the following paragraphs.

CLB-type logic — flip-flops, function generators, XC4000 RAM and carry logic — is placed according to any placement constraints, and other logic is then guided around these pre-placed elements.

Example 1: Assume a flip-flop is in location CLB_R3C7 in the guide file and has the parameter LOC=CLB_R5C10 in the design file. PPR places this flip-flop in CLB_R5C10.

Example 2: Assume flip-flop 1 is in location BC in the guide file and has no placement constraints, but flip-flop 2 has the parameter LOC=BC in the design file. PPR places flip-flop 2 in location BC, and flip-flop 1 is unguided and placed according to the normal placement procedure.

Each group of *BUFTs with a common output signal* is placed according to the guide design, unless a placement constraint moves one of the BUFTs to a new row, or moves a different group of BUFTs onto the original row. In either case, PPR unguides all of the BUFTs on that output signal.

Example: Assume that the guide design contains seven BUFTs driving the signal DATA3, and they are located in TBUF_R3C3.1 through TBUF_R3C8.1. In the design file, one BUFT is assigned the parameter LOC=TBUF_R7C2.2. PPR places the constrained BUFT in location TBUF_R7C2.2, and unguides the other six BUFTs to place them somewhere in row TBUF_R7C*.2.

Each group of *BUFTs with a common enable signal* is placed according to the guide design, unless one of the BUFT locations in the guide design is prohibited with a CST file constraint. If any BUFT location is blocked, PPR unguides all BUFTs having that enable signal and attempts to align them vertically in an available column.

Each group of *edge decoders* with a common output signal is placed according to the guide design, unless a placement constraint conflicts with the guide location of any single edge decoder. If any constraint-guide conflicts are found, the entire group of edge decoders is unguided and placed according to the constraints.

Understanding Route_thru_blks and Guide_thru_routes Options

Platform: All

Architecture: XC3000A/L, XC3100A, XC4000/A/D/E/H

Design Step: Implementation

Reference Number: 15818

PPR V5.x has two options that control the use of through-routes, which are signals routed through CLBs or other blocks to improve routability and/or performance. The `Route_thru_blks` option controls where through-routes can be placed. The `Guide_thru_routes` option determines which through-routes from a guide design are preserved in the new design. The interaction between these two options and the guide process is not clearly explained in the documentation.

- The `Route_thru_blks` option controls only new routing. For example, assume that a signal is initially routed by PPR when `Route_thru_blks` is set to OK and a through-route is used. If this LCA file is used as a guide file for the next iteration of PPR, the through-route on that signal is preserved, even if `Route_thru_blks` is changed to Limit or Never (assuming, of course, that the signal is unchanged).
- The `Guide_thru_routes` option actually controls the placement of new unmatched logic. If through-routes are to be guided, the CLB resources used to generate them must not be assigned logic elements during placement. Conversely, if `Guide_thru_routes` is set to None, CLB resources used as through-routes are available for new logic. If new logic is placed there, the original through-route is not guided.

As a general rule, choose a setting for `Route_thru_blks` at the beginning of your design cycle, and change to a less restrictive setting such as OK if you need to improve routing quality. Consider changing `Guide_thru_routes` to a less restrictive setting such as None if you are adding logic to your design and are running short of CLB resources.

Placer_effort \geq 4 May Degrade Designs with 5+ BUFGs

Platform: All
Architecture: XC4000/A/D/E/H
Design Step: Implementation
Reference Number: 16905

If a design uses more than four global buffers, PPR V5.x attempts to place flip-flops such that no more than four different global buffer outputs drive clock pins in any one CLB column. This placement allows all clock pins to be routed directly from the global buffer network.

However, if the `placer_effort` option is set to a value of 4 or greater, the additional placement effort may override the original column assignments determined by PPR. The result may be unrouted clock pins on global buffers. For this reason, it is recommended that `placer_effort` values of 4 or greater not be used for such designs, unless the global buffer loads are properly floorplanned.

The report file generated by XNFPrep (`design.rpt`) gives details of global buffer usage in your design, as well as recommendations for assigning signals to the buffers.

Constraining RPMs via the CST File

Platform: All
Architecture: XC3000/A/L, XC3100A, XC4000/A/D/E/H
Design Step: Implementation
Reference Number: Not Available

In PPR, it is possible to specify the origin of an RPM (RLOC set), or an allowed area for an RPM, in the CST file. The new `place set` constraint provides CST file support for the `RLOC_ORIGIN` and `RLOC_RANGE` schematic parameters introduced in XACT 5.0.

To specify a single origin for an RLOC set (the equivalent of an `RLOC_ORIGIN` parameter), use the following syntax.

```
place set set_name : RnumberCnumber;
```

The `set_name` can be the name of any type of RLOC set: a `U_SET`, an `HU_SET`, or a system-generated `H_SET`. For a list of all RLOC sets in the design, except those generated by XBLOX, consult the `design.mrg` file created by the XNFMerge program.

The origin itself is expressed as a row number and column number, which represents the location of the element(s) at RLOC=R0C0. No CLB_ prefix is used here, as with the RLOC_ORIGIN parameter.

To specify a range or area for an RLOC set (as with an RLOC_RANGE parameter), use the following syntax.

```
place set set_name: RnumberCnumber;
```

As with the place instance constraint, the square brackets indicate a rectangular area. The RLOC set can be placed anywhere within this rectangle. (Of course, the rectangle must be at least as large as the RLOC set being constrained.) As with RLOC_RANGE, a wildcard (*) character can be substituted for either the row number or the column number of BOTH corners of the range.

If a particular RLOC set is constrained by an RLOC_ORIGIN or RLOC_RANGE parameter in the design netlist and is also constrained by a Place Set constraint in the CST file, the CST file constraint overrides the netlist constraint.

Internal Program Error: ...Can't Allocate Memory

Platform: All

Architecture: XC2000/L, XC3000A/L, XC3100A, XC4000/A/D/E/H, XC5200

Design Step: Implementation

Reference Number: 10973

XDE issues the following error if it runs out of memory while trying to load an LCA file.

```
internal program error:... can't allocate memory
```

You can limit the amount of the design in memory at any one time by running XDE with the -p option. This option limits the amount of the design in memory to the size of the screen. See the “XDE” chapter of the *Development System Reference/User Guide* for more information about the -p option.

LCA Files with Unroutes

Platform: All

Architecture: XC2000/L, XC3000/A/L, XC3100A, XC4000/A/D/E/H, XC5200

Design Step: Implementation

Reference Number: 12280

By default, MakeBits does not perform a DRC on the input LCA file. If the input LCA file produced by PPR or APR has unroutes, MakeBits indicates that it has ended normally and creates a BIT file. This BIT file is invalid.

Always check the RPT file — or the OUT file when running XMake — after processing a design to verify that the LCA file is fully routed. To force MakeBits to perform a DRC on your LCA file, select the `-d` option.

Floorplanning

Unexpected Menus May Be Displayed When Using the Ratsnest Dialog

Platform: Windows 3.1/3.11

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 26340

If the Ratsnest dialog is opened and you make no selections, certain menus will become enabled, which ordinarily are disabled unless something is selected.

To remedy this situation, select a macro (or the whole design), then unselect it, using the Unselect All command from the Edit menu.

The Floorplan Window May Scroll Slowly

Platform: Windows 3.1/3.11

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H,
XC5200

Design Step: Floorplanning

Reference Number: 26578

The scrolling speed of the Floorplan window can be quite slow, especially when the Floorplanner is drawing a large number of ratsnest lines. If the ratsnest lines are not needed, then it is best to turn them off while scrolling. If the ratsnest lines are needed, then you can improve the scrolling speed by turning off “direction arrows” in the Ratsnest Options dialog box (accessible by clicking the Options button in the Ratsnest dialog box, which is opened when you invoke the Ratsnest command from the View menu in the Floorplan window.

You can also turn off the graphics resources and/or labels using the appropriate Toolbar buttons to reduce the details in the Floorplan window, which may speed up scrolling.

Online Tutorial Displays Using “Large Fonts” Clip the Screen

Platform: Windows 3.1/3.11

Architecture: Not Available

Design Step: Floorplanner Online Tutorial

Reference Number: 20347

The Floorplanner tutorial was designed to support standard VGA displays using small fonts. Displays using large fonts will clip the screen and make the tutorial unusable.

Make sure you are using small fonts.

The Function Keys Do Not Work When the 'Num Lock' or 'Caps Lock' is On

Platform: Workstations

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H,
XC5200

Design Step: Floorplanning

Reference Number: 17642, 17752

The F function keys are disabled when the Num Lock or Caps Lock keys are on.

In order for the function keys to work the Num Lock and Caps Lock must be turned off.

PPR May Fail Due to Invalid Floorplanner Placement

Platform: All

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 20598, 20599, 20552, 20573, 20574, 20750, 25103, 25546, 25632, 25651

The Floorplanner does not check for all the placement rules; consequently, PPR may fail on a design due to invalid placement that was not caught by the Check Floorplan command.

Check the ppr.log file and/or on-screen messages to determine invalid placement that the Check Floorplan command did not indicate.

Warning 12926 Occurs When Floorplanner Reads a Constraints File That Contains Wild Cards

Platform: All

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 21084

The Floorplanner does not support wild cards in the constraints file. For example, if your CST file has the following entry:

```
place instance li*pd7: p111;
```

The following message will occur:

```
*** FPLAN: WARNING 12926:
Symbol li*pd7 in constraint file was not found
```

Do not use wild cards to specify location constraints in the CST file when floorplanning.

Multiple Periods Are Not Supported in File Names

Platform: Workstations

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H,
XC5200

Design Step: Floorplanning

Reference Number: 22141

If you use multiple periods when saving files in the Floorplanner, the resulting filename may be different.

Do not use more than one period when naming files.

Printing Hangs the System if No Default Printer Selected

Platform: Windows 3.1/3.11

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H,
XC5200

Design Step: Floorplanning

Reference Number: 25481

If no default printer is specified and you try to print, a dialog box displays with the statement, "Printing DESIGN (Starting Document)." Clicking the cancel button causes the mouse to become unresponsive.

Make sure you have a default printer selected before trying to print.

The Floorplanner Will Not Load a File from a Directory that Only Has Group Write Permission

Platform: Workstation

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H,
XC5200

Design Step: Floorplanning

Reference Number: 25490

The user running the Floorplanner must have user-write permission for the Floorplanner to function. Having group write permission for the design directory is not sufficient.

Ensure that the user has user-write permission to the design directory.

Saving a File to a Write-Protected Floppy Results in a System Error

Platform: Windows 3.1/3.11

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 26051

If you issue a Save command to a write-protected floppy disk you will not get a message dialog stating that the diskette is write-protected. Instead, you will get a system error dialog with a cancel button and a retry button.

You should eject the floppy disk, change the write protect tab to enable writing, re-insert the floppy disk, then select the retry button.

Page Fault May Be Caused by Having 32-bit File Access Turned On

Platform: Windows 3.1/3.11

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 26198

32-bit file access is an option supplied with Windows for Workgroups 3.11. To access this option, open the Control Panel window, and click on the Enhanced icon. Click the Virtual Memory button on the Enhanced dialog box, then click the Change button on the Virtual Memory dialog box.

If the Floorplanner crashes and the following message is displayed, you should try turning off the 32-bit file access if it is currently on.

```
FPLAN caused a page fault in module <unknown>
```

The Floorplanner Does Not Optimally Place Counter Macros

Platform: All

Architecture: XC3000/A/L, XC3100/A/L, XC4000/A/D/E/H, XC5200

Design Step: Floorplanning

Reference Number: 25157

Note: RPM counters are placed optimally by the Floorplanner.

When you drop a macro into the Floorplan window, the Floorplanner automatically places the symbols of the macro beginning at the top of the Design window. It drops the function generators in contiguous positions until all function generators of the macro have been placed. It also drops the flip flops in contiguous positions until all flip flops of the macro have been placed. The best placement for these macros is to have the flip flop and its sourcing function generator placed next to each other in the same CLB.

This does not always happen if you just drop the whole macro into the Floorplan window. Unless the counter is an RPM, it is better to drop individually, the sub-components of the counter.

Select the macro that you want to place, then use the Group by command to make groups of function generators to flip-flop pairs. Then place each new group, one at a time in a column, to ensure optimal placement.

Simulation File Creation

IFD Hold and Delay on D Pin Are Not Modeled Correctly for Simulation

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E

Design Step: Simulation File Creation

Reference Number: 14681

The hold requirement for the XC3000 and XC4000 input flip-flop is not modeled correctly. Although *The Programmable Logic Data Book* guarantees zero external hold time if the global clock distribution is used, timing simulation requires a non-zero hold time. The hold time between the device pad and the flip-flop clock input is negative, but since most simulators cannot support negative hold times, it is set to zero. The external hold time becomes positive.

In addition, the delay between the device pad and the flip-flop D-pin is not modeled. Therefore, if the data on the pad changes between the external clock edge and the clock at the flip-flop input pin, simulation shows the new data being clocked into the flip-flop.

In order to determine whether or not there is a true violation, compare the timing of the device input signals against the parameters

published in *The Programmable Logic Data Book*. For XC4000 family devices, use the guaranteed pin-to-pin parameters.

The missing delay in the input path is most likely to cause problems in board-level simulation. In this case, add an extra delay buffer at the board level, going into the device inputs. A delay the same as or larger than the delay on the clock input path should be sufficient to eliminate the false clocking of data. To determine this delay, use XDelay's -ClockInput option, or consult *The Programmable Logic Data Book* for global clock buffer delays.

LCA2XNF -v Option Is Not Supported

Platform: All

Architecture: XC4000

Design Step: Simulation File Creation

Reference Number: 26129

XNFBA cannot back-annotate XC4000 designs with carry logic when you run LCA2XNF with the -v option. There are no symbols for the XC4000 carry logic in the pre-unified library XNF. The carry logic is replicated in gates when LCA2XNF -v is run, but XNFBA cannot determine the symbols to which it delays should be assigned.

Timing Analysis

The Timing Analyzer Show Settings Window Does Not Always Push to the Top

Platform: Windows 3.1/3.11

Architecture: All

Design Step: Timing Analysis

Reference Number: 23408

In the Timing Analyzer the Show Settings window will not push through to the top if another timing report window is opened full screen.

Minimize or close the windows that are not in use and or select the Show Settings window from the "window" selection in the command bar.

XDelay/Timing Analyzer Reported Setup Value on Carry Logic Path Appears Erroneous

Platform: All
Architecture: XC4000/A/D/E/H
Design Step: Timing Analysis
Reference Number: 24282

It is possible for XDelay and Timing Analyzer to report setup delays along a carry logic path which appear to be larger than the guaranteed values in the Data Book. An example is a carry-in (CIN) signal which enters a CLB on the F1 pin and feeds the CLB flip-flop data pin. The Data Book indicates that the setup time from F/G inputs should be 4.5nS (Tick). However, in this example, XDelay and Timing Analyzer reports a setup time of 9.5nS:

Thru: Net SA6 to CLB_R3C4.F1 : 1.7ns (22.9ns)
To: FF Setup (D), Blk Q6 : 9.5ns (32.4ns)

The Tick value of 4.5nS indicated in the Data Book refers to the setup time from an F pin to FFX, or from a G pin to FFY. However, the 9.5nS value reported refers to the setup time from the F1 pin, through the carry-logic generator, through the G function generator, to FFY. Although XDelay and Timing Analyzer does not report the details of this path, the reported setup value is accurate (9.5nS in this example).

XDelay/Timing Analyzer Does Not Accept Valid -ToIOB Option from Template File

Platform: All
Architecture: All
Design Step: Timing Analysis
Reference Number: 21821

After reading in a valid timing analysis template file (XTM), XDelay/Timing Analyzer issues the following error:

```
abc.xtm line 58: XDelay -ToIOB U16
`' (U16): not a valid output IOB.
Missing output IOB.
```

There are two possible work arounds:

- From within the XDelay/Timing Analyzer, manually select the -ToIOB pins which are causing the errors. Manually selecting the pins should avoid the problem. If you still encounter the error,

then most likely the error is correct and you should verify that the pin name you selected is a valid endpoint.

- Edit the XTM template file and replace the package pin names which are causing errors with the die pad names. To determine the die pad name, use the package data file for the device located in the XACT/DATA directory. For example, the package data file 5206g191.pkg indicates that pin U16 for the XC5206PG191 corresponds to die pad pad111. Change the line in the template file from “XDelay -ToIOB U16” to “XDelay -ToIOB pad111.”

Printing World in XACT Causes OpenWin to Crash

Platform: Sun4

Architecture: All

Design Step: Design Entry/Timing Analysis

Reference Number: 20407

There is a bug in OpenWin that causes Print World from XACT to crash the X server, killing XACT and all other windows. Reports indicate OpenWin2.0 is more susceptible to this problem than OpenWin3.0. However, this problem has also been seen with OpenWin3.0 when printing larger designs (XC4010 and larger).

No work around is available.

-Maxpaths Is Ignored when Performing TimeSpec Analysis; Use -TSMmaxpaths

Platform: All

Architecture: All

Design Step: Timing Analysis

Reference Number: 25999

When performing an XDelay-TimeSpec analysis on a design, the -Maxpaths option is ignored. Setting a value for this option has no effect on the analysis. The -Maxpaths options is only valid for non-TimeSpec mode analysis.

The method of limiting the number of paths reported for each TimeSpec in the XDelay report is to use the -TSMmaxpaths option.

Delay from T Pin to Stable Long Line May Be Longer Than Reported

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Design Step: Timing Analysis

Reference Number: 16865

In certain rare cases, the delay from the BUFT T pin to a stable longline logic level may be longer than reported by XDelay. These cases occur only if your design meets the following criteria:

- Contains a longline being driven by non-wired-AND BUFTs
- Relies on pull-up resistors to provide a logic level High on the longline when no BUFTs are actively driving the longline

A BUFT is in a wired-AND configuration if the I input of the BUFT is tied to GND or to the same source as the T input. If the longlines in your design contain wired-AND BUFTs, XDelay reports the delays through BUFTs correctly and this problem is not an issue for your design.

However, if your design meets the two aforementioned criteria, XDelay will report a delay through the BUFT that is too optimistic. The reason is that on a longline with non-wired-AND BUFTs, XDelay assumes that the logic level on the longline is always actively driven by a BUFT. For most applications, this is correct and the XDelay report is valid. However, if your design contains states where there is no BUFT driving the longline and it relies on the pull-up resistor to switch the logic level on the longline from Low to High, the calculated delay will be too optimistic. The parameter that XDelay should be using is T_{puf} or T_{pus}, but it uses T_{on} instead, which is incorrect.

For reference, the four parameters that describe the delay from the T pin of a BUFT to its O pin are described in *The Programmable Logic Data Book*, p.2-50, p.2-156, and p.2-180.

- T_{on}: T going Low to longline going from resistive High to driving active-Low.
- T_{off}: T going High to BUFT going 3-state.
- T_{pus}: T going High to longline going from Low to High, pulled by a single resistor.

- T_{puf}: T going High to longline going from Low to High, pulled by two resistors.

T_{puf} should almost always be used instead of T_{on} whenever the logic-High output signal is provided by the pull-up resistor. T_{pus} should be used instead of T_{puf} whenever there is only one pull-up on a longline running the full width of the chip. This situation only occurs after the design is edited in XDE to only have one pull-up on a whole longline.

Correlating Delays Through BUFTs with Data Book Values

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Design Step: Timing Analysis

Reference Number: 16865

At first glance, it appears that the delays through BUFTs as reported by XDelay do not correspond with those in the data book. They do. The confusion stems from the fact that XDelay lumps part of the delay through the BUFT into the routing delay through the longline.

For example, the following sample XDelay report seems to indicate that the delay from the T to the O pin of the BUFT is only 5.3 ns, while T_{on} for this XC4013 example should be 12.6 ns.

```
From: Blk P109 PADto P109.I2 : 3.0ns ( 3.0ns)
Thru: Net enableto TBUF_R24C24.1.T :18.8ns ( 21.8ns)
Thru: Blk TBUF_R24C24.1to TBUF_R24C24.1.O : 5.3ns \
( 27.1ns)
Thru: Net long0 to P46.O : 8.4ns ( 35.5ns)
To: O pin to PAD, Blk P46 : 7.0ns ( 42.5ns)
```

The total delay from this BUFT T pin to the pad is $5.3 + 8.4 = 13.7$ ns which accounts for (T_{on} + Routing on the longline) = $(12.6 + 1.1) = 13.7$ ns.

Does Not Read IGNORE TimeSpecs from PPR

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Design Step: Timing Analysis

Reference Number: Not Available

An XACT-Performance attribute with a value of IGNORE tells PPR not to analyze paths through the specified connections. However, the IGNORE Timespec information is not passed to XDelay, while all explicitly specifications are. Additionally, PPR does not analyze delays through combinatorial loops. Therefore, XDelay might analyze paths that were ignored by PPR.

Use the XDelay Ignorenet option to specify nets that you do not want traced. XDelay does not support partial net suppression, such as the tracing through some load pins of a net but not others.

Analyze Mode Does Not Account for Clock Skew

Platform: All

Architecture: XC2000/L, XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Design Step: Timing Analysis

Reference Number: 5211

The XDelay Analyze mode reports a minimum period for each clock signal. However, the analysis of clock-to-setup paths does not take clock skew into account. The minimum period reported by XDelay assumes that there is no skew between clock pins.

For a clock signal distributed on a global clock network (BUFG, GCLK, or ACLK in XC2000 and XC3000 devices; BUFG, BUFGP, or BUFGS in XC4000 devices) the skew between clock pins is very small. However, if a clock signal is not distributed on a global clock network, the skew between clock pins can be significant. In either case, use the Clock Input option of XDelay to determine the worst-case skew between clock pins and add this skew to the minimum clock period reported by using Analyze.

OUTFF Feeding INFF in an Unbonded IOB Not Included in Clock-to-Setup Analysis

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E

Design Step: Timing Analysis

Reference Number: 19396

An OUTFF sourcing an INFF in an unbonded IOB can be used to achieve a two clock cycle delay on a signal without using CLB

resources. XDelay does not report Clock-To-Setup delays from OUTF to INFF in the UPAD.

All necessary data is available in *The Programmable Logic Data Book* to manually confirm whether the path will run at the desired speed.

Configuration

Tie Option Accepted through Implementation Template but Not Configuration Template

Platform: PC
Architecture: All
Design Step: Configuration
Reference Number: 28256

In order to tie a placed and routed design, a custom template has to be created with the MakeBits -t option. The MakeBits -t options is only accepted through a customized Implementation Template; it is not accepted through the Configuration Template.

To customize a template for tie, from the Design Manager, click on Utilities → Template Manager → (Select Templates: Implementation) → Select a template) → Customize and then type makebits -t in the dialog box.

Downloading, Configuration, and Verification

MakeBits Should Configure TTL Inputs by Default

Platform: All
Architecture: XC4000E
Design Step: Downloading and Configuration
Reference Number: 27400

When invoked from the command line, MakeBits configures CMOS input levels for all IOBs by default. This problem does not occur if MakeBits is invoked from XDE. The work around is to invoke MakeBits with the following -f configuration option:

```
makebits -f input:TTL
```


Help Button in the New Group Name Dialog Does Not Invoke Help

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 26434

Clicking on the New button in the Signal Groups dialog opens the New Group Name dialog. Clicking on the Help button in the New Group Name dialog does not invoke the Hardware Debugger online help file.

To invoke help on creating signal groups, use the Help button in the Signal Groups dialog.

Hardware Debugger May Issue an EMM386 Error or Hang on Invocation

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Numbers: 26195 and 26450

On some machines, the Hardware Debugger may give an EMM386 error or simply hang when it is invoked. On some machines this behavior may be due to an out-of-date serial port driver called SERIAL.386 found in the Windows for Workgroups SYSTEM sub-directory.

Make sure that the target board and download cable is connected and powered before invoking the Hardware Debugger.

XChecker Confuses Mouse for XChecker Cable

Platform: All

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 16772

The XChecker software can confuse a Logitech Mouseman Serial Port mouse for the XChecker cable.

If this situation prevents downloading, you may need to swap the serial port connections of the mouse and XChecker cable.

Logic Level of Pins Command Is Not a Continuous Probe

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 19918

The Cable command Logic Level of Pins is not a continuous probe. The Logic Level of Pins command probes the cable pins and then displays the values. If the logic levels change, the dialog that displays the values will not be updated.

To re-probe the cable pins, re-select the Logic Level of Pins command from the Cable menu.

Cannot Delete a Group from the Signal Groups Dialog Box

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 20219

Once a group is added to the display list using the Display Signals dialog, it cannot be deleted.

To delete a group, remove it from the display list by removing it from the Displayed Signals list box in the Display Signals dialog. The Display Signals dialog can be opened by clicking on Display in the Control Panel, or by selecting the Settings->Display Signals command from the Debug menu.

Viewing Waveforms Textually Prohibits Copying Snapshots and Signals

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 20222

When viewing a waveform window as text, the various snapshots and signals cannot be selected for copying.

Save the waveform window by selecting the Save Readback command from the File menu. Then open the waveform.txt text file using Notepad or another editor.

Cannot Modify a Group Using the Signal Group Command

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 20227

You cannot modify a group using the Signal Groups dialog.

Once you add a group to the display list using the Display Signals dialog, you cannot add nor remove signals.

To modify a group, remove it from the display list by removing it from the Displayed Signals list box in the Display Signals dialog. The Display Signals dialog can be opened by clicking on Display in the Control Panel, or by selecting the Settings, Display Signals command from the Debug menu. Once the group is no longer a member of the display list, use the Signal Groups dialog to add or remove signals. When the desired signals have been added or removed, add the group back to the display list using the Display Signals dialog.

Help is Disabled if Help File is on a Network Drive

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 20367

If the XACTstep installation is located on a network drive, the Hardware Debugger will be unable to load the help file “hwdebugr.hlp.”

To access help from the Hardware Debugger, create a local XACT directory with a sub-directory DATA. Copy the file “hwdebugr.hlp” from the network XACT\DATA directory to the local XACT\DATA directory. Then, so that the Hardware Debugger will know to locate the file locally, modify the XACT environment variable to include the new local directory.

Example XACT setting:

```
SET XACT=E:\TOOLS\XACT;C:\XACT
```

Where E:\ is the network installation drive and C:\ is the local drive.

Printing a Graphic Waveform Using the Landscape Orientation Does Not Rotate the Waveform

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 20741

When trying to print a waveform using the Landscape setting of the Printer Setup dialog, the Hardware Debugger may not actually rotate the waveform display correctly.

This behavior only happens when using some print drivers. Changing Windows print drivers may fix the problem. Otherwise, print the desired waveform using the Portrait setting and zooming into the various regions to be printed.

Once a Signal or Group Is Selected in a Graphic Waveform, It Cannot Be Deselected

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 21070

Once a signal or group is selected in a graphical waveform, it cannot be unselected.

To de-select a signal or group, select the Move command from the View menu and specify the current location of the signal or group. The signal or group will be de-selected, and reside in the same location.

Double-clicking on the Close Box in a Window Title Bar Does Not Close the Window

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 21072

If one of the windows in the Hardware debugger is full screen, it cannot be closed by double-clicking on the close box in the window's title bar.

To close a window, first reduce the window so that it is not full screen and then double-click on the close box in the window's title bar. A full screen window can also be closed by selecting the Close command from the close box menu.

Nets That Have Been Split during Implementation Appear as Split Nets in the Available Signals List Box

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 21565

Split nets are nets that are created when the implementation software needs to route a particular net from one source to multiple loads and uses CLBs to split the original net creating several “source” connections. When split nets are created, all the nets will appear in the available signals list boxes.

When split nets are displayed in the available signals list box, any one of the nets can be chosen to be displayed in a waveform or used to create a group. Typically, the smallest split net should be chosen. When the design is re-implemented, the split nets chosen may need to be added again, to the display list or to any groups which reference them.

Time-out After X Seconds Option in Trigger Settings Dialog Is Only for External Triggers

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Configuration and Verification

Reference Number: 21835

The Time-out After X Seconds option in the Synchronous Trigger Settings dialog can only be used when the Trigger On pull-down list box is set to External.

To use the Time-out After X Seconds option, set the Trigger On option to External.

Clicking on No in the Press Enter to Start Readback Dialog Box Displays Failed Readback Message

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 21835

When the Trigger On option in the Synchronous Trigger Settings is set to the Enter Key and a readback is issued, a dialog is displayed that says to press Enter to start the readback. If No is selected, a message stating that the readback failed is displayed.

The readback failed message can be ignored.

Selecting the Print Command from the File Menu without Having a Printer Installed Gives an Internal Warning

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22151

If the Print command is selected when a printer is not installed, an XVT warning will be displayed.

Ignore the warning, install a printer, and select the Print command again to print the desired waveform.

The Hardware Debugger Can Crash if Too Many Waveform Windows Are Opened at Once

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22262

Depending on the system, opening too many waveform windows can cause the Hardware Debugger to crash.

The following internal error is displayed:

```
NULL handle.  
Category : Invalid Argument [Null Handle]  
Function : xvt_menu_set_free  
           xvt_win_create  
           xvt_app_create  
File: wmenu.c line:781
```

Re-start Windows and the Hardware Debugger. As you work in the Debugger, save the session by saving the Console commands to a macro file. Should the problem occur again, a macro script will exist so that work will not be lost.

Once a Macro Has Been Issued, It Cannot be Interrupted

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22365

When running a macro, either by selecting the Run Macro command from the File menu, or clicking on the Run macro toolbar icon with a macro in focus, there is no way to stop the macro.

To run a macro in stages, break the macro into multiple sub-macros. Then run each sub-macro individually.

When a Macro is Saved, Invalid Macro Commands Are Not Flagged

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22612

When saving a macro, all commands are saved, whether they are correct or incorrect. This will result in errors when the macro is opened and run.

Correct any errors before saving or running a macro.

Non-consecutive Lines in the Console Window Can Not Be Selected Using the CTRL Key

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22613

Holding down the CTRL key while selecting lines in the Console window with the left mouse button does not select non-consecutive lines.

To copy non-consecutive lines from the Console to a macro or other destination, copy each line individually.

Printing Only Prints the Currently Displayed Waveform Portions

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, +XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 22937

When a graphical waveform is printed, only the section of the waveforms that appear in the display are printed.

To print an entire waveform, zoom to full and print. If the resulting printed waveform is too small to read, perform several prints, zooming into sections of the waveforms.

Clicking on the Run Macro Toolbar Icon Generates an Error if a Macro is not in Focus

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 23105

If a macro is not the active window, the Run macro toolbar icon can be selected and will result in an error.

Select the desired macro to be run before clicking on the Run macro toolbar icon.

Console and Macro Windows Can Not Be Printed from the Hardware Debugger

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 24230 and 24231

You cannot print the Console or Macro windows from the Hardware Debugger.

To print the contents of the Console, open a new macro, copy the Console contents to the new macro, save the macro, and then open and print the macro text file using Notepad or another text editor.

More than 500 Snapshots Will Not Be Displayed

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 24737

When reading back from a programmed device, no more than 500 snapshots can be displayed in any one waveform window.

To capture more than 500 snapshots, capture a portion and then open a new waveform window. Opening a new waveform window will detach the first windows from the readback stream and connect the new waveform. All snapshots captured will be displayed in the new waveform window.

An Empty Readback Text File Is Created if There Is Insufficient Disk Space

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 24957

A readback text file (.rdb) of 0k bytes will be created if there is not enough disk space.

Free up an appropriate amount of disk space and re-save the read-back data.

Textually Saved Waveforms Cannot Be Re-opened into the Hardware Debugger

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 25013

Waveforms that are displayed in text format and are then saved can not be re-loaded into the Hardware Debugger.

If a waveform is to be re-loaded into the Hardware Debugger, save the waveform when it is displayed graphically.

Can Not Download Using the Hardware Debugger if Running from an Executable CD-ROM

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 25055 and 25408

If the Hardware Debugger is running off an executable CD-ROM, the working directory must be pointing to a directory other than the CD-ROM. The Hardware Debugger uses the working directory to write out temporary files and so the working directory cannot be set a CD-ROM.

Change the Working Directory setting in the Program Item Properties dialog invoked from the Windows Program Manager by selecting the Properties command from the File menu. The new setting should be a writable directory that contains a copy of the hwdebugr.ini file.

The Hardware Debugger Can Not Readback at 9600 Baud on Some Machines

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 25672

The Hardware Debugger cannot readback at 9600 baud on some machines. On some systems, the Hardware Debugger cannot read-back or verify a device at 9600 baud.

Set the Baud rate to either 19200 or 38400 using the Cable Communications dialog.

The First Read-back Attempt May Fail after a Verify Has Been Performed in the Middle of Several Read Backs

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 26232

The first readback attempt may fail after a verify has been performed in the middle of several read backs. If several read backs are performed, and then the device being read back is verified, the next readback may fail.

Should a readback fail, re-issue the readback command by clicking on the Read button in the Control Panel or selecting the Read FPGA command from the Debug menu.

The Save Readback Command in the File menu Is De-activated When a Waveform is Minimized

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: None

The Save Readback command in the File menu is de-activated when a waveform is minimized.

To save a waveform window as readback data, click on the Save Readback toolbar icon. The Save Readback toolbar icon will open the Save Readback dialog which can then be used to save the waveform window.

Text Waveforms Cannot Be Printed from the Hardware Debugger

Platform: Windows 3.1/3.11

Architecture: XC2000/L, XC3000/A/L, XC3100/A, XC4000/A/D/E/H, XC5200

Design Step: Downloading and Verification

Reference Number: 26355

Text waveforms cannot be printed from the Hardware Debugger.

This behavior only occurs when using some print drivers. Changing Windows print drivers may fix the problem. Otherwise, to print a text waveform, save the waveform to a waveform.txt file and then open and print the waveform.txt text file using Notepad or another text editor.

Warning 001 Is Misleading

Platform: PC

Architecture: XC2000/L, XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Design Step: Downloading and Verification

Reference Number: Not Available

When executing a Verify operation, XChecker might report the following warning.

```
WARNING 001: Current design must have  
ReadCapture set to Enable.  
Snapshot readback is incorrect.
```

In spite of this warning, XChecker can still verify the bitstream. The message indicates that the data portion of the readback bitstream (snapshot) cannot be read. However, the configuration information was in fact read and verified against the original data.

To enable readback of the data and generate a snapshot with both valid data and valid configuration information, regenerate the bitstream using the Makebits option `-f readcapture:enable`. From the system prompt, type `makebits -f readcapture:enable design.l`, or select the option from the XDM menu.

XC2000 Bit Streams May Have Pin Conflicts in Peripheral Mode

Platform: All

Architecture: XC2000L

Design Step: Downloading and Verification

Reference Number: 15785

If user outputs are placed in IOBs corresponding to the device pins CS0, CS1, CS2, or WRT, conflicts may occur in configuration if config-

uring in peripheral mode. These outputs can be assigned by the user or automatically by APR.

The problem can arise because XC2000 family devices require two additional CCLKs after the configuration bit stream is read in before their DONE pins go HIGH. On the first extra CCLK, the device's IOBs go active, and on the second CCLK, the DONE pin goes HIGH and the internal GLOBALRESET net is released. However, when the first CCLK activates the IOBs, the user outputs can override the external conditions applied to the CS0, CS1, CS2, and WRT pins. This situation occurs when these IOBs are configured as outputs and their reset states, which exist while GLOBALRESET is active, conflict with the externally applied states.

If this conflict occurs, the external device attempting to configure the part can no longer put the correct combination of HIGHs and LOWs on the CS0, CS1, CS2, and WRT pins and enable the final CCLK. Without the last CCLK, the DONE pin does not go HIGH and the internal GLOBALRESET net remains active.

To avoid this situation, always verify that the CS0, CS1, CS2, and WRT pins are not programmed as user outputs when configuring in peripheral mode.

Corrupted .il Files On CD-ROM

Platform: ALL

Architecture: ALL

Design Step: Downloading and Verification

Reference Number: 27426

Downloading via XChecker with the verify option selected produces a message stating that MISMATCHES have occurred during readback after configuring the LCA. This is due to old .il files in the installed area. These data files were not generated with the current MakeBits program. Use one of the following options as a work around.

- Run MakeBits -makell=part#, which creates a new .il file in the current working directory. Then use XChecker to download and verify the download.
- Run MakeBits -makell=all, which creates a complete set of .il files that can be copied to the \$XACT data area so you need not worry about running Makell to verify the download.

CAE Tools

Cadence

Negative Timing Delay Errors on Designs Containing XC4000E Synchronous and Dual-Port RAMs

Platform: All

Architecture: XC4000E

Design Step: Timing Simulation

Reference Number: Not Available

Because negative delay values are used in the modeling of the WCLK pin-to-output block delays in ram16x1s, ram32x1x, and ram16x1d (XC4000E Synchronous and Dual-Port RAM primitives), you must invoke Verilog-XL with two additional options, +neg_tchk and +splitsuh. If these options are not used, XNF2VERILOG issues error messages about delays being negative or too large. Unfortunately, Version 2.2.1 of Verilog-XL on the Sun4 platform will core dump when the +neg_tchk option is specified.

Users on Sun4 platforms should install the Verilog-XL Version 2.2.8 hot fix to correct this problem. The Verilog-XL patch is available in both configurable and non-configurable versions from the Xilinx ftp site, [ftp.xilinx.com](ftp://ftp.xilinx.com). If only the non-configurable executable is required, download

```
verilog2.28sun4.t.Z.uu
```

If you need to be able to configure your Verilog executable or link to PLI routines, download these two files:

```
vconfig03.23-p007sun4.t.Z.uu
```

```
verilogx102.20-s018sun4.t.Z.uu
```

These Cadence Verilog-XL archives outlined above are all compressed, uuencoded tar files and are available in the customer download area of [ftp.xilinx.com](ftp://ftp.xilinx.com). Log in as “customer” with the password “xilinx” to access this area:

```
ftp ftp.xilinx.com
```

```
login: customer
```

```
password: xilinx
```

```
cd download
```

```
get filename
```

Please note that this is a blind area, so you will not be able to see a listing of the available files. To extract the archives:

```
cd install_dir
```

XC5200 OSC52/OSC5 Behavior Can Not Be Simulated Using the Verilog Library Model

Platform: All

Architecture: XC5200

Design Step: Functional and Timing Simulation

Reference Number: Not Available

OSC52/OSC5 behavior currently cannot be simulated using the Verilog library model. If you are using either form of the XC5200 oscillator in your design, you must force it in your stimulus or test bench.

Pulse Width Checks on the CLK Signal Should Be Performed for Both CLock Hlgh and Clock Low Times

Platform: All

Architecture: XC4000E

Design Step: Timing Simulation

Reference Number: 27390

On the CLK signal, pulse width checks should be performed for both High and Low periods of the clock signal. Currently, the check is only done when the clock is High, as indicated in the width record of the .sdf file, at the last line of the excerpt below:

```
(CELL
    (CELLTYPE "ram16x1s")
    (INSTANCE Nram_out_7_)
    (DELAY (ABSOLUTE
        .
        .
        .
```



```
(TIMINGCHECK
    (SETUPHOLD a0 (posedge wclk) ((2.4)) ((0.0)))
.
.
.
(WIDTH (posedge wclk) (7.2))))
```

XNF2Verilog Error: Symbol Does Not Have Corresponding Entry in the PIN File

Platform: All

Architecture: All

Design Step: Functional or Timing Simulation File Creation

Reference Number: Not Available

XNF2Verilog Error:

ERROR: The following symbol(s) were found in the design, but do not have corresponding entries in the PIN file:

If the problem is with a DFF, you will see something similar to this:

Symbol *name* does not have a corresponding entry in the PIN file:

```
Symbol QOUT_REG<9> (type DFF)
```

```
Symbol QOUT_REG<8> (type DFF)
```

```
Symbol QOUT_REG<7> (type DFF)
```

```
Symbol QOUT_REG<6> (type DFF)
```

The pin file that the error message refers to is a Verilog-XL pin file, which lists the symbol pins for every element in the Verilog primitive library for that architecture. Pin files are named xc2000.pin, xc3000.pin, xc4000.pin, etc., and are located in *install_dir*/data.

The error message means that XNF2VERILOG cannot find a matching entry in the Verilog-XL pin file for the particular symbol (say, an AND7) in the input XNF file.

Very often this error is issued when XNF2VERILOG cannot resolve certain primitives found in a post-synthesis, pre-routed Synopsys XNF file. The error may also be the result of improperly processing the netlist (skipping X2VPREP).

In the case of post-synthesis Synopsys XNF, the XNF file generated by Synopsys contains modules such as BUFG_F, AND7, etc., for example, that are not standard Xilinx Unified library simulation primitives. These modules may be present in a pre-route XNF generated by Synopsys or other HDL synthesis tool. They are also restored to the XNF file when you run XNFBA as part of a timing simulation flow on a Synopsys design.

For Functional Simulation

Pre-route, post-synthesis functional simulation of Synopsys designs is currently not supported by the Verilog interface. As a work around, you can simulate the design after allowing PPR to flatten it, skipping the routing stage. Since the routing stage is skipped, no routing delay information is produced.

The suggested modified flow for post-synthesis functional simulation is:

```
syn2xnf
xnfprep
ppr design route=false placer_effort=1
timenetx design xc4000 -x
```

Furthermore, by default, Verilog-XL assumes zero delays in the absence of a .sdf file with non-zero timing delays. To get a unit delay simulation rather than zero delay simulation, you must run Verilog-XL with a +delay_mode_unit option:

```
verilog +delay_mode_unit designt.v designt.stim
```

For Timing Simulation

Specify the -x option when running timenetx to skip XNFBA. Note that Version 5.2.1a of timenetx automatically determines that a design has been generated using Synopsys if the associated XFF file resides in the working directory.

For Functional or Timing Simulation

Another common cause of this error is trying to process the XNF file directly using XNF2VERILOG. Preprocessing by X2VPREP is a required step.

The easiest way to ensure that the correct flow is used is to process the design using one of the following scripts, which are included in the interface:

Functional simulation: funcnetx

Timing simulation: timenetx

Cadence Verilog-XL: Driving GSR, GR and GTS in Verilog Simulation

Platform: All

Architecture: XC3000, XC4000, XC4000E, XC5200

Design Step: Functional or Timing Simulation

Reference Number: Not Available

GSR (XC4000 devices), GR (XC5200 and XC3000 devices), and GTS (XC4000 and XC5200 devices) are defined as wires, typically at the end of the .v Verilog source file generated by XNF2VERILOG. They are declared in a global module called *design_globals*. These signals are internal to the device and do not appear in the module port declaration.

To drive these signals in a Verilog simulation, you need to use the Force command, and reference the signals as *global_module.signal_name*:

```
force design_name_globals.[gsr, gr, gts] = [0,1];
```

Example:

```
force calct_globals.gsr=1;
```

Here, calc is the design name, calct_globals is the name of the global module for the timing simulation netlist, and the signal being driven is GSR.

XNF2VERILOG V9502-1.21G ERROR: 'Could not find primitive...does_pin_have

Platform: All

Architecture: All

Design Step: Functional or Timing Simulation File Creation

Reference Number: Not Available

XNF2VERILOG may issue errors of this nature when reading the Verilog pin file:

```
checking XNF file contents...

Reading pin file /tools/xact/share/library/xilinx/
data/xc4000.pin...

Checking pin file contents...

ERROR: Could not find primitive NAND2, pin 1 in
does_pin_have_delay

ERROR: Could not find primitive NAND2, pin 2 in
does_pin_have_delay

ERROR: Could not find primitive NAND2, pin 1 in
does_pin_have_delay

.

.

.
```

XNF2VERILOG is flagging mismatches between the pin names for the symbols found in the XNF file and pin names for this symbol in the Verilog pin file it reads. There is a separate .pin file for each Xilinx architecture (xc2000.pin, xc3000.pin, xc4000.pin, etc.), located in the *install_dir*/data directory.

One possible cause is an error in the Verilog pin file (missing pin records, etc.). Another possible cause is that the XNF netlist version of the XNF file being processed is incompatible with the version of the interface being used.

Between XACT 4.X and XACT 5.X, there was a change in pin naming conventions for combinational logic gates. In XNF version 4, the convention for naming combinational gate symbol pins was to use numbers only for the pin names:

PIN,1,I

PIN,2,I;

etc.

In XNF 5.0, the naming convention was changed to require an “I” prefix to the pin name:

PIN, I1, I;

PIN, I2, I

etc.

The Verilog pin files and library primitives in the 9502 Cadence release follow the XNF 5.0 naming convention. Hence, the 9502 pin files and a version 4 XNF netlist would not be compatible.

You are likely to see this problem if you run LCA2XNF with the -V option to generate a version 4.0 XNF netlist, then try to process this netlist with XNF2VERILOG 9502 or later.

Check the LCANET version record in the routed XNF file to determine whether it is a version 4 or 5 netlist. If it is a version 4 netlist (LCANET, 4) and you are running LCA2XNF with the -v option, re-run LCA2XNF without the -v option. If it is a 3rd party tool (Exemplar, for example) that wrote out the version 4 XNF file, contact the vendor to see if they have an update that supports LCANET 5.

Some Xilinx Unified Library Components Renamed

Platform: All

Architecture: All

Design Step: Schematic and Simulation Libraries

Reference Number: Not Available

A number of the Xilinx Unified Library components are renamed in the Concept and Verilog libraries to avoid conflict with pre-defined Verilog primitive names:

Component name in Xilinx Verilog	Avoids conflict with this Verilog library primitive component
pulldown1	pulldown
pullup1	pullup
buff	buf

Primitives with Underscore Ones (“_1”) in the Unified Library for Verilog Have Been Renamed

Platform: All

Architecture: XCX4000, XC4000E

Design Step: Simulation Libraries

Reference Number: Not Available

Primitives with underscore ones (“_1”) in the Unified Library for Verilog have been renamed in the Verilog library by removing the underscore.

The reason for this is that Vloglink takes the SIZE property in a Cadence Concept library component and attaches “_SIZE” to the name of the primitive. This could cause a name collision with the corresponding component called “component_1” if SIZE = 1.

For example, an ild instance in Concept with a size of 1 would be renamed by Vloglink to “ild_1”, and this could cause a name collision with an ild_1 instance in the same design.

The following XC4000 primitives have been renamed:

Xilinx Component Name in Libraries Guide	Verilog Library Component
ild_1	ild1
ildi_1	ildi1

The following XC4000E primitive have been renamed:

Xilinx Component Name in Libraries Guide	Verilog Library Component
ildx_1	ildx1
ildxi_1	ildxi1

Verilog-XL: How to Handle Upper/Lower Case Conversion of Verilog Signal Names

Platform: All

Architecture: All

Design Step: Timing Simulation

Reference Number: Not Available

Users may find that the Verilog-XL simulator is unable to recognize signal names that they declare in their original, Verilog behavioral description and test bench files when they attempt to simulate their designs after the routing phase.

Often this is because the case of the signal and instance names in the original test bench file and the synthesized design netlist do not match.

The problem is often seen in designs done in Synopsys, when the user declares signal names in lower case in the original Verilog source description. The Synopsys tools, and the Xilinx programs SYN2XNF,

and XNFMERGE all preserve the case of signal names. However, if Synopsys happens to target X-BLOX modules in the design, X-BLOX will convert the lower case names to upper case in the output netlist. The upper case names are preserved for the remainder of the implementation process, all the way up to the generation of the Verilog functional or timing simulation netlist.

As a result, if the user tries to use the same test bench for post-synthesis simulation that was used for behavioral simulation, and this test bench has signals all in lower case, Verilog will not be able to match any of the signals and symbol names in the test bench with the names in the design netlist because of its case-sensitive nature.

The best solution is to use only UPPER CASE for signal and instance names in the behavioral Verilog netlist from the start to avoid these types of problems.

If a design does contain mixed case or lower case names, use the following Unix command to make the case of all names consistent:

```
dd conv={ucase,lc case} {input file} {output file}
```

Example: To convert all upper case names to lower case:

```
dd conv=lc case oldfile.v newfile.v
```

where *oldfile.v* is the input file and *newfile.v* is the output file.

Note that the conversion must be done on both the .v and the corresponding .sdf files.

Functional Simulation of Pre-Route, Post-Synthesis XNF Netlists from Synopsys (Improved Work Around)

Platform: All

Architecture: All

Design Step: Functional Simulation

Reference Number: Not Available

Currently, post-synthesis functional simulation of Synopsys designs is not supported. To obtain a post-synthesis gate-level functional simulation netlist, you must place the design using PPR to translate all of the modules into primitives, then follow a timing-simulation netlist flow to generate a netlist that can be simulated. The flow is the following

```
xmake -n design
```

```
ppr design route=false placer_effort=1  
timenetcx design xc4000 -x
```

To get a unit delay simulation, you then run Verilog-XL with a +delay_mode_unit option.

```
verilog +delay_mode_unit design.v design.stim
```

Documentation

This section provides information about and lists corrections reported against the documentation.

Online Documentation

Platform: All
Architecture: All
Design Step: Installation
Reference Number: Not Available

The directory structure of the compiled index files for the online documents is as follows:

- Xilinx Apps Info: \xact\online\onlinedb.pdx
- Xilinx Online Docs: \xact\online\online.pdx
- PRO Series Online Docs: \proser\online\proser.pdx

Hardware & Peripherals User Guide

Group Command Description Does Not Explain Signal Order

Platform: All
Architecture: All
Design Step: Not Available
Reference Number: 10803

The example in the Group command does not explain the importance of the signal ordering. The leftmost signal in the command-line string represents the MSB of a bus; the rightmost signal the LSB of the bus. Thus, in the example, “A0, A1, A2, A3,” the MSB will be a 0; the LSB will be a 3.

Libraries Guide

RLOC_ORIGIN Required On BUFT RLOCs

Platform: All

Architecture: XC3100/A, XC3000/A/L, XC4000/A/D/E/H

Reference Number: Not Available

In the *Libraries Guide*, references to BUFT support for RLOCs on pages 4-40, 4-41, 4-72, and 4-80 are misleading. RLOC sets containing BUFT components must be fixed with an RLOC_ORIGIN parameter

XC4000 CLB Carry Logic Illustration Correction

Platform: All

Architecture: XC4000/A/D/E/H

Design Step: Not Available

Reference Number: 10538

In the *Libraries Guide*, Figure 4-18 on page 4-98 is incorrect. The F3 input to the F Carry Logic block is sourced by the XACT F3 input to the CLB, not by the F4 input.

ACLK, GCLK Description Corrections

Platform: All

Architecture: XC2000, XC3000/A/L, XC3100/A

Design Step: Not Available

Reference Number: 10533

In the *Libraries Guide*, the ACLK (page 3-32) and GCLK (page 3-301) text descriptions are incorrect. You cannot connect GCLK or ACLK to a PAD element. You should connect these elements to an IPAD, or to an IBUF if a direct pad connection is not desired.

STARTUP Symbol Correction

Platform: All

Architecture: XC4000/A/D/E/H

Design Step: Not Available

Reference Number: 7470

The STARTUP symbol on page 3-442 in the *Libraries Guide* shows DONEIN as an output. DONEIN is an input.

Development System Reference Guide

XMake -I Option Description Is Incomplete

Platform: All
Architecture: All
Design Step: Not Available
Reference Number: Not Available

The description of the XMake -I option is incomplete. The third and fourth paragraphs should be replaced by the following information:

For XC2000, XC2000L, XC3000, XC3100, XC3000A/L and XC3100A designs, the mapping of the CLBs is guided via the XNFMAP -h or -k option, specified in the profile. If XMake finds neither of these option in the profile, -k is used when running XNFMAP, provided that *design.pgf* file exists in the current directory, for XC3000A/L and XC3100A designs. For XC2000, XC2000L, XC3000 and XC3100 designs, XMake automatically runs LCA2XNF on the guide LCA file to generate a *design.pgf* for use by XNFMAP.

XMake Now Reads in a Viewlogic WIR File

Platform: All
Architecture: All
Design Step: Not Available
Reference Number: Not Available

XMake now reads in a Viewlogic WIR file, instead of a schematic file. It looks in the “wir” subdirectory for the Viewlogic design file instead of the “sch” subdirectory.

Substitute “wir/*design.1*” for all references to “sch/*design.1*.”

A sample MAK file for 5.2/6.0 follows:

```

#
# Created by XMAKE Version 5.2.0 on Tue May 30 09:39:39 1995
#
# The following options were used: -G -L -R
#
# The following is the hierarchy of the design 'wir/zoundz.1'
#
# wir/zoundz.1
#   wir/peak_mtr.1
#   z_rom.mem
#   wir/a_d_st.1
#     approx.abl
#     wir/a_d_reg.1
#     wir/a_d_io.1
#   wir/zero.1
#   wir/sys_osc4.1
#   wir/dbfaeio.1
#   wir/freq_ctr.1
#     wir/clkgen.1
#   wir/dec_disp.1
#     wir/sel_disp.1
#
DEFAULT_TARGET zoundz.bit

zoundz.bit : zoundz.lca
             makebits zoundz.lca

zoundz.lca : zoundz.cst zoundz.xtf
             ppr zoundz.xtf parttype=4003PC84-5
             xdelay -D -W zoundz.lca

zoundz.xtf : zoundz.xg
             xnfprep zoundz.xg zoundz.xtf parttype=4003PC84-5

zoundz.xg : zoundz.xtg
            xblox zoundz.xtg zoundz.xg parttype=4003PC84-5

zoundz.xtg : zoundz.xff
            xnfprep zoundz.xff zoundz.xtg parttype=4003PC84-5

zoundz.xff : xnf/sel_disp.xnf xnf/dec_disp.xnf xnf/clkgen.xnf \
             xnf/freq_ctr.xnf xnf/dbfaeio.xnf xnf/sys_osc4.xnf xnf/zero.xnf xnf/a_d_io.xnf \
             xnf/a_d_reg.xnf xnf/approx.xnf xnf/a_d_st.xnf xnf/z_rom.xnf xnf/peak_mtr.xnf \
             xnf/zoundz.xnf
             xnfmerge -A -D xnf -D . -P 4003PC84-5 xnf/zoundz.xnf zoundz.xff

xn timer : xnf/sel_disp.1 xnf/dec_disp.1 xnf/clkgen.1 xnf/freq_ctr.1 \
           xnf/dbfaeio.1 xnf/sys_osc4.1 xnf/zero.1 xnf/a_d_io.1 xnf/a_d_reg.1 \
           xnf/a_d_st.1 xnf/peak_mtr.1 xnf/zoundz.1
           wir2xn timer -B -OD xnf zoundz zoundz.xnf

xn timer : z_rom.mem
           memgen z_rom.mem output_directory=xnf -old_library

xn timer : approx.abl
           abl2xn timer approx.abl output_directory=xnf -old_library family=XC4000 parttype=4003PC84-5

```


Xilinx Customer Support Information

For registration, authorization codes, update information, warranty status, shipping, product issues, and technical support, call Monday through Friday, 8 a.m. to 5 p.m. Pacific time.

Registration, Authorization, and Customer Service

- United States and Canada.....1-800-624-4782
- Europe..... Contact your local Distributor
- Japan.....81-33-297-9191
- Southeast Asia/All Other Countries.....852-2424-5200
- Facsimile Transmission.....1-408-559-0115

Technical Support

Hotline Access

Location	Telephone	Electronic Mail
U.S. and Canada	1-800-255-7778	hotline@xilinx.com
Japan	81-3 -3297-9163	jhotline@xilinx.com
France	33-1-3463-0100	frhelp@xilinx.com
Germany	49-89-9915-4930	dlhelp@xilinx.com
United Kingdom	44-1-932-820821	ukhelp@xilinx.com
To Contact Factory	1-408-879-5199	hotline@xilinx.com

- Technical Support FAX(24 hours/7 days)1-408-879-4442
- Technical Support BBS (24 hours/7 days)1-408-559-9327
- Internet E-mail Address (24 hours/7 days).....hotline@xilinx.com
- Xilinx Worldwide Web Site <http://www.xilinx.com>

Training

- Xilinx Training Administrator1-408-879-5090
- International customers, contact your local sales representative or distributor.



The Programmable Logic CompanySM



0401534