



Release Document

***XACTstep* Version 5.2/6.0**
XEPLD Translator Core Tools

October 1995

Read This Before Installation

XACT 6.0 Install for Windows

The following information supersedes the instructions in the *Getting Started & Installation Guide* for installing XACTstep 6.0 software on PCs running Microsoft Windows. These steps minimize XACTstep 6.0 problems caused by PC resource issues and Microsoft Windows configurations that are not optimal.

Note: After installation is complete, the install program will present you with required environment variable settings for your autoexec.bat program. In some cases this may include multiple paths to the PROSeries tools. The duplicate entry will not prevent the software from running, and can be deleted.

For complete configuration instructions, please see the “Setting Up the Xilinx Environment” chapter of the *Getting Started & Installation Guide*.

1. Before starting the XACTstep 6.0 installation process, Xilinx recommends that you make backup copies of the win.ini and system.ini files located in your Windows directory.
2. Before starting Windows, run a batch file called rmwin32s.bat in DOS to remove any previous version of the Microsoft WIN32S driver that may be installed on your PC.

The latest version (v1.25.142.0) is necessary for use with XACTstep 6.0 and is compatible with all previous versions. If you are not sure if WIN32S is installed on your PC, you can still run this program. If the driver is not installed, rmwin32s.bat tries to delete certain files and then reports that these files could not be found.

To run `rmwin32s.bat`, first identify the CD-ROM drive letter, for example, `D:\`.

From the DOS command prompt, type the following:

```
d:\xbbs\utils\rmwin32s.bat
```

If the WIN32S driver is found, all associated files are removed from your system, and you are prompted to manually remove `winmm16.dll` and `device=...W32S.386` from your `system.ini` file.

3. Next, start Microsoft Windows.
4. In Windows, select **File** → **Run** from the Program Manager.
5. In the command line box, type the following:

```
d:\win32s\disk1\setup.exe
```

This step installs the latest version of the Microsoft WIN32S driver needed for XACTstep 6.0 applications.

6. Select **File** → **Run** from the Program Manager.
7. In the command line box, type the following:

```
d:\xbbs\utils\xinfo\xinfo.exe
```

XINFO is a Xilinx utility that analyzes your computer's system resources for compatibility with the XACTstep software. Review the "Hints" page for suggestions on changes that you should make to your PC configuration to allow XACTstep 6.0 to run more efficiently on your PC.

8. Select **File** → **Run** from the Program Manager.
9. To begin the installation of the XACTstep 6.0 toolset, type the following in the command line box:

```
d:\setup.exe
```

Note: Preliminary calculations of disk space requirements may be inaccurate, depending on how your hard disk is formatted. To identify required disk space accurately, the Install program must calculate disk space on the basis of the selected products list. Using Custom Install, you can correctly calculate the required disk space by turning on the Analyze Disk Space option after making your selections. Using Quick Install, simply continuing the installation process by selecting the Install button correctly calculates the available disk space.

10. After installation is complete, exit from Windows.

11. Using a text editor, load c:\autoexec.bat.

Certain XACT*step* tools require that the temporary variable be set. If you do not see a line such as “set temp=c:\temp” in your autoexec.bat file, add it to this file. (The location of the temporary directory is not important; only the existence of the variable and a valid path are important.)

12. Next, reboot your PC to ensure that all environment variables have been set correctly.

Refer to the *Getting Started & Installation Guide* for information on other topics, such as environment variables and disk space requirements.

Installing Online Documentation

Starting with the 5.2/6.0 release, online documentation is now available on the Sun and HP workstations.

Installing Online Documentation on a Sun Workstation

To use online documentation, you must install the Acrobat reader and the online documents on your workstation.

Installing the Reader and Documents

Version 1.0 of the Acrobat reader is included on the XACTstep Sun 5.2 CD-ROM disk. To install the Acrobat reader, follow the instructions on page 4-4 of the *Getting Started & Installation Guide*.

Because the online documents are in tar format, you must use the XACTstep 5.2 installation program to install the online documents on your workstation. Refer to the Sun4 instructions on page 3-2 of the *Getting Started & Installation Guide*.

Opening Documents with Acrobat Reader — Sun Workstation Installations

To access the AcroRead program from the command line, follow these instructions:

1. Include the path to the /AcroRead_1.0/bin directory in the \$path variable of your configuration file,
2. At the command line, type the following to invoke the Acrobat reader:

```
acroread
```

The Open file dialog box of the Acrobat reader is displayed.

3. Specify the following path in the Filter box of the Open file dialog box to view Xilinx Online Documents:

```
/xact_dir/online/online/*.pdf
```

To view Xilinx Application Information, specify the following path:

```
/xact_dir/online/onlinedb/*.pdf
```

4. Select the document you want from the displayed list of .pdf files.

Installing Online Documentation on a HP Workstation

To use online documentation, you must install the Acrobat reader and, optionally, the online documents on your workstation.

Installing the Reader and Documents

Version 2.1 of the Acrobat reader is available on HP workstations on a separate enclosed Acrobat CD-ROM disk also provided by Xilinx. Use the instructions outlined in this section to install the Acrobat software on an HP workstation.

Installation of the Acrobat reader requires the HP-UX 9.05 operating system, the HP-VUE window manager, and 12 MB of disk space. You do not have to install the online documents to your hard disk, but if you choose to do so, you will need 52 MB of disk space.

1. Insert the CD-ROM disk into the CD-ROM drive.
2. Mount the CD-ROM drive. You need system administrator privileges to complete this step.
3. Invoke the Acrobat Installation program as follows:

```
/cdrom_dir/acrobat/unix/install
```

By default, after you have installed the desired products to your HP workstation, the installation program copies the Acrobat reader to the /usr/AcroRead directory. Xilinx recommends that you install the reader to /xact_dir/doc/AcroRead. You must include the AcroRead/bin directory in your path.

For more information, print the “Introducing Adobe Acrobat Reader 2.1” file located in `/cdrom_dir/acrobat/unix/instguid.txt`.

Note: If you want to install the document files on your workstation, copy the `/cdrom_dir/onlindb` and `/cdrom_dir/online` directory trees from the XACTstep Version 5.2 CD-ROM to your disk. For example:

```
cp -Rp /cdrom_dir/onlindb /xact_dir/doc/onlindb ↵
cp -Rp /cdrom_dir/online /xact_dir/doc/online ↵
chmod -R u+w xact_dir/doc↵
```

Opening Documents with Acrobat Reader — HP Workstation Installations

To view documents on an HP workstation, follow the instructions outlined in this section. For additional information refer to the “Viewing Documents with Acrobat Reader” section on page 4-7 of the *Getting Started & Installation Guide*.

You can either start the reader first and then decide what type of documents you want to view, or you can open the type of documents you want to view at the same time you load the reader.

To start the reader without specifying any documents, follow these instructions:

1. Ensure that the Acrobat Reader `AcroRead/bin` directory is in your path.
2. To start the reader, type the following:
acroread
3. Specify one of the following paths corresponding to the type of documents you wish to view:

To view Xilinx Online Documents, open the file:

`/cdrom_dir/online/linkpage.pdf`

or

`/xact_dir/online/linkpage.pdf`

To view Xilinx Application Information, open the file:

`/cdrom_dir/onlindb/dblink.pdf`

or

`/xact_dir/onlindb/dblink.pdf`

To specify the type of documents you wish to view at the time you invoke the reader, include the path you want after the `acoread` command as follows:

To view Xilinx Online Documents, use the command:

`acoread /cdrom_dir/online/linkpage.pdf &`

or

`acoread /xact_dir/online/linkpage.pdf &`

To view Xilinx Application Information, use the command:

`acoread /cdrom_dir/onlindb/dblink.pdf &`

or

`acoread /xact_dir/onlindb/dblink.pdf &`

Versions and Compatibility

The following master table indicates Xilinx core software with the current version numbers.

Software Versions

Program	Windows Version	DOS Version	Workstation Version
APR	5.2	5.2	5.2
APRLOOP	5.2	5.2	5.2
CstCvt	5.2	5.2	5.2
Design Manager	6.0	N/A	N/A
Floorplanner	6.0	N/A	5.2
Flow Engine	6.0	N/A	N/A
Hardware Debugger	6.0	N/A	N/A
HM2RPM	5.2	5.2	5.2
LCA2XNF	5.2	5.2	5.2
MakeBits	5.2	5.2	5.2
MakePROM	5.2	5.2	5.2
MAP2LCA	5.2	5.2	5.2
MemGen	5.2	5.2	5.2
PPR	5.2	5.2	5.2
PROM File Formatter	6.0	N/A	N/A
Report Browser	6.0	N/A	N/A
SymGen	5.2	5.2	5.2
Timing Analyzer	6.0	N/A	N/A

Program	Windows Version	DOS Version	Workstation Version
XACT	5.2	5.2	5.2
XBLOX	5.2	5.2	5.2
XChecker	5.2	5.2	5.2
XCK88	N/A	5.2	N/A
XDE	5.2	5.2	5.2
XDelay	5.2	5.2	5.2
XDM	N/A	N/A	5.2
xdm	5.2	5.2	5.2
XEMake	N/A	N/A	5.2
XEMake6	6.0	N/A	N/A
XKey	5.2	5.2	N/A
XMake	5.2	5.2	5.2
XNFBA	5.2	5.2	5.2
XNFCvt	5.2	5.2	5.2
XNFMAP	5.2	5.2	5.2
XNFMerge	5.2	5.2	5.2
XNFPrep	5.2	5.2	5.2
XPP	5.2	5.2	5.2
XPrint	5.2	5.2	5.2
XSimMake	5.2	5.2	5.2

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Chapter 1

Introduction

Welcome to the XEPLD Translator Core Tools Interface from Xilinx! This release note supports the following products.

- XEPLD Translator Core Tools (DS-550)

The 5.2 release for workstations contains bug fixes. There are no changes to algorithms in the fitter.

The 6.0 release for PCs is a major upgrade with enhancements to fitter algorithms that improve first-pass fit rate and enhance pin locking capability.

With the V6.0 release will not support DOS versions of the software. On the PC, run the Design Manager under Windows. Entering commands on a Command Line is not supported.

Contents

The Development System (DS) product you received contains software and documentation. Update products have software and documentation also.

Software

Xilinx software for all platforms is provided on CD-ROM, including:

- Installation Program
- XEPLD Translator Core Tools (DS-550)

Documentation

The following documentation is available in print for XEPLD products.

- *Getting Started & Installation Guide*
- *Additional Products & Services Packet*

Online Documentation

The following online documentation is included with your XEPLD products.

- *Libraries Guide*
- *Libraries Supplement Guide*
- *Floorplanner Reference/User Guide*
- *Design Manager/Flow Engine Reference/User Guide*
- *Timing Analyzer Reference/User Guide*
- *Hardware Debugger Reference/User Guide*
- *PROM File Formatter Reference/User Guide*
- *Development System User Guide*
- *Development System Reference Guide, Vols 1-3*
- *Hardware & Peripherals User Guide*
- *XEPLD Reference Guide*
- *XEPLD Design Guide*
- *XEPLD Schematic Design Guide*
- *XEPLD Reference Guide (for Windows)*
- *XEPLD Schematic Design Guide (for Windows)*

Note: Xilinx Core FPGA and EPLD documentation for Sun and PC platforms is available online via CD-ROM. Some documentation for product updates and for other workstation platforms is included on the basis of product configuration.

Selected Xilinx manuals are available in printed form. See the “Documentation Order Form” in the *Additional Products & Services Packet*.

Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with one year of maintenance¹; you will receive all software and documentation updates automatically during that time. You will receive a notice at the end of the year giving instructions on how to renew your maintenance contract.

Memory Manager Support

Xilinx PC-based software runs under MS-DOS 5.0 or later. With MS-DOS 5.0, do not start the HIMEM.SYS expanded memory manager in your CONFIG.SYS file.

1. Not included with DS-550-PC1.

System Requirements

This chapter describes system requirements for PC (V6.0) and workstation (V5.2) software.

Hardware

PC Requirements (V6.0)

To run V6.0 software, you need the following hardware:

- IBM-compatible PC 486 or Pentium
- VGA (or SVGA) graphics card and monitor.
- 16 MB of RAM, minimum.
- At least 4 MB of disk space on the hard disk drive to run Xilinx Windows Setup Program. To install XACTstep Development System Tools, you need 30 to 180 MB, depending on which options you choose.

Software	Approximate MB
FPGA Core	30 to 100
EPLD Core	30
PRO Series PROcapture and PROsim	20
PRO Series PROsynthesis	14
Viewlogic Interface	7 to 16
OrCAD Interface	20

- 460 KB of free conventional memory
- ISO9660 CD-ROM drive.

- Windows-compatible mouse
- Two serial RS-232 ports and one parallel port (for a Viewlogic or OrCAD security key, if required)

Workstation Requirements (V5.2)

Workstations require the following:

- Workstation types:
 - Sun4 (SPARC) with SunOS 4.1.x
 - HP-PA 9000 (RISC) Model 700 with HP-UX 9.05
 - IBM RS6000 with AIX 3.2.5
 - DEC Alpha AXP with OSF/1 Version 1.3 or 3.0
- RAM: 64 MB (recommended)
- Swap space: 75 MB

In addition, the following requirements must be met to run the Install program using a CD-ROM.

- CD-ROM drive: ISO9660
- Disk space: 10 MB
- RAM memory: 32 MB

Operating System

PC Requirements (V6.0)

To run Xilinx PC-based software, you need the following:

- MS-DOS 5.0 or later operating system
- Windows 3.1 or later to run the Xilinx setup program

Note: We recommend setting up a Virtual Memory of at least 16 MB. You can use either a permanent or temporary Virtual Memory. To set up Virtual Memory on a 486 PC with Windows 3.1:

1. Select the **Control Panel** icon. The Control Panel menu will appear.

2. Select the **386 Enhanced** icon. The 386 Enhanced menu will appear.
3. Click on the **Virtual Memory** softkey.
4. Click on **Change** to get the expanded Virtual Memory menu.
5. At the **Type** line select Permanent. If you have fragmented disk space you may have to select Temporary to get sufficient size.
6. On the **New Size** line, enter at least **16000** (KB is assumed). Press **OK**. You will have to restart Windows for the change to take place.

Workstation Requirements (V5.2)

- TCP/IP software
- Display: X-Windows

See Workstation Requirements (V5.2) under Hardware for operating system requirements for specific Workstations.

Chapter 3

Features in This Release

This chapter discusses the new features of XEPLD V6.0 release.

Where to Start in the XEPLD Reference Manual

Chapter 1 of the new 6.0 *XEPLD Reference Guide* contains a short tutorial that introduces you to the new user interface and shows you the simplest way to process a design. Chapter 1 and the Design Directories and Files appendix describe the flows and files for all the supported schematic, behavioral, and synthesis design tools.

Windows-Based Interface

The Design Manager, which is common to FPGA and EPLD, makes design implementation easier than ever. This Windows-based user interface has the following graphical ease-of-use features:

- Standard Windows look and feel
- More intuitive menu and command names
- Toolbar with icons for frequently used commands
- Icons for tools such as the Timing Analyzer
- On-line help system

This interface has the following functional ease-of-use features:

- Simple design import and export
- Simple pushbutton design processing in the Flow Manager
- Dialog boxes for advanced-user options
- File management handled automatically

- All global design and fitter options selected from the interface (instead of using global attributes in your design file).

The new interface is described in detail in the *XEPLD Reference Guide for Windows*.

Automatic Device Selection

You can now select a range of devices and allow the software to choose the smallest device into which the design fits. For example, you can select a package type (such as PC68) and/or speed grade (such as -10) and allow the software to choose the best device with that package type and/or speed grade.

Timing Analyzer

The Timing Analyzer, which is part of the Design Manager toolset and has a Windows-based graphical interface, allows you to analyze the timing of your implemented design. You can choose from the following timing reports:

- Performance to TimeSpecs — Compares the implementation of the design with the imposed timing constraints.
- Performance Summary — Summarizes the overall design performance.
- Detailed Path Report — Lists worst-case path delay information for all paths in the design that have not been excluded by filters.
- Check for Asynchronous Logic — Lists signals that are possibly asynchronous and the product-term clock signals that control them.
- Show Clocks — Lists the clock signals in the design.
- Show Settings — Lists the current settings of the timing analyzer, including which path filters have been applied.

You can apply filters to include in the reports only the paths you are interested in. You can also change other options that affect timing, such as the speed grade of the device.

XACT-Performance Supported for EPLD Devices

Timing specifications for paths and groups of paths in your design can now be specified using the same attributes used on FPGA designs. You can see whether your fitted design meets these specifications using the Timing Analyzer.

To specify timing for a behavioral design, use a .cst (constraint) file.

XEPLD supports only the newer “FROM:TO:” TIMESPEC format introduced in XACT V5.0. Do not use the old-style “path-to-path” format for EPLDs.

Report Browser and New Reports

The Flow Manager produces several reports, which appear as icons in the Report Browser window after you have fitted your design. Double clicking on a report icon displays the report in a separate window.

The reports carried over from the last release are as follows:

- Resource Report — Lists the device resources used by the design and the resources remaining.
- Pin Out Report — Shows how the external nets in your design were mapped to the device pins.
- Mapping Report — Tells you how the logic in the design was mapped to the device.
- Fitting Report (formerly Partitioner Report) — Shows the allocation of Function Block resources.

The new reports are as follows:

- Timing Report — Shows the calculated worst-case timing for the logic paths in your design.
- Timespec Report — Tells you if you have made any errors in assigning TSPEC attributes in your design and lists the TSPECs that the fitter used.

Simulation Support

From Dos

Functional simulation of schematic designs with behavioral modules is now possible using XSIMMAKE, which is invoked under DOS. The Master Reset pin is also supported under functional simulation. All registers preload to the state you define using the INIT=R or INIT=S attribute, if specified.

The XSIMMAKE command performs all the steps necessary to create a functional or timing simulation netlist file for Viewlogic or OrCAD simulation. The format of this command is as follows:

```
xsimmake -f vef6 | vet6 | oef6 | oet6 [-o output_file]  
                        design_name
```

The -o option specifies the name of the output simulation netlist file, minus the extension; the default is the input file name. If you perform functional simulation, you may wish to use a different name for your timing simulation netlist file.

The target (-f target) is always required. Select one of the following targets:

- vef6 (Viewlogic EPLD Functional) — Prepares a functional simulation netlist file (VSM format) based on a schematic or mixed-mode design.
- vet6 (Viewlogic EPLD Timing) — Prepares a timing simulation netlist file (VSM format) based on a completed EPLD design (VM6 database) produced by the Design Manager.
- oef6 (OrCAD EPLD Functional) — Prepares a functional simulation netlist file (with .vst extension) based on a schematic or mixed-mode design.
- oet6 (OrCAD EPLD Timing) — Prepares a timing simulation netlist file (with .vst extension) based on a completed EPLD design (VM6 database) produced by the Design Manager.

From Windows

You can also use the Simulation icon in Windows to invoke any of these XSIMMAKE flows. In the dialog box that appears after double-clicking the icon, select the name of a schematic file (sch\filename.1 for

Viewlogic or *filename.sch* for OrCAD) for either functional or timing simulation.

Select the XC7000 family. If your schematic does not contain a PART-TYPE attribute, select “New Parttype” and enter the device code in the box.

Select the desired simulation (Functional or Timing) and the name of your simulation tool (Viewlogic or OrCAD). Xsimmake generates the appropriate simulation netlist (*filename.vsm* for Viewlogic or *filename.vst* for OrCAD). Errors, if any, are written to *Xsimmake.out*, which can be viewed by opening the Xsimmake Results icon.

Partitioner Performs Second Pass to Fit the Design

The partitioner may try a second pass to fit your design. During the second pass, it may move Fast Function Block signals into High-Density Function Blocks and vice versa to fit the design. Only the final Fitter Report is created.

New Guide File for Pin Freezing

To preserve the pinout of your design, use a guide file (*design_name.gyd*), which is created when you run the fitter. You can still use *.vmf* files, but guide files are preferred.

We strongly recommend using the guide file instead of back-annotating the pinout into the design.

Fitter Removes Redundant and Constant Output Ports, and Redundant Input Ports

The fitter automatically removes feedthrough output ports, constant high/low output ports, all but one of multiple output ports driven by the same logic source, and redundant input ports. Use BUF with OPT=OFF to prevent optimization.

Automatic Symbol Generation

Use the Symbol Generation Utility icon in the XACT Window to automatically generate symbols in Viewlogic or OrCAD for behavioral models in your schematic design.

In the dialog box that appears, enter the name of a PLUSASM language equation file (with extension “.pld”), or go to the Browse menu and select “PAL Equation Files” as the file type to get a listing.

Then select either Viewlogic or OrCAD as the Symbol Type. XEPLD software will read your equation file, checking for errors, then generate either a Viewlogic symbol (sym\filename.1) or an OrCAD macro command file (filename.cmd) that you can run in LIBEDIT to create a symbol in your custom OrCAD symbol library.

INIT Attribute

The INIT component attribute allows you to specify the preload value of a registered component (such as FDCE or CB8CE) in a schematic design. INIT=S specifies a preload value of 1; INIT=R specifies 0. Do not use this attribute for input registers or components whose outputs are tagged with the F attribute, because input and Fast Function Block registers always have a preload value of 1.

Slew Rate Control for XC73144 Devices

The XC73144 devices have two slew rates, SLOW (the default), and FAST. In PLUSASM behavioral designs, use the following declarations to specify a fast slew rate:

```
FAST ON signal_list
```

In schematic designs, use the following schematic attribute on output ports such as OBUF and IOPAD:

```
FAST
```

Using the FAST schematic attribute on a component that does not have an output pin results in an error when you attempt to fit the design.

New Devices

All supported devices are listed below. The XC7336Q is a new device with this release.

Device	Packages	Speed Grades
XC7236A	PC44	-16, -20, -25
XC7318	PC44, PQ44	-5, -7
XC7336	PC44, PQ44	-5, -7, -10, -12, -15
XC7336Q	PC44, WC44, PQ44, VQ44	-10, -12, -15
XC7354	PC44, PC68	-7, -10, -12, -15
XC7372	PC68, PC84, PQ100	-7, -10, -12, -15
XC73108	BG225, PC84, PG144, PQ100, PQ160	-7, -10, -12, -15, -20
XC73144	BG225, PQ160	-7, -10, -12, -15

Features No Longer Supported

OrCAD Global Attributes

Global attributes, such as “|PRELOAD_OPT=OFF,” and the global attribute header string “|GLOBAL” are no longer supported in OrCAD schematics. Instead, use the new Windows-based user interface to select all desired global design and fitter options. You must delete any global attribute strings from your existing designs. The “pipe-text” mechanism can only be used to specify TIMEGRP information as used by X-Performance. The TSPREP step of design entry will report an error if an obsolete global attribute is found.

PALCONVT Command

Automatic generation of a top level PLUSASM behavioral design file is no longer supported. Instead, create the top level file with a text editor.

JED2PLD Command

JEDEC files targeted at 20V8 and 22V10 PALs can no longer be converted directly to PLUSASM files using the JED2PLD command.

New Attribute for Behavioral Modules

To specify that the logic for a custom symbol (PAL component) is defined in a behavioral file, assign to the component instance the following attributes:

FILE=*file_name*

DEF=PLD

The original attribute, PLD=*file_name*, is still supported for backward compatibility, but should not be used for new designs.

Chapter 4

Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 ^a	PC44, PC68, PC84, PG84, TQ100, VQ64	-33, -50, -70, -100, -130
XC2064 ^a	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L ^a	PC84, VQ64, VQ100	-10
XC2064L ^a	PC68, VQ64	-10
XC3020 ^a	CB100, CQ100, PC68, PC84, PG84, PQ100	-50, -70, -100, -125
XC3030 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 ^a	CB100, CQ100, PC84, PG84, PG132, PP132, PQ100, TQ100	-50, -70, -100, -125
XC3064 ^{a b}	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 ^{a b}	CB164, CQ164, PC84, PG175, PP175, PQ160, PQ208	-50, -70, -100, -125
XC3020A	CB100, PC68, PC84, PG84, PQ100	-6, -7
XC3030A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-6, -7
XC3042A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-6, -7
XC3064A ^b	PC84, PG132, PP132, PQ160, TQ144	-6, -7
XC3090A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, TQ144, VQ100	-8
XC3064L ^b	PC84, TQ144	-8

Device	Packages	Speed Grades
XC3090L ^b	PC84, TQ176	-8
XC3120 ^a	CB100, PC68, PC84, PG84, PQ100	-3, -4, -5
XC3130 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 ^a	CB100, PC84, PG84, PG132, PP132, PQ100, TQ100, TQ144	-3, -4, -5
XC3164 ^{a b}	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 ^{a b}	CB164, PC84, PG175, PP175, PQ160, PQ208	-3, -4, -5
XC3195 ^{a b}	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-3, -4, -5
XC3120A	CB100, PC68, PC84, PG84, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-1, -2, -3, -4, -5
XC3142A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-1, -2, -3, -4, -5
XC3164A ^b	PC84, PG132, PP132, PQ160, TQ144	-1, -2, -3, -4, -5
XC3190A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-1, -2, -3, -4, -5
XC3195A ^b	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-1, -2, -3, -4, -5
XC4003	PC84, PG120, PQ100	-4, -5, -6
XC4005 ^b	CB164, PC84, PG156, PQ100, PQ160, PQ208	-3, -4, -5, -6, -6B, -10
XC4006 ^b	PC84, PG156, PQ160, PQ208	-3, -4, -5, -6
XC4008 ^b	MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6
XC4010 ^b	BG225, CB196, MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6, -10
XC4013 ^b	BG225, CB228, MQ208, MQ240, PG223, PQ160, PQ208, PQ240	-3, -4, -5, -6, -10
XC4002A	PC84, PG120, PQ100, VQ100	-5, -6
XC4003A	CB100, PC84, PG120, PQ100, VQ100	-4, -5, -6, -10
XC4004A ^b	PC84, PG120, PQ160, TQ144	-5, -6
XC4005A ^b	PC84, PG156, PQ160, PQ208, TQ144	-4, -5, -6
XC4010D ^b	BG225, PC84, PQ160, PQ208	-5, -6
XC4013D ^b	BG225, PQ160, PQ208, PQ240	-5, -6
XC4003H	PG191, PQ208	-5, -6
XC4005H ^b	MQ240, PG223, PQ240	-5, -6
XC5202	PC84, PG156, PQ100, TQ144, VQ100	-5, -6

Device	Packages	Speed Grades
XC5204	PC84, PG156, PQ100, PQ160, TQ144, VQ100	-5, -6
XC5206 ^b	PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100	-5, -6
XC5210 ^b	BG225, PC84, PG223, PQ160, PQ208, PQ240, TQ144	-5, -6
XC5215 ^b	HQ304, PG299, PQ208, PQ240	-5, -6
XC7236A ^a	PC44	-16, -20, -25
XC7318 ^a	PC44, PQ44	-5, -7
XC7336 ^a	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 ^a	PC44, PC68	-7, -10, -12, -15
XC7372 ^a	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q ^a	PC44, PQ44, VQ44	-10, -12, -15
XC73108 ^a	BG225, PC84, PG144, PQ100, PQ160	-7, -10, -12, -15, -20
XC73144 ^a	BG225, PQ160	-7, -10, -12, -15

a. Not supported in X-BLOX.

b. Not supported in Base packages.

Known Issues

This chapter describes the known issues in this release.

Software

Installation

Analyze Components Package Before Using PROsynthesis

Platform: PC

Architecture: XC7000

Design Step: Installation

Reference Number: Not Available

Before using the XC7000 Components Package (use xc7000.components.all) in a PROsynthesis design on the PC, you need to analyze the package using the synthesis tool. The analyzed version of the package is not installed from the CD. After installing and configuring your system to run PROsynthesis, go to DOS (or a DOS window) and type:

```
cd c:\proser\unified\xc7000
vhdldes
vhdl comp.vhd
quit
```

Design Entry

Connect All Schematic Macro Inputs

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: Not Available

Leaving inputs of macro symbols unconnected in a schematic may give unintended logical results. Connect all unused inputs to a VCC or GND symbol in your schematic. Inputs of primitive logic gates can be left unconnected.

Initial States of Registers in Schematics Are Predictable Only by Using the INIT Attribute or by Disabling Preload Optimization

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: 19467

By default, the software automatically assigns the initial preload state of all registers in a schematic design to achieve higher mapping efficiency. You can use the INIT=R or INIT=S attribute on registered components to explicitly control preload values. The default initial states defined in the *Libraries Guide* and any PRLD equations you specify in the equation files for embedded behavioral modules are maintained only if you disable the preload optimization feature in the Design Manager (V6.0) or specify the PRELOAD_OPT=OFF global attribute. Disabling preload optimization may seriously decrease mapping efficiency. When using V6.0, if a register's initial state is not defined in the schematic, functional simulation will not initialize the register when the PRLD or MRESET signal is pulsed.

Device Features Not Supported by XEPLD V5.2/6.0

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: 19468

The following feature of EPLD devices is described in the device data sheets (*The Programmable Logic Data Book*) but not supported in the current version of the development software.

FastInput (FI) pins for High-Density Function Blocks — which would provide three additional high-speed inputs to the Function Block AND arrays of XC7236 and XC7300 devices. The normal input path (to the UIM) is still supported on the pins designated as I/O/FI. FI pins for the Fast Function Blocks of XC7300 devices are fully supported.

The XC7272 device is not supported by V6.0.

The Fastcompare logic in XC7272 devices is no longer supported by XEPLD V5.2/6.0, even if you are using the old (V4.x) library.

Fitter Overwrites PLD Files with Same Name as Schematic (V5.2 only)

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: 14530

FITNET (or XEMAKE) converts all schematics into a PLUSASM behavioral file written to *design_name.pld*. Any PLD or custom component equation file of the same name is overwritten. Never name a PLD file the same as any design schematic in the same directory. No message warns you that you are about to overwrite this PLD file.

The IOPIN (FI) Option and PIN Feedback

Platform: All

Architecture: XC7000

Design Step: PLUSASM Design Entry

Reference Number: 17388

In PLUSASM behavioral designs, the FI option of the IOPIN declaration specifies that, by default, instances of the named signals appearing on the right-hand side of equations are taken from the FastInput path of the EPLD. If the signal name appears without a ".PIN" extension, the input is taken from the FastInput (not internal feedback). If you use the signal name with the ".PIN" extension, input is taken from the pin through the UIM path (and input-pad register, if used), not from the FastInput.

NEVER specify both the FI and PINFBK options in the same IOPIN declaration statement. The software may produce inconsistent results.

In general, be careful to keep all references to signals declared as IOPIN unambiguous whenever the FastInput path is used. If ALL instances of an I/O signal (on the right-hand side of equations) require the FastInput path, you can use the "IOPIN (FI)" default declaration; you do not need dot-extensions in your equations. If ANY instances of an I/O signal use either internal feedback or the UIM-input path, you should not use the FI option in your IOPIN statement. Instead, use the ".PIN" or ".FI" extension on each instance requiring UIM-input or FastInput, respectively.

PARTITION Statement Limitations (V6.0 only)

Platform: All

Architecture: XC7000

Design Step: PLUSASM Design Entry

Reference Number: Not Available

The following restrictions apply to PLUSASM behavioral designs:

1. The XEPLD fitter software ignores and displays a warning about some logical and physical partition statements. Use logical partitions only for logic that uses the arithmetic carry chain. Also, physical partitions for carry chain logic must always specify the starting macrocell numbers.

If you want to control the placement of arithmetic equations, for example A1, A2, and A3, use:

```
PARTITION FBn_m A1 A2 A3;
```

or:

```
PARTITION logical_name A1 A2 A3;
```

but NOT:

```
PARTITION FBn A1 A2 A3;
```

For logic that does not use the arithmetic chain, you may only use physical partitions, either with or without the starting macrocell number.

2. Do not use more than one partition statement for the same arithmetic chain, even if the chain spans more than one functional block. The first output name of any partition statement must not have its carry-in enabled (should not specify output. ADD=VCC). For example, the following is invalid:

```
PARTITION FB6_1 X0 X1 X2 X3 X4 X5 X6 X7 X8
PARTITION FB5_1 X9
EQUATIONS
X0 = X0.D1 XOR X0.D2
X0.D1 = A                X0 = A0 :+: B0
X0.D2 = B

X[1..9] = X[1..9].D1 XOR X[1..9].D2
X[1..9].D1 = A                X[1..9] = A[1..9] :+:
B[1..9]
X[1..9].D2 = B
X[1..9].ADD = VCC
```

Instead, you must specify one long PARTITION statement for the whole arithmetic chain. The two partition statements above should be replaced with the following:

```
PARTITION FB6_1 X0 X1 X2 X3 X4 X5 X6 X7 X8 X9
```

INIT Attributes Ignored on Input Registers

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: Not Available

Input registers (IFD) and input latches (ILD) are not affected by INIT attributes or the preload optimization option. Physically, input registers always preload to the “1” state. However, the fitter will change the apparent preload state if necessary to resolve inversions on their Q-outputs.

Behavioral Modules with 3-state Outputs Handled Differently in XEPLD V6.0

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: Not Available

In schematic designs, behavioral modules (PAL symbols) with 3-state outputs (out.trst=en) are interpreted differently in XEPLD V6.0.

In XEPLD 5.x, the 3-state enable affects only the chip output pin. All internal feedback is taken from the input to the 3-state buffer, unless the PLUSASM NODETRST declaration is used in the equation file.

In XEPLD 6.0, the 3-state enable affects the chip output and all internal feedback, except feedback used inside the same equation file. If your design uses equation feedback both inside the equation file and for other logic in the schematic, the 3-state buffer can not be optimized and will occupy a separate macrocell.

If your design depends on reproducing the behavior of XEPLD 5.x, remove the 3-state equation from the equation file and use an OBUFE on the schematic to create the 3-state chip output.

Note: If the equation file contains the NODETRST declaration, all internal feedback will be affected by the 3-state equation in both V5.x and V6.0, and the 3-state buffer can be optimized.

Do Not Use PLFFB9 with XEPLD V6.0

Platform: PC

Architecture: XC7000

Design Step: Design Entry

Reference Number: Not Available

XEPLD V6.0 does NOT support the use of PLFFB9 symbols. Use ordinary behavioral module symbols instead. You can still access all fast-function block features. Follow these steps to replace your PLFFB9 symbol:

1. In the PLUSASM equation file, change the **CHIP** type from **PLFFB9** to **COMPONENT**.
2. If you have used **.export** equations, add a **PARTITION** statement to define the order of the macrocells participating in the export chains. This should be the same order they appeared in your existing pin list.
3. To get backward compatibility with version 5.x software, you need to change output pin polarity (version 5.x software inverted the polarity of PLFFB9 equation outputs). Insert or remove a slash (/) in front of each equation output declaration on the pinlist.
4. Remove all **FASTINPUT** declarations from the equation file. If necessary, you can specify fast-inputs in the schematic using the "F" net attribute.
5. Use SYMGEN to assemble the **.pld** file and generate a schematic symbol showing the signal names.
6. Replace the PLFFB9 symbols in your schematic with the generated symbol. Add the attributes **DEF=PLD** and **FILE=filename** to each instance of the new symbol.
7. The fitter automatically assigns logic in your design to FFBs whenever possible. Any equations using export will always be implemented in an FFB. For critical timing paths, you can add timing specifications to your design. FFBs will be used automatically when necessary to meet timing specifications. Otherwise, you can add the "F" attribute to the nets connected to your behavioral symbol outputs if you want to explicitly assign them to FFBs.

Using Both Registered Input and Fast Input Paths Requires PLFFB9 (V5.2 only)

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: 19313

Some XC7300 devices have input pins that allow you use a fast-input, bypassing the UIM, and a registered input that goes through the UIM from the same device pin.

If you want to implement this schematically, connect IFD and IBUF components to an IPAD. The IBUF component represents the fast-input path. You can connect the IBUF component to a PLFFB9 component with that equation file input labelled FASTINPUT. If you attempt to connect the IBUF to any other component you receive the following error message.

```
dr62:[Error]Fast Input-only pin (DIBUF:O) is  
connected to standard Input-only pin (M2_1:D0)
```

Do Not Use Signal Name MRESET or PRLD In Your Design

Platform: All
Architecture: XC7000
Design Step: Design Entry
Reference Number: Not Available

MRESET and PRLD are reserved signal names that cannot be used in your design. These signal names are placed into the simulation netlist produced by the software and used to initialize your registers at the beginning of your simulation session.

Implementation

Internal 3-State Control Ignored in 7318 and 7336 Designs

Platform: All
Architecture: XC7000
Design Step: Implementation
Reference Number: 17593

3-state control functions (TRST equations) affecting internal feedback nodes (declared using NODETRST) can only be accomplished using High-density Function Blocks. The 7318 and 7336 devices contain only Fast FBs and therefore cannot implement on-chip 3-state bussing. The software ignores, without warning, any 3-state control functions applied to internal nodes in designs mapped onto these devices.

3-State Signals Pass Through Buffers/Inverters

Platform: All
Architecture: XC7000
Design Step: Implementation
Reference Number: 19469

In a schematic, a BUFE or a BUFT connected to an OBUF controls the 3-state driver of the device pin, even if a BUF or an INV is inserted between them. The software always optimizes the BUF and INV components into the OBUF unless you place the OPT=OFF attribute on the BUF or an INV symbol.

JEDEC Files May Not Be Usable for EPLD Programming

Platform: All
Architecture: XC7000
Design Step: Implementation
Reference Number: 14622

The JEDEC files produced by MAKEJED can only be read by device programmers specifically supporting the Xilinx EPLD JEDEC format. Many programmers supporting JEDEC for other devices do not support XC7000 JEDEC files.

Use the HEX format (PRG) file from MAKEPRG instead of a JEDEC file.

Pin and Node Assignment Example in Design Guide Is Incorrect (V5.2 only)

Platform: All
Architecture: XC7000
Design Step: Implementation
Reference Number: 19470

The way the XEPLD V5.x PALCONVT command interprets 3-state signals is not correctly described in the *XEPLD Design Guide*. The incorrect statements in the manual are as follows.

In Figure 3-7 on page 3-14 of the XEPLD Design Guide, the following lines are incorrect.

```
OUTPUTPIN L H  
NODE J K G F
```

They should be corrected as follows.

```
OUTPUTPIN L H K G  
NODE J F
```

The first sentence on page 3-15 of the Design Guide is not entirely correct. The sentence reads as follows.

The PALCONVT software interprets all signals that appear on both sides of the equations as nodes and assigns them to NODE statements in the Top-Level file.

The exception is correctly described on page 3-2.

Signals used as outputs that also have .TRST control inputs are assigned to OUTPUTPIN statements, even if they are also used as inputs.

Design Uses Too Many FB Resources to Fit Into the Target EPLD (V5.2 only)

Platform: All

Architecture: XC7000

Design Step: Implementation

Reference Number: Not Available

One of the reasons that a design may not fit into a particular EPLD device is that the logic optimization routine takes every opportunity to optimize for speed, sometimes at the expense of density. As a consequence, the optimizer may consume extra Function Block resources speeding up a path which may not give you any speed benefit in your application. For example, if the logic path for only one state register of a multi-bit state machine is made faster, it still does not allow you to clock the circuit at a higher frequency.

The V5.2 tools apply several different logic optimization routines to the design, trading speed for density until a fit is achieved. To determine if the logic optimizer is using extra resources to speed-up some but not all paths through a node, examine the "Collapse Module Report", `design_name.lgc`. The report contains two tables under the heading "Outputs that were collapsed". The second table lists logic nodes that were optimized forward into other outputs. If this table contains any messages of the form

```
n instances of node_name remain unoptimized--used in:  
output_name
```

then the logic for "`node_name`" still occupies a macrocell (it has not been completely absorbed by all of its fanouts). The outputs into which `node_name` was successfully optimized are made faster due to the optimization, but those outputs also generally increase in size. Unless any of the listed optimizations provide a speed-up that actually benefits your application, the optimization wastes resources.

You can inhibit the optimization of logic nodes which are not completely optimized. For any `node_name` reported with "instances ... remain unoptimized" (and for which you do not rely on any speed optimization), disable logic optimization for the `node_name` as follows.

For behavioral designs, place the following declaration into your PLUSASM top-level file.

```
LOGIC_OPT OFF node_name...
```

In a schematic design, apply the OPT=OFF attribute to the component instance containing the named output signal.

Failure To Fit the Design Using the Frozen Pinout

Platform: All

Architecture: XC7000

Design Step: Implementation

Reference Number: 19637,18786

In rare cases, the partitioner may report that it cannot fit a design using the frozen pinout even though you made little or no change to the design itself. Assigning pins changes the sequence of partitioner execution and can give a slightly different result.

```
es46:[Error]This design requires 1 more function
blocks than are available on the device. Consider
using the same device in a package with more I/O (if
available), a larger device, or multiple devices; or
remove design constraints and try again.
```

In V5.2, if you copy the *design_name*.eqn file from the successful fitting to *new_name*.pld and rerun the new file (using FITEQN for V5.2), the software should fit the design with the frozen pinout successfully.

In V6.0, remember to use the **.gyd** file instead of back-annotating the pinout into the design.

Cannot Access “Unbonded” Pad Resources

Platform: All

Architecture: XC7000

Design Step: Implementation

Reference Number: 18438

Smaller packages have “unbonded” pads. You cannot use the input register of an unbonded I/O pad. You cannot use “unbonded” fast-clock or FOE pads for on-chip generated fastclock or FOE signals.

If you want to use “unbonded” pad resources, target a larger package and use its programming file to program the smaller package. You must control the pinout so that the software uses only the “unbonded” pads you want.

Automatic Device Selection May Generate Spurious Error Messages (V6.0 only)

Platform: PC
Architecture: XC7000
Design Step: Implementation
Reference Number: Not Available

When the XEPLD fitter software tries different devices to find the smallest one in which your design fits, you may see error messages about the design not fitting before the proper device is found. You can ignore these messages.

Automatic Device Selection May Affect Timing Results

Platform: PC
Architecture: XC7000
Design Step: Implementation
Reference Number: Not Available

If you provide timing specifications in your design and you use automatic device selection, the fitter will determine the slowest speed grade device that can meet your timing specs, if possible. If you select a specific device speed grade and run the same design, the combination of logic optimizations performed to satisfy your timing specs may be different. In some cases, a faster speed grade device may be required to satisfy all your timing specs than the device chosen by automatic device selection. Selecting the faster speed grade is recommended if you want to increase the probability of reproducing your timing results in subsequent design iterations. Otherwise, you could continue to choose automatic device selection to see if subsequent design iterations can meet your timing specs using the slower device speed grade.

Use Guide File to Maintain Pinout (V6.0 only)

Platform: PC
Architecture: XC7000
Design Step: Implementation
Reference Number: Not Available

Use a guide file to reproduce a frozen pinout. Do not back-annotate the frozen pinout into the original design file.

Pin-assigning a function to a Fast Function Block may cause the software to perform different optimizations. The guide file records some of the optimizations performed on the previous fitting and allows the software to reproduce those optimizations.

Drive Unused I/O Option

Platform: PC

Architecture: XC7000

Design Step: Implementation

Reference Number: Not Available

The "Drive Unused I/O Pads on Chip" option in the Design Manager Implementation Template (v6.0), and the "-U" option of the FITNET and FITEQN commands (v5.x), should only be used with 7236A devices, and not with any 7300 family devices. Unused input and I/O pins should be managed according to the target EPLD device, as follows:

For 7236A devices, you must not allow any unused input or I/O pins to remain floating. We recommend that you specify the Drive Unused I/O option so that the software automatically drives valid logic levels onto all unused I/O pins. Each unused I/O pin will then be driven to the signal produced by the associated buried macrocell, if used, or to the Low state if the macrocell itself is unused. You must still tie all unused input-only pins to ground on your board. If you do not enable the Drive Unused I/O option, you must tie all unused input and I/O pins to ground on your board.

For 7336 and 7318 devices, you must always tie all unused input and I/O pins to ground on your board. These devices do not support the Drive Unused I/O feature.

For 7354, 7372, 73108 and 73144 devices, unused input and I/O pins may be left unconnected. These devices have weak pull-downs built into all input and I/O pins to prevent unused pads from floating. These pins should not be connected to floating traces on the board. You should not specify the Drive Unused I/O option for these devices. Please disregard the "tie" indications in the PIN report; these unused pins do not need to be tied to ground.

For all devices, never connect unused output-only pins on the board. The software may drive some of these pins with the internal macro-cell output values even if no output port is specified in your design.

Applying Clear and Preset Concurrently Gives Unpredictable Results

Platform: All

Architecture: XC7000

Design Step: Implementation

Reference Number: Not Available

If you assert both the clear (CLR) and preset (PRE) inputs of a flip-flop (FDCP) concurrently, the Q-output is unpredictable.

This issue involves design implementation, not simulation. Because the fitter may arbitrarily invert the logic stored in a flip-flop, the user cannot predict how the actual chip will function if CLR and PRE are asserted concurrently. Functional simulation does not accurately predict the ultimate behavior of the chip under these conditions. Timing simulation, however, will behave exactly as the chip is programmed.

Functional Simulation

Functional Simulation May Show Incorrect Preload Values

Platform: All

Architecture: XC7000

Design Step: Functional Simulation

Reference Number: 19467

In XEPLD V5.2, functional simulation uses the default preload values defined for library components. INIT attributes and PLUSASM PRLD equations are ignored in functional simulation but are recognized in the fitting process and in timing simulation.

In XEPLD V6.0, flip-flops remain uninitialized unless an INIT attribute is used, or preload optimization is disabled.

Timing Analysis

Timing for Input-Pad Flip-Flops is Inaccurately Reported (V6.0 only)

Platform: All

Architecture: XC7000

Design Step: Timing Analysis and Simulation

Reference Number: Not Available

All reported timing relating to input-pad flip-flops is inaccurate due to an excess delay in the flip-flop's clock path equal to the parameter tFCLKI. As correctly shown in the device Data Book, parameter tFCLKI should not be involved in timing calculations for the input-pad flip-flops. The value of tFCLKI should be subtracted from the reported clock-to-output delay and added to the reported setup time. Macrocell register timing is reported correctly.

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