

Board Level Simulation With Xilinx Foundation Series

version 1.1

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A generic library of FPGA and EPLD symbols which can be used to perform board level simulation of mixed FPGA/EPLD designs is available. This read-only, system-level symbol library does not currently contain all of the device packages that Xilinx offers; however, the symbols that are included can be used as starting points for creating your own symbols.

This library is called XFPGA. It is not currently shipped with the Foundation software but is available on the Xilinx FTP (ftp.xilinx.com) and BBS sites (408-559-9327 in the U.S., (44) 1932 333540 in Europe) as /pub/swhlp/foundation/XFPGA.ZIP.

This library enables the user to place EPLD and FPGA symbols onto a 'board level' schematic, and then assign a post-route, timing-annotated netlist to each symbol. This assignment process not only establishes connectivity between the symbol and the netlist but also automatically updates the symbol pin names with the net names found in the EXT records of the netlist.

The following steps should be followed to perform board-level simulation:

- Create individual FPGA and EPLD designs
- Create a project representing the board level
- Attach the FPGA library plus the necessary device libraries (XC7000U, XC5000U, etc.) to the board level project
- Place EPLD and FPGA symbols onto the board level schematic
- Assign timing back annotated netlists to the EPLD/FPGA symbols
- Connect the components
- Simulate as normal

Before the XFPGA library can be used for the first time, it must be attached to the Foundation development system. If you are familiar with how to perform this task, jump ahead to the section titled EXAMPLE.

Attaching the FPGA library to the Foundation Development System.

- Unzip the contents of XFPGA.ZIP to your C:\ACTIVE\SYSLIB subdirectory.
- From the Foundation Project manager select *Applications -> Library Manager*
- From the Library Manager window select *Library -> Attach*.
- In the Window that pops up, the default path is C:\ACTIVE\SYSLIB. As a result of this, the XFPGA library should be resident in the 'Libraries Found' window. Select *Attach.-> Close*.
- Scroll through the list of attached libraries and confirm that XFPGA has been attached as a System Macro Library.

EXAMPLE

The following shall discuss how to prepare a board level simulation of three Xilinx devices that interface together.

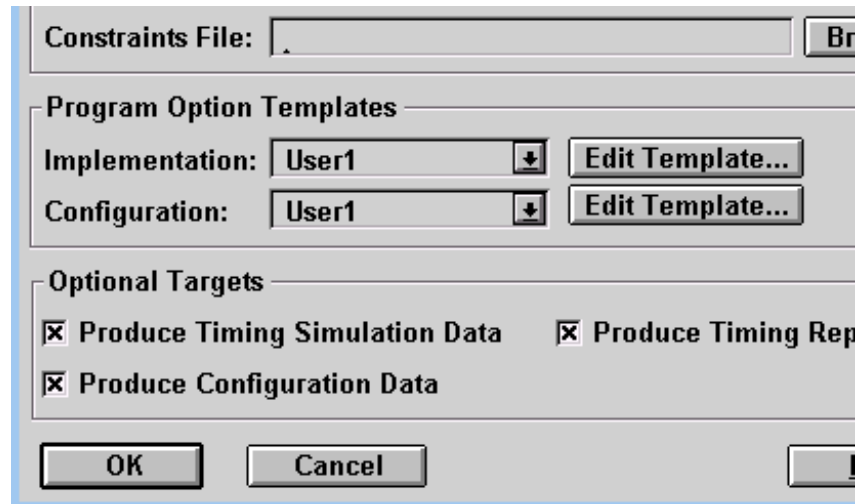
Consider a design called BOARD that uses the following three Xilinx devices.

Device	Design Name	Entry Method	Function
XC7354PC68-7	7KDECODE	Foundation Schematics with ABEL Modules.	Address Decoder
XC5204PC84-5	5KCOUNT	Foundation Schematics with ABEL Modules.	5 Bit Counter
XC4005EPC84	4KMEM	Foundation Schematics with XBLOX components	5 Bit Counter and PROM + SRAM.

PROCEDURE

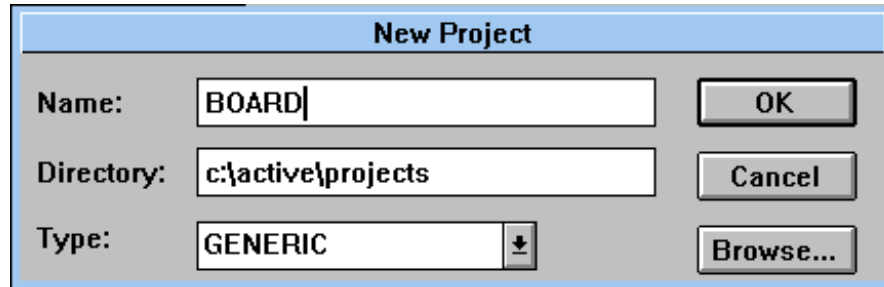
1) Design, place and route each device that is to be simulated.

For each case, ensure that the XACT 6.0 flow manager has the 'Produce Timing Simulation Data' option set in the Implementation dialogue box.



2) **Start the Foundation Project manager and create a new Generic project called BOARD.**


FILE -> New Project



3) **Attach the EPLD/FPGA symbol library and any other device libraries to the board level project.**

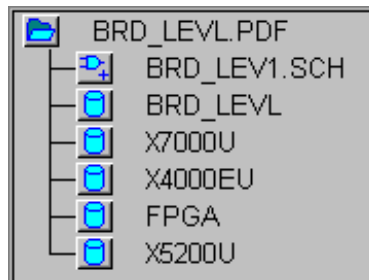
i.e. The following libraries would need to be attached to the 'BOARD' project:

XFPGA.	This is the library of symbols used to represent the FPGA's/EPLDs at the board level.
XC7000U	This provides simulation models for the back annotated 7KDECODE design
XC4000EU	This provides simulation models for the back annotated 4KEMEM design.
XC5000U	This provides simulation models for the back annotated 5KCOUNT design.


To do this click on the  icon in the Foundation Project Manager.

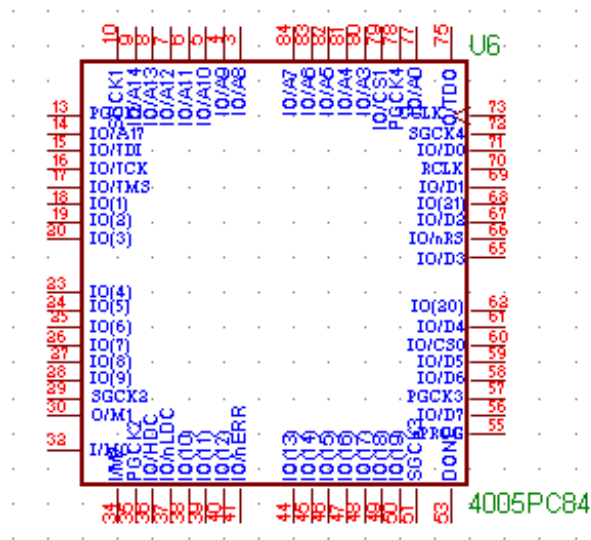
Double click on the desired library in the 'Attached Library' window. The library should migrate across to the 'Project Libraries' window.

Return to the Foundation Project Manager window and confirm that the libraries are attached.



4) **Add the appropriate FPGA/EPLD components to the BOARD schematic.**

- I) Start the Foundation Schematic Editor.
- ii) Use *FILE -> Page Setup* to select desired sheet size.
- iii) Click on the  icon to invoke component selection window and then add the the appropriate components. .



Example symbol of 4005PC84 with no underlying netlist

Note that the symbol pins are annotated with numbers AND generic pin descriptions.

5) **Assign a timing back annotated netlist to the symbol.**

The timing-annotated netlist for an EPLD is created by TSIM.EXE and is named TSIMTIME.XNF.

The timing-annotated netlist for an FPGA is created by XNFBA.EXE and is named XNFBA.XNF.

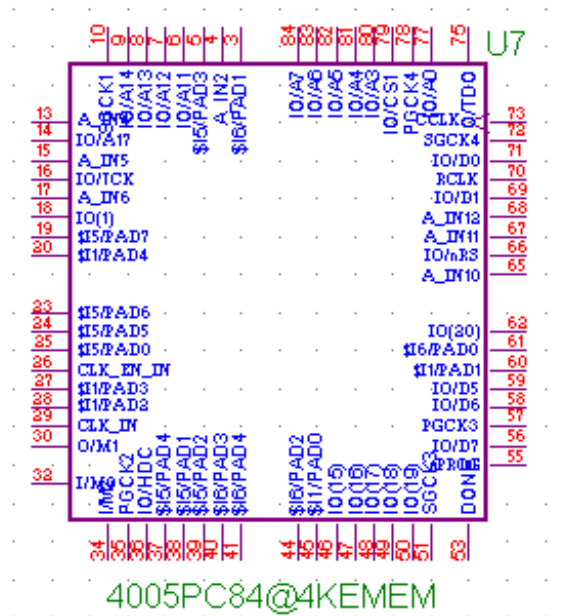
Each type of file is copied within its own project directory and renamed as *design.BAX* by the foundation software. Consequently it is always *design.BAX* that is assigned to a symbol, whether that symbol represents an EPLD or an FPGA.

To assign a netlist to a symbol,



- (i) Enter the Foundation Schematic editor and select *HIERARCHY -> Assign Netlist*.
- (ii) Use the mouse to identify which component is being assigned the netlist.
A 'Windows' selection window will pop up

- (iii) Navigate to the *dir:/ACTIVE/PROJECTS/design* directory that is represented by the selected FPGA/EPLD. Select the *design.BAX* file, and then click on OK.

There will be a flurry of activity as the .BAX netlist is assigned to the selected symbol. The symbol will then be updated as shown below.



- * Note that the symbol name is modified to reflect the netlist name.
- ** The symbol pin names are also updated to reflect the netlist I/O names.

- 6) Repeat steps 4(i) to 4(iii) for all FPGA/EPLD devices.
- 7) Establish Board level interconnect between the devices using nets and buses.
- 8) Simulate the design just like simulating a design for an individual FPGA or EPLD.
Click on the  icon to add probes, then click on the  icon to launch the simulator.

- 9) Annotating PCB track delays onto device pins.
 - Double click on an FPGA or EPLD symbol.
 - Click on the Pin Parameters button to launch the Pin Parameter window.
 - Select a pin from the pin list.
 - Enter LDEL in the Name: window.
 - Enter 100PS in the Description: window.
 - Click on the Add button to see the entries moved to the Parameters window.
 - Unfortunately you will be unable to show which pins have had delays added, because this feature has been turned off. The reason is related to importing Viewlogic symbols.
 - A delay of 100PS has now been added to the selected pin.