

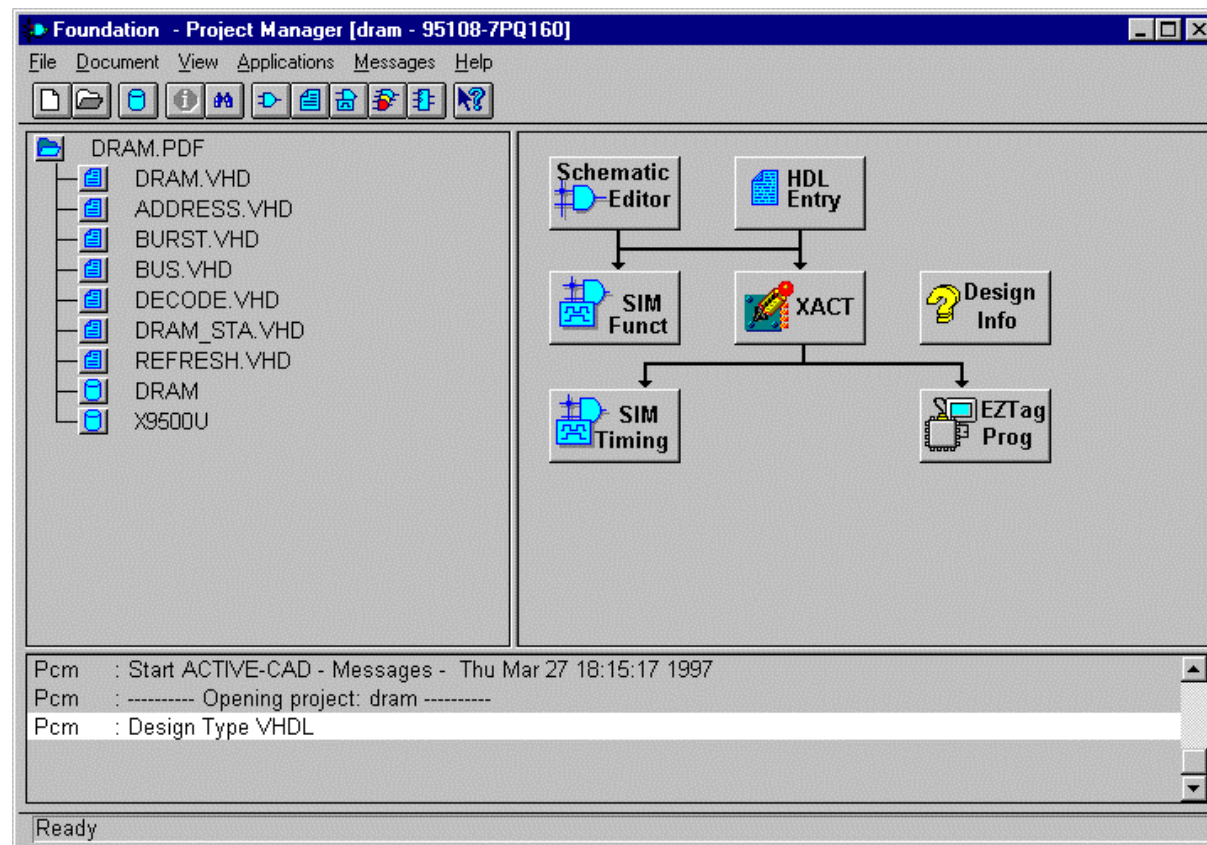
Demonstration Screens

CPLD Demo Using Foundation VHDL Tools

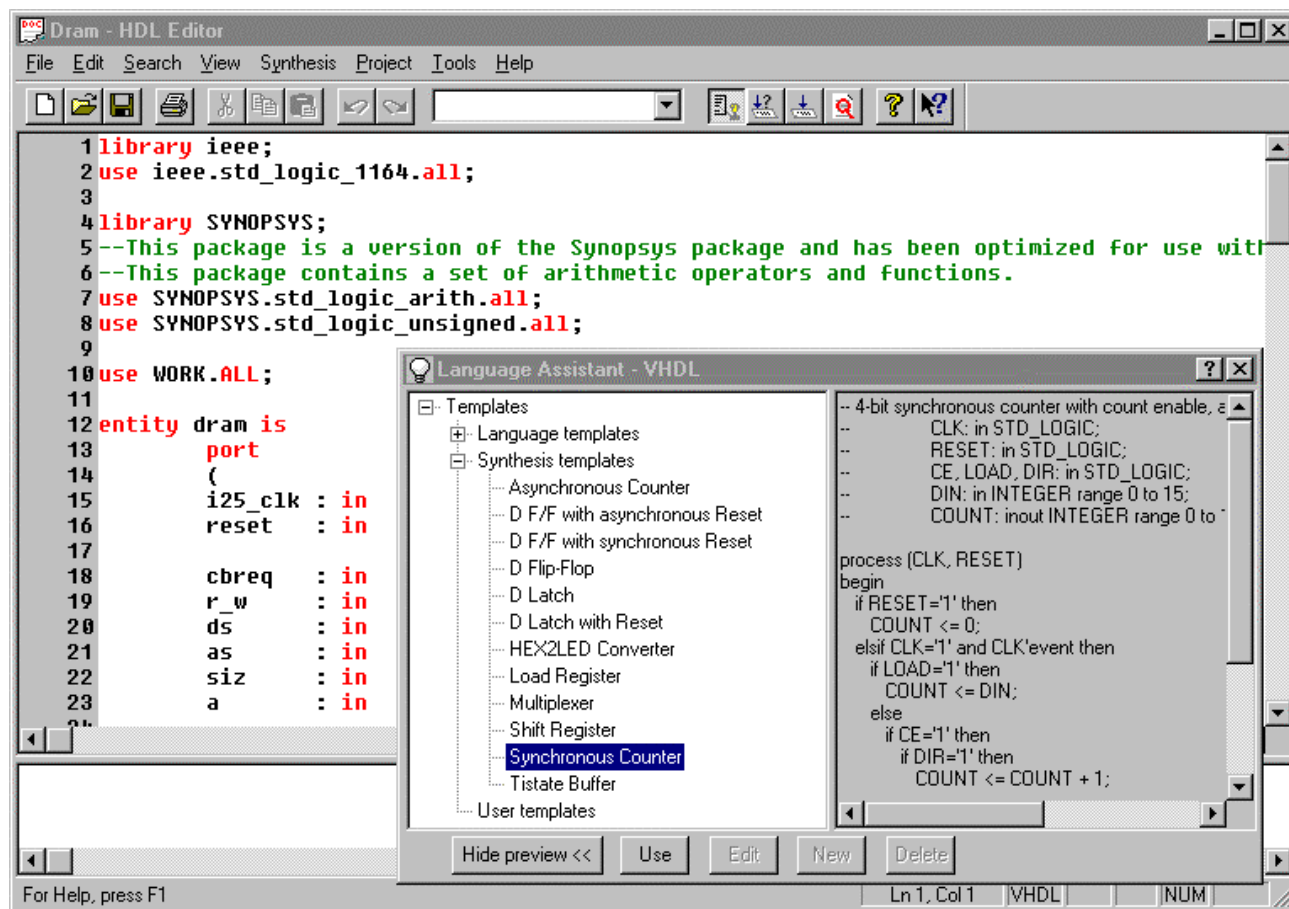
Foundation Project Manager Using VHDL

**VHDL Files
used**

**Library Files
used**



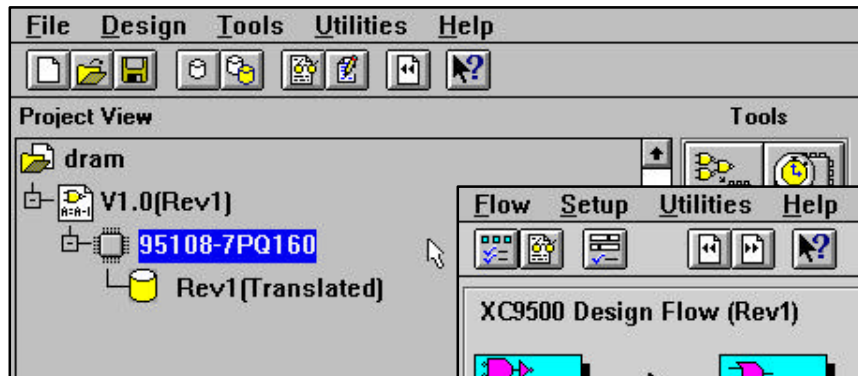
HDL Language Assistant Templates & Libraries



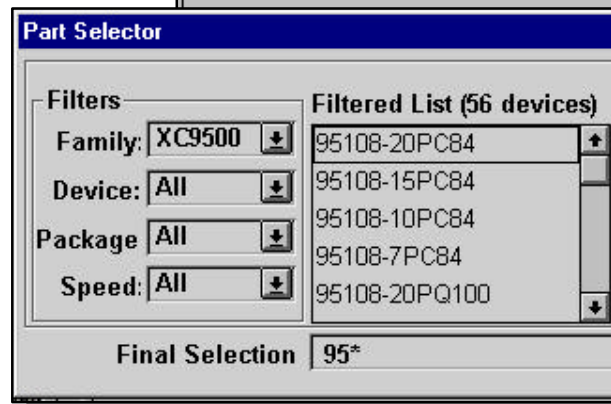
XC9500 Fitter Tools

Easy as 1...2...3

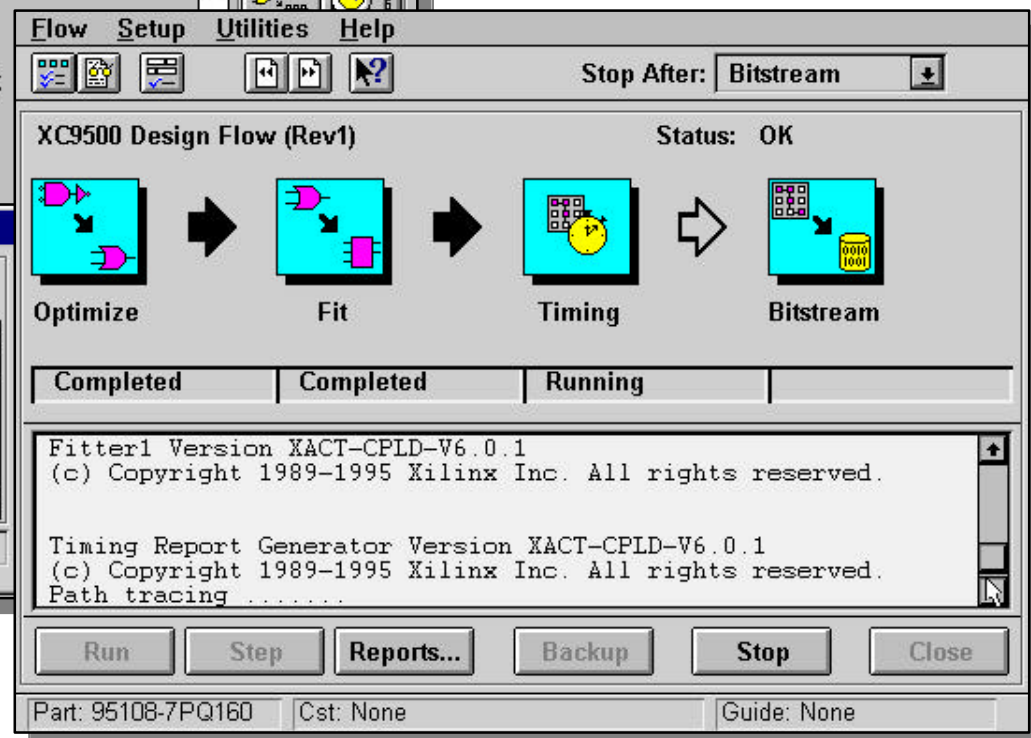
1.



2.



3.



Fitter Report

Shows You What You Need To Know

Translation Report
Fitting Report
Timing Report

XEPLD, Version XACT-CPLD-V6.0.2d

Design Name: dram

Fitting Status: Successful

PIN RESOURCES:

Signal Type	Required
Input	32
Output	20
Bidirectional	0
GCK	1
GTS	0
GSR	1
Total	54

Xilinx Inc.

Fitter Report

Date: 3-30-97, 10:04PM

***** Resource Summary *****

Design Name	Device Used	Macrocells Used	Product Terms Used	Pins Used
dram	XC95108-7PQ160	62 / 108 (57%)	210 / 540 (38%)	54 / 108 (50%)

***** FB3 *****

Number of function block inputs used/remaining: 36/0

Number of signals used by logic mapping into function block: 36

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pwr Mode	Pin #	Pin Type	Pin Use
REFRESH_MACHINE/REF7	1	0	^1	3	FB3_1	STD	25	I/O	(b)
WE<1>	10	5<-	0	0	FB3_2	STD	17	I/O	0
REFRESH_MACHINE/COUNTER<6>	1	1<-	^5	0	FB3_3	STD	31	I/O	I
REFRESH_MACHINE/COUNTER<5>	1	0	^1	3	FB3_4	STD	32	I/O	I
WE<0>	9	4<-	0	0	FB3_5	STD	19	I/O	0
REFRESH_MACHINE/COUNTER<4>	1	0	^1	0	FB3_6	STD	34	I/O	I
M_A<2>	2	0	0	3	FB3_7	STD	35	I/O	0
REFRESH_MACHINE/COUNTER<3>	1	0	0	4	FB3_8	STD	21	I/O	I
REFRESH_MACHINE/COUNTER<2>	1	0	0	4	FB3_9	STD	26	I/O	I
M_A<6>	2	0	0	3	FB3_10	STD	40	I/O	0
REFRESH_MACHINE/COUNTER<1>	1	0	0	4					

Flexible P-Term
Cascading

CPLD DEMO - 5

Timing Reports

User-Customized Summaries

Minimum Clock Period: 13.5ns
Maximum Internal Clock Speed: 74.0Mhz
(Limited by Cycle Time)

Estimated Maximum External Clock Speed: 71.4Mhz
(Limited by Clock Pad to Output Pad)

Combinational Pad to Pad Delays(nsec)												
From	A	A	A	A	A	A	A	A	A	A	A	A
<	<	<	<	<	<	<	<	<	<	<	<	<
1	1	1	1	1	1	1	1	1	1	1	2	2
0	1	2	3	4	5	6	7	8	9	0	1	2
>	>	>	>	>	>	>	>	>	>	>	>	>
To												
M_A<0>				7.5								
M_A<10>					7.5							
M_A<1>			7.5									
M_A<2>				7.5								
M_A<3>					7.5							
M_A<4>						7.5						
M_A<5>							7.5					
M_A<6>								7.5				
M_A<7>									7.5			
M_A<8>	7.5									7.5		
M_A<9>		7.5									7.5	