

Agenda

- The Future of Programmable Logic
- Product Overview
- Design Methodology Case Studies
- **The Next Generation**
- Summary / Q&A

Technology Leadership

- Today: Outstanding PLD solutions
 - XC9500: Pin locking, ISP, low price
 - XC4000E: World's fastest 5 V FPGA
 - XC4000XL: World's fastest and largest FPGA (3.3 V)
 - XC4000XV: World's first 0.25 μ FPGA
- Future: Next Generation FPGAs
 - Extending density and performance
 - Address system solution issues
 - Platform for LogiCORE (IP) reuse
 - High-level software design tools

Next Generation: A True System Solution

■ Density and Performance

- <20K to 400K gates, 1,500-32,000 logic cells, 100+ MHz clock rates

■ System Performance

- Clocking, PLL, external timing control, RAM performance

■ System interfaces

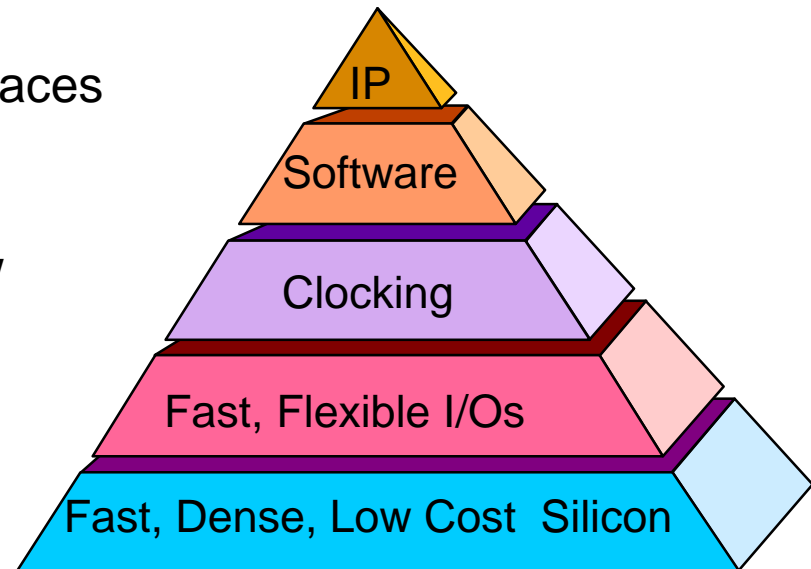
- Fast I/Os, mixed 3 V / 5 V interfaces

■ Software

- Best fit into ASIC synthesis flow
- Constraint-driven tools

■ Intellectual property

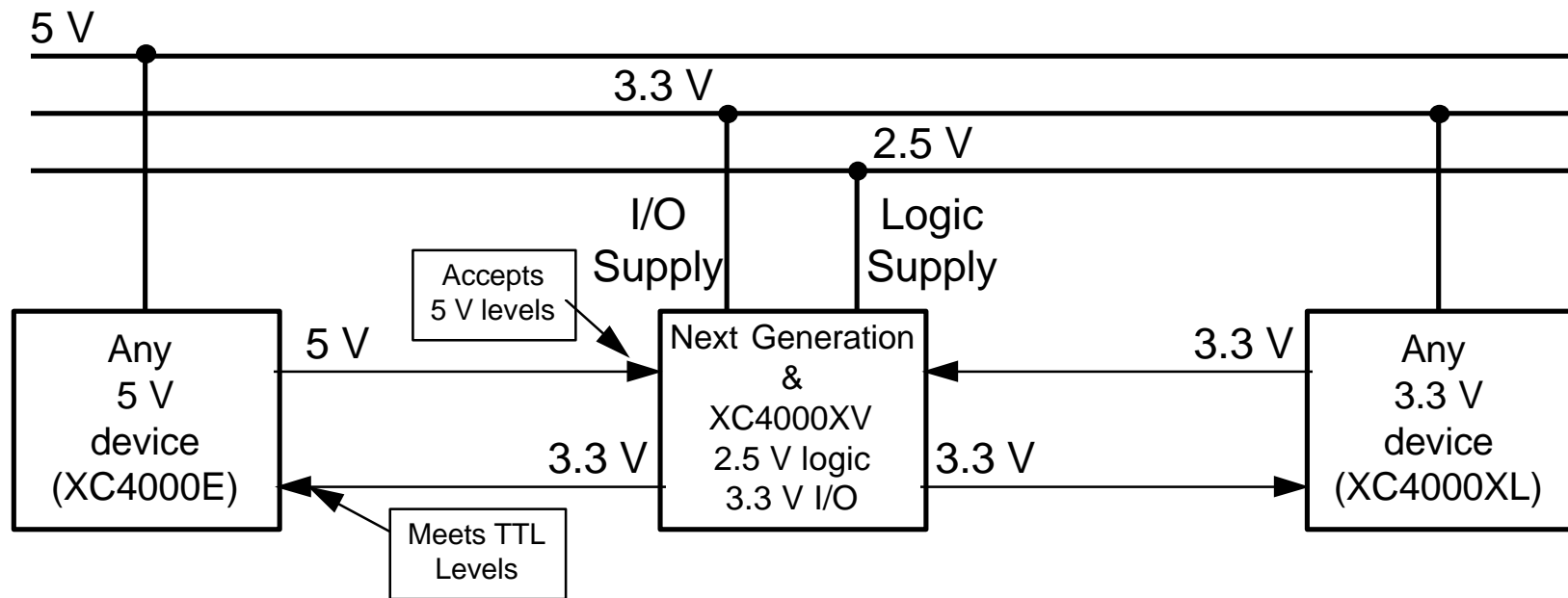
- Ideal CORE delivery platform



Voltage and Family Migration

- Next Generation FPGAs and XC4000XV share common process (0.25 μ)
 - 2.5 V logic, 3.3 V I/O with 5 V tolerance
- Family migration from XC4000XL possible
 - Voltage migration guide will assist users
- Design with XC4000XL now and plan ahead for XC4000XV and Next Generation FPGAs

Xilinx 0.25 μ , 5 Volt-Compatible FPGAs



- Family migration possible if you plan for:
 - Additional power/ground pins
 - Dedicated clock and configuration pins
- Voltage migration guide to help users

Next Generation Software Strategy

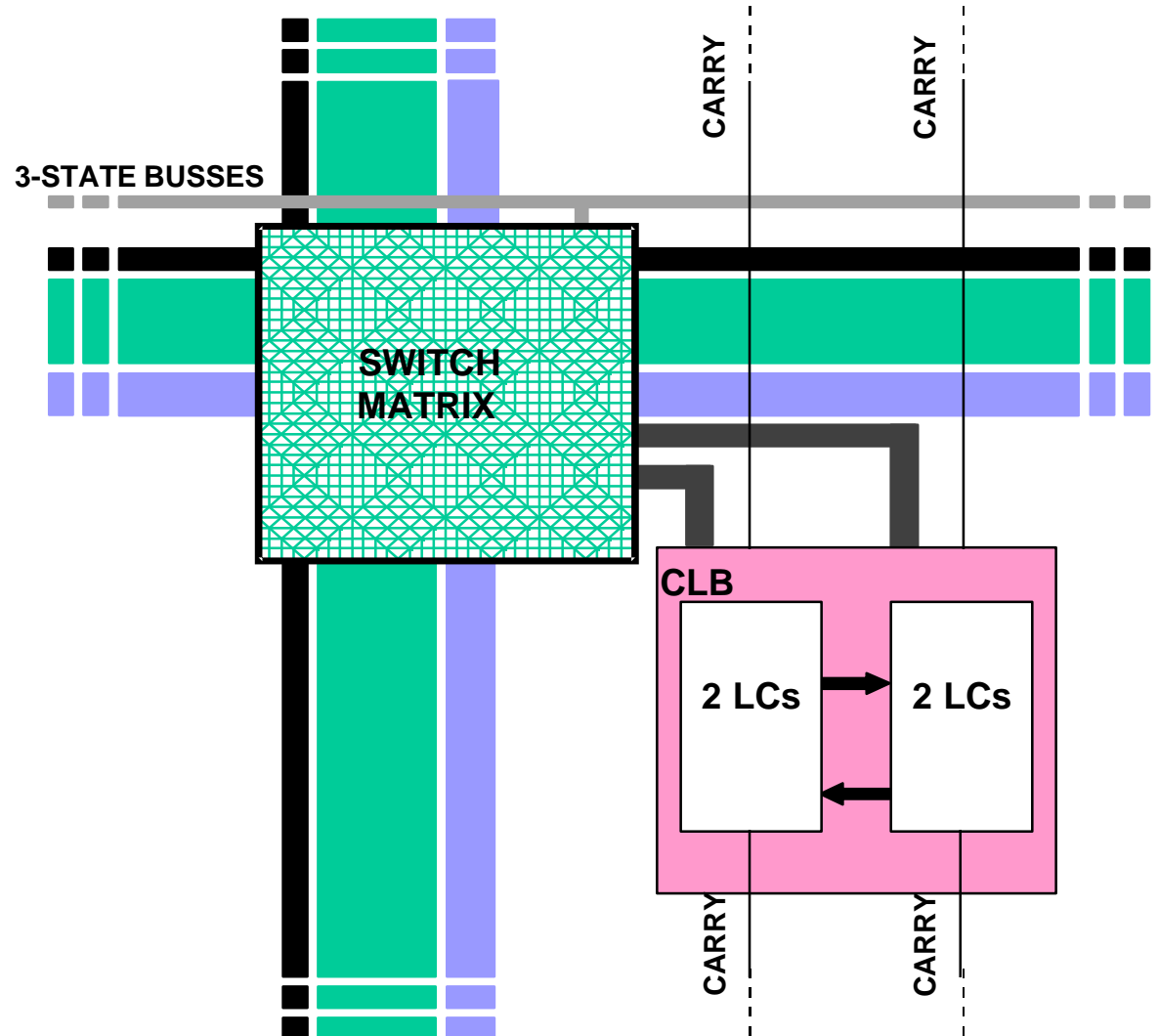
- As design size grows, synthesis design flow support becomes vital
- Software flows have been designed around synthesis design flows
 - Schematic design is still supported
- Support team-based design and intellectual property reuse

Next Generation Software Solutions

- Leading FPGA synthesis tools now work with 4-input look up tables (LUTs)
 - Building block for XC4000X and Next Generation FPGAs
- Software will be based on M1 XC4000X tools
 - Builds on history of robust EDA tool integration
 - Emphasizes constraint-driven design philosophy
 - Fast and predictable interconnect allows accurate design analysis early in the design flow

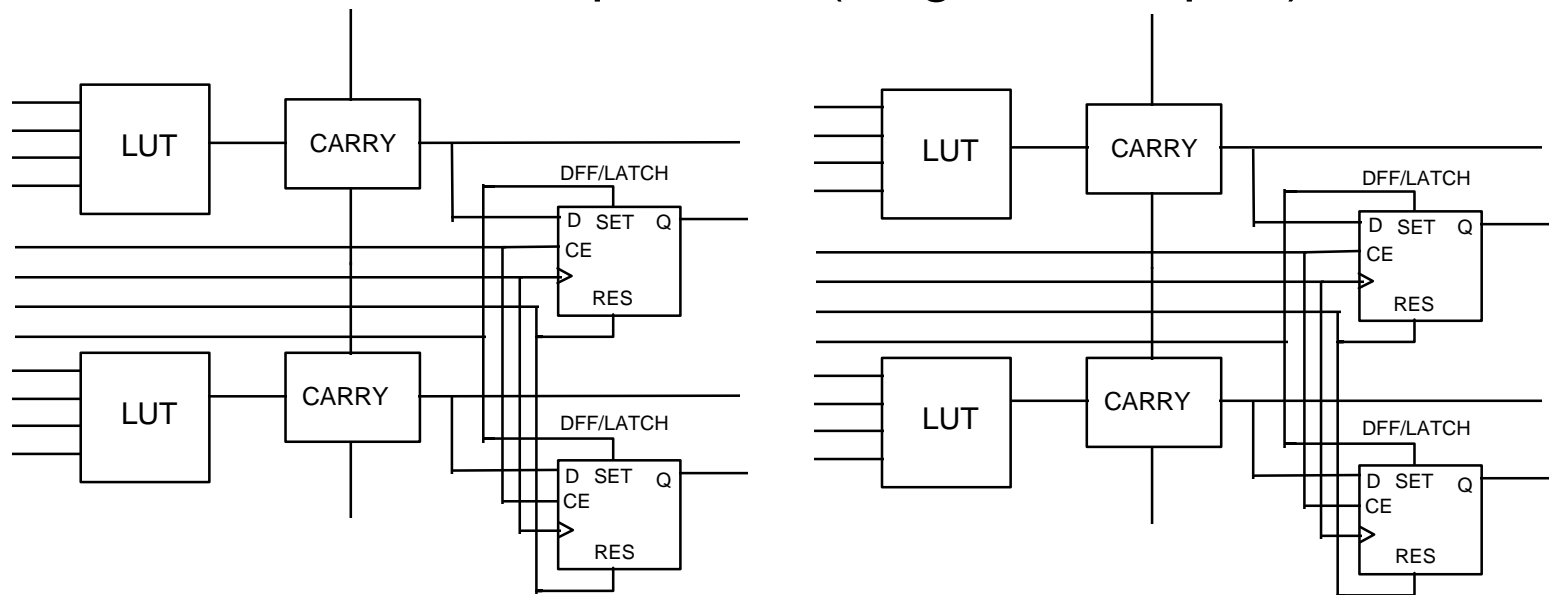
Logic and Interconnect

- 4 LCs per CLB
- Fast local routing within CLBs
- General purpose routing between CLBs
- Hierarchical interconnect is scaleable, and has predictable fast performance



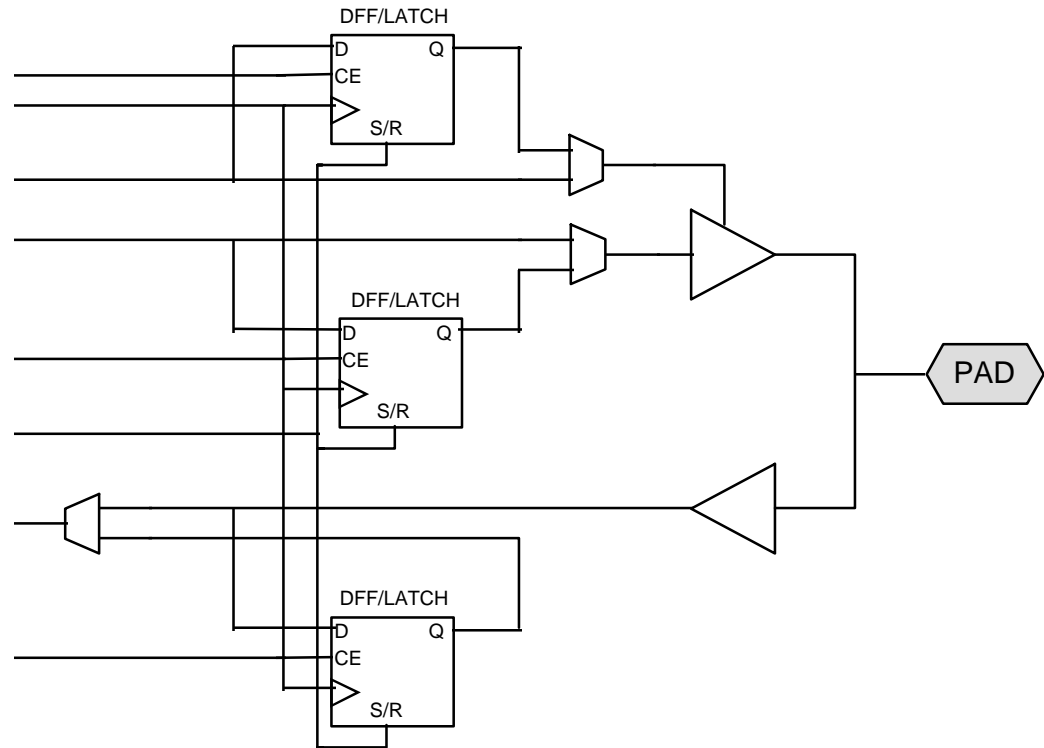
Simplified CLB

- 4 Logic Cells per CLB
- Carry logic (2 independent chains)
- 4 FFs/Latches, 2 BUFTs per CLB
- 16 bits of SelectRAM per LUT (single / dual-port)



Simplified IOB

- Fast I/O drivers
- Registered input, output, 3-state enable control
- Programmable slew rate, pull-up, input delay, etc.



System Solution Features

- Arithmetic support
 - High-speed carry logic
- Clocking and PLL
 - Match I/O performance to fast internal speed
- RAM hierarchy
 - SelectRAM identical to XC4000X
 - Block RAM on chip
 - Fast access to large external RAM

Clocking and PLL

- Ultra-low skew, fast clocks
 - 66 MHz PCI performance without PLL
- Phase-Locked Loop (PLL)
 - Compensate for clock network delay
 - Clock multiplication
 - Duty cycle correction
 - Reference output for system timing

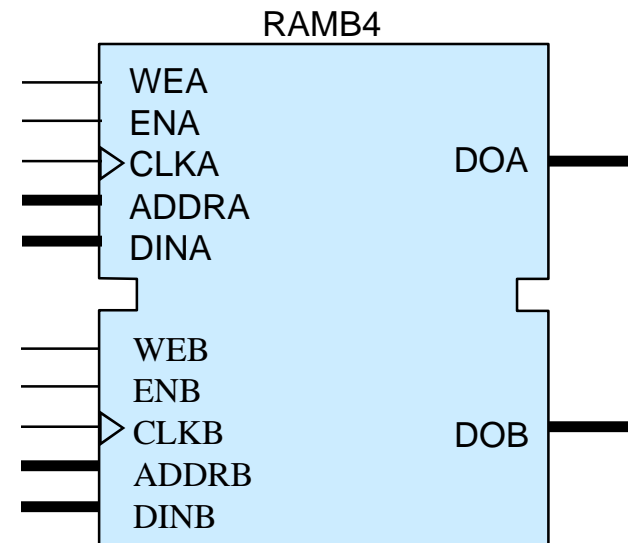
Xilinx Next Generation FPGAs Deliver World-Class Performance

- 100+ MHz system interface speeds
- 100 MHz internal speeds (3-4 levels of logic)
- Performance

	without PLL	with PLL
– Tco (output register)	6 ns	3.5 ns
– Tsu (input register)	3 ns	3 ns
– Th (input register)	0 ns	0 ns
– Max I/O performance	110 MHz	160 MHz

Block RAM

- Configure as: 4096 bits with variable aspect ratio
- 8-30 blocks per device (20K-200K logic gate devices)
- True dual-port, fully synchronous operation
 - Cycle time <10 ns
- Flexible block RAM configuration
 - 5 blocks: 2K x 10 video line buffer
 - 1 block: 512 x 8 ATM buffer (9 frames)
 - 4 blocks: 2K x 8 FIFO
 - 9 blocks: 4K x 9 FIFO with parity



Next Generation FPGA Summary

- Next Generation FPGAs open new applications
 - 66 MHz PCI @ 3.3 V
 - 155 MHz SONET data stream processing
- 100+ MHz system speeds,
1.6K-32K logic cells, (20K-400K logic gates)
- Hierarchy of RAM solutions
 - SelectRAM, block RAM, efficient external RAM interface
- Synthesis-friendly design flows
- Excellent platform for CORE reuse