

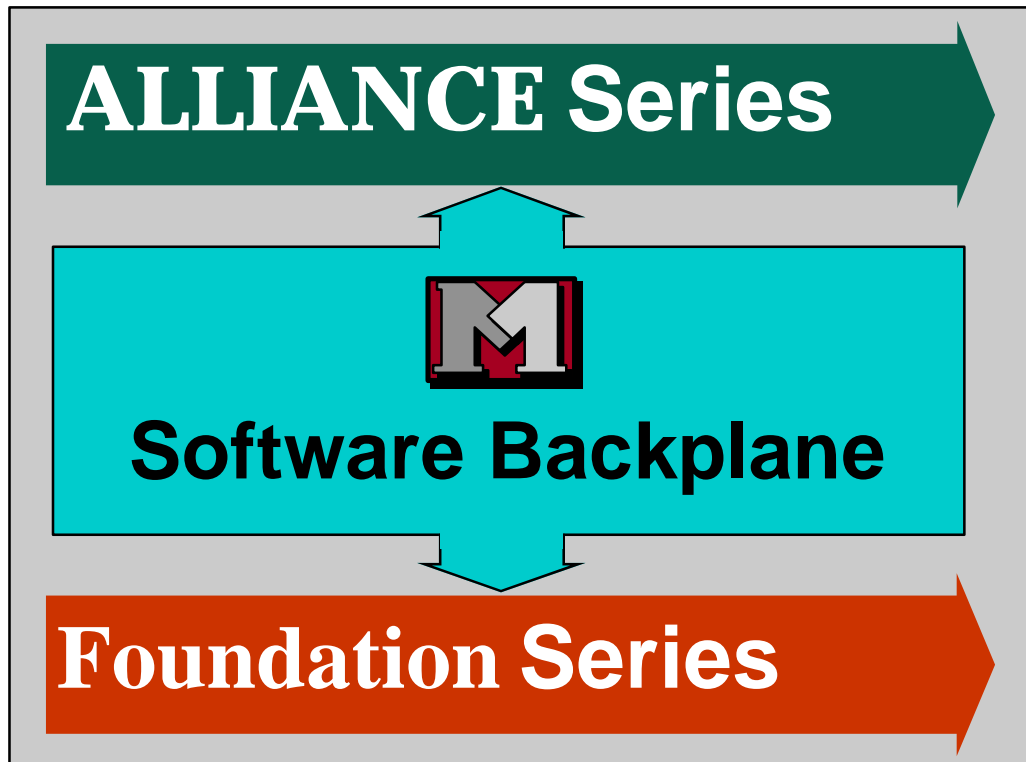
# Agenda

- The Future of Programmable Logic
- **Product Overview**
- Design Methodology Case Studies
- The Next Generation
- Summary / Q&A

# **Xilinx Product Solutions**

- M1 software solutions
- Xilinx CORE solutions
- XC4000X series
  - Industry's largest and fastest FPGAs
- XC4000E - Industry's fastest 5 V FPGAs
- Low-cost solutions
  - XC5200
  - HardWire
- XC9500 - Flash-based ISP CPLDs

# Alliance and Foundation Series Software Leverage Advances in M1 Software Backplane



**Open Systems Integration**

**Libraries and Interfaces for  
Leading EDA Vendors**

**Complete, Ready-to-Use**

**Includes Schematic, Simulation,  
and VHDL Synthesis**



# Software Backplane Design Flows



**Integration**



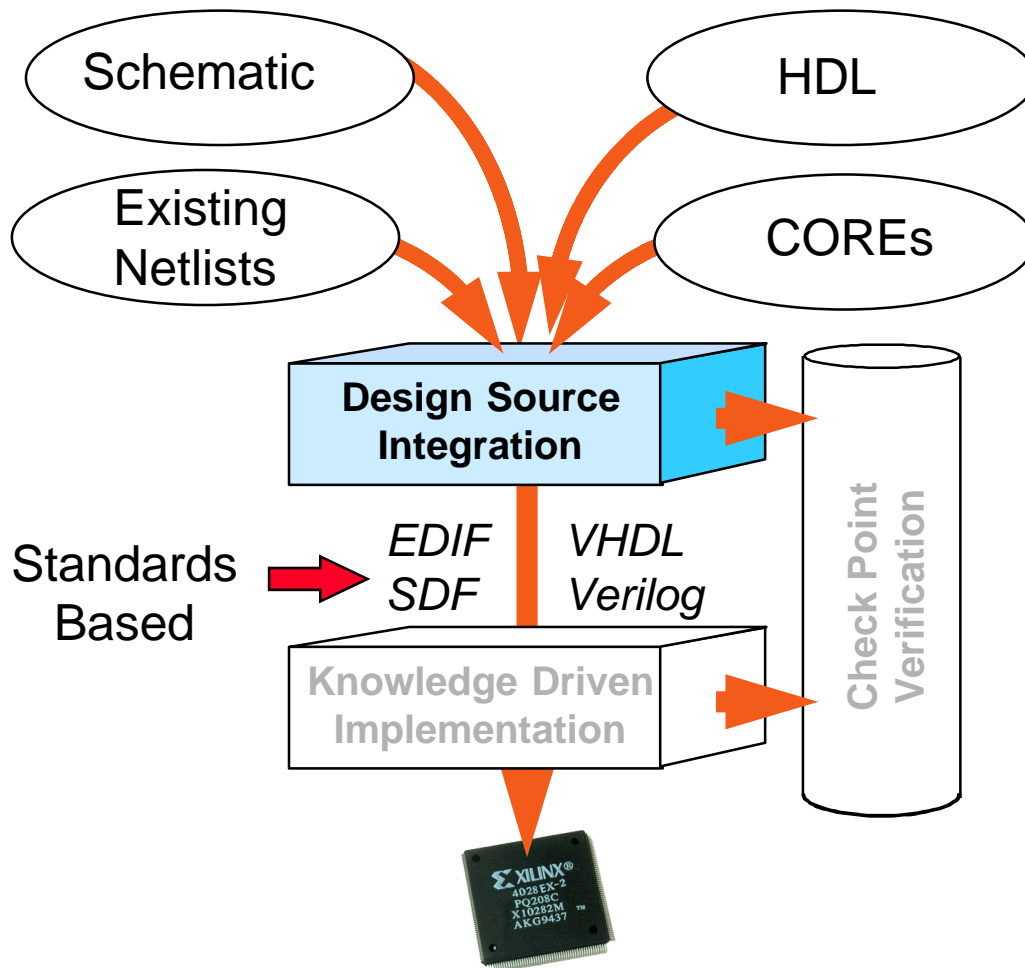
**Implementation**



**Verification**

- Mixed-level design flows
- Standards-based infrastructure
- Interfaces for leading EDA vendors
- Automatic, push-button flows
- Intuitive control of automatic tools
- Combines user and tool knowledge
- Function and timing verification
- Multiple verification points and methods
- Test bench template generation

# Design Source Integration



- ◆ Enables multiple EDA tools in the same flow
- ◆ Allows *team-based* development
- ◆ Required for complex high-density designs

# Knowledge-Driven Implementation

## Designer Knowledge

- Design structure
- Performance requirements
- **SMART specs**
  - Total control over timing-driven tools

*and*

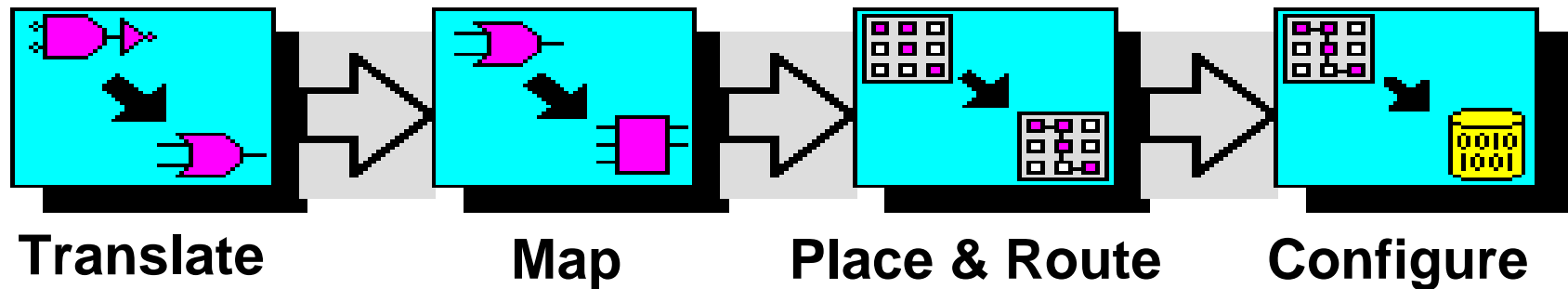
## Powerful Design Tools

- Push-button, timing-driven
- Recognize design **structure**
- **SMART guide**
  - Use previous design results
  - More successful turns per day

*Users focus on design innovation*

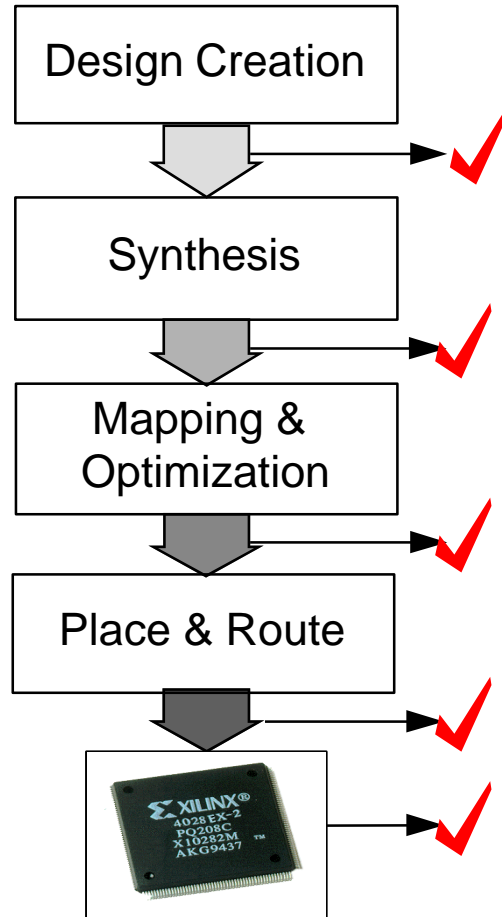
*Leave implementation details to the software*

# Automatic Push-Button Flows



- Logical DRC *detects errors early*
- Automatic structured placement
- Advanced, timing-driven place and route algorithms

# Check-Point Verification



- Versatile verification points and mechanisms
- Based on industry standards
- Automatic HDL test bench template generation
- Powerful in-circuit debugging

***Shortens Development Cycles***



# Alliance Series

## Provides EDA Vendor Integration



SYNOPSYS®

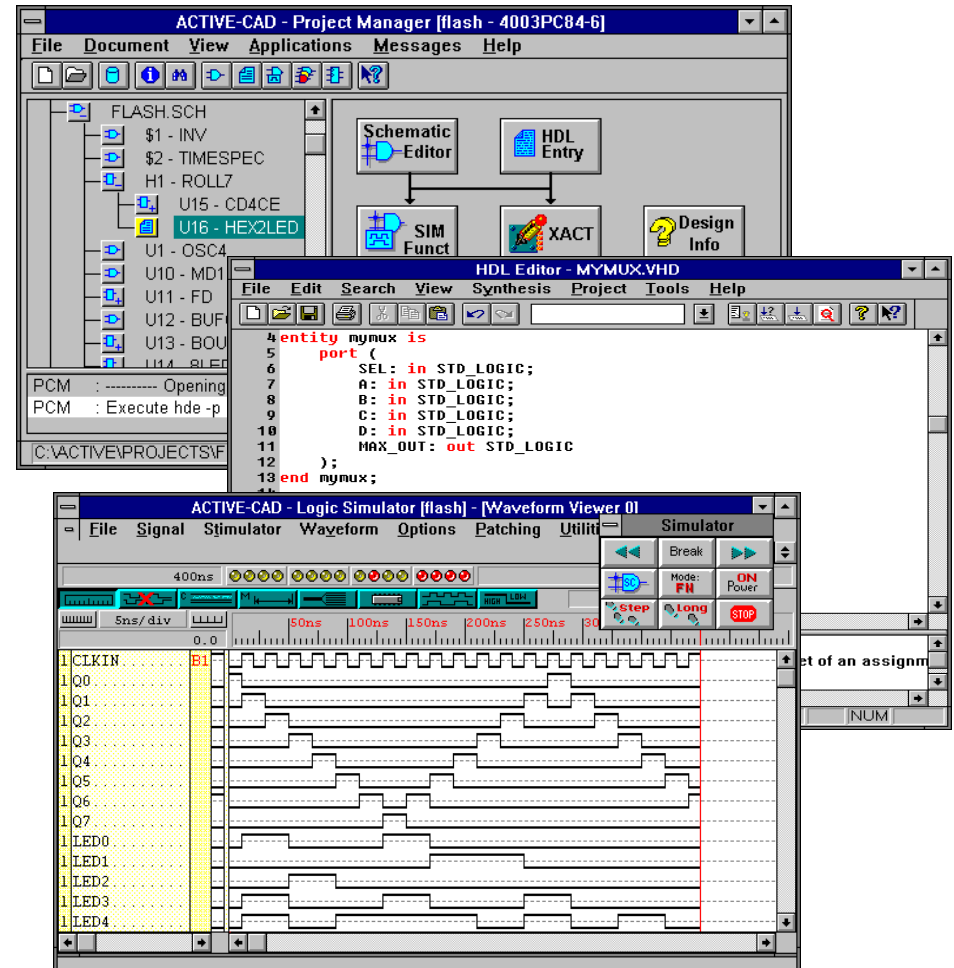


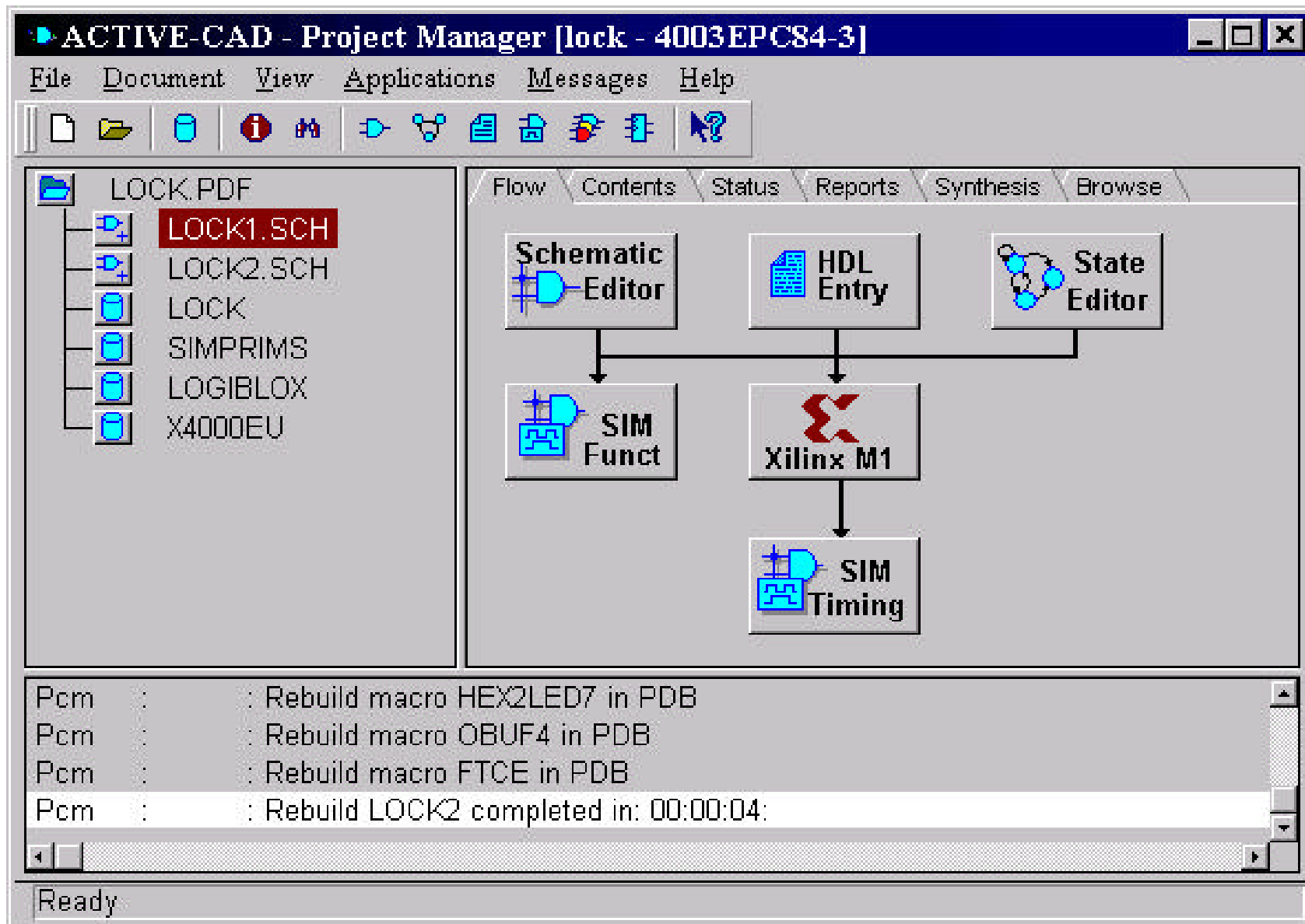
*"Technology Through Teamwork"*

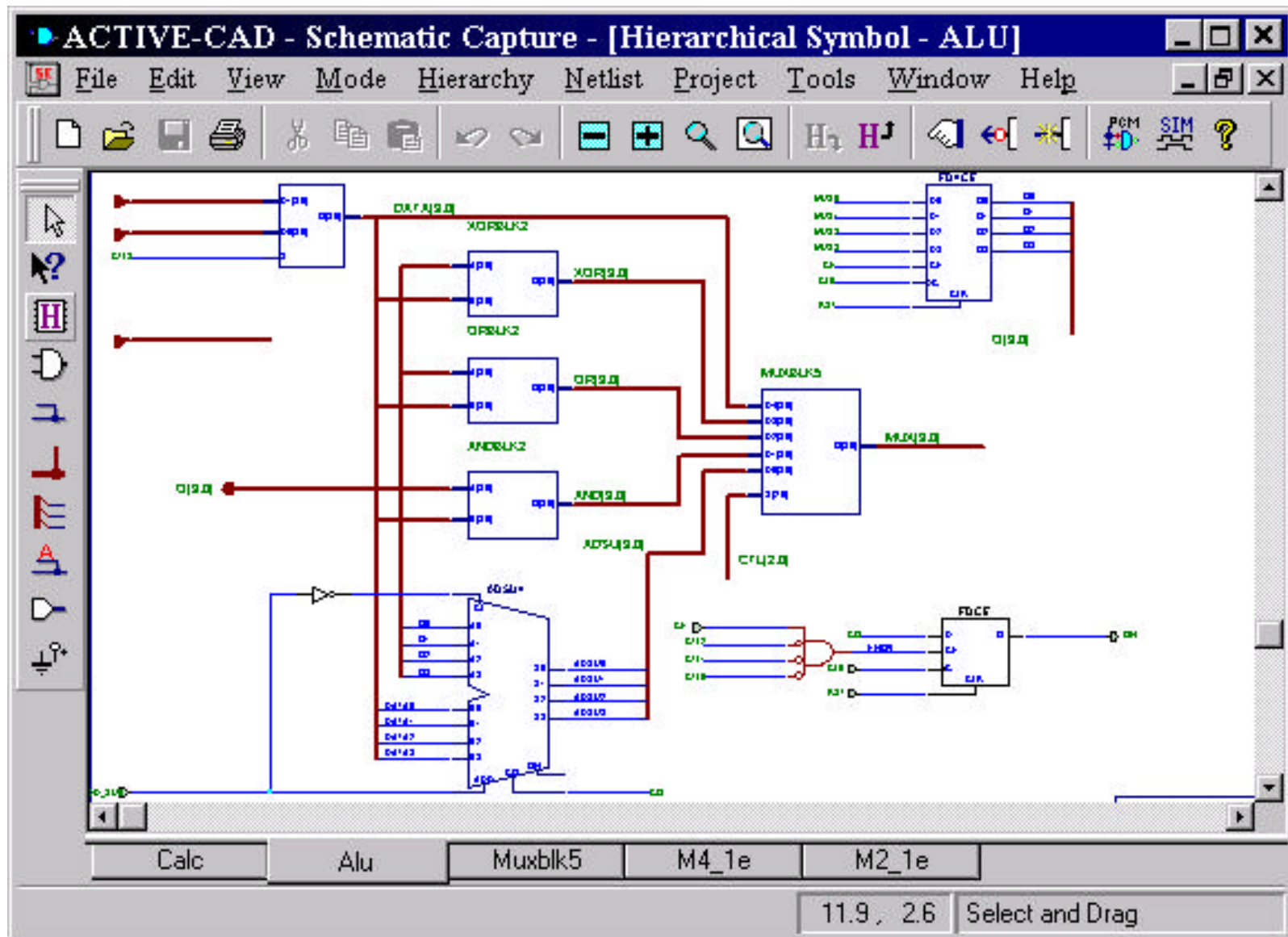
- ◆ Standards-based design flow integration
- ◆ Interface kits for popular EDA vendors
- ◆ Joint definition of next-generation design flows and technology

# Foundation Series Delivers Value & Ease of Use

- Complete, ready-to-use software solution
- Simple, easy-to-use design environment
- Easy-to-learn VHDL design
- Best-value software solution







### control.asf - State Editor

File Edit Search View FSM Draw

control\_fsm

For Help, press F1

### Compar.vhd - [Macro COMPAR] - HDL Editor

File Edit Search View Synthesis Project Tools Help

```

14      RESET: in      STD_LOGIC ;
15      CIN:   in      STD_LOGIC_VECTOR (3 downto 0) ;
16      B_LD:  in      STD_LOGIC ;
17      BIN:   in      STD_LOGIC_VECTOR (3 downto 0) ;
18      AIN:   in      STD_LOGIC_VECTOR (3 downto 0) ;
19      EQ_CB: out     STD_LOGIC ;
20      EQ_ABREG: out   STD_LOGIC
21    );
22  begin
23  end compar ;
24
25  architecture
26
27  signal B_reg:
28  begin

```

Checking...  
Error 219 L27/C25 :  
1 error(s) 0 warning(s)

For Help, press F1

#### Design Wizard - Ports

To create a new port click New.

To change attributes of a port, select it on the list. Then you can change its name, range and direction; to set other attributes click Advanced.

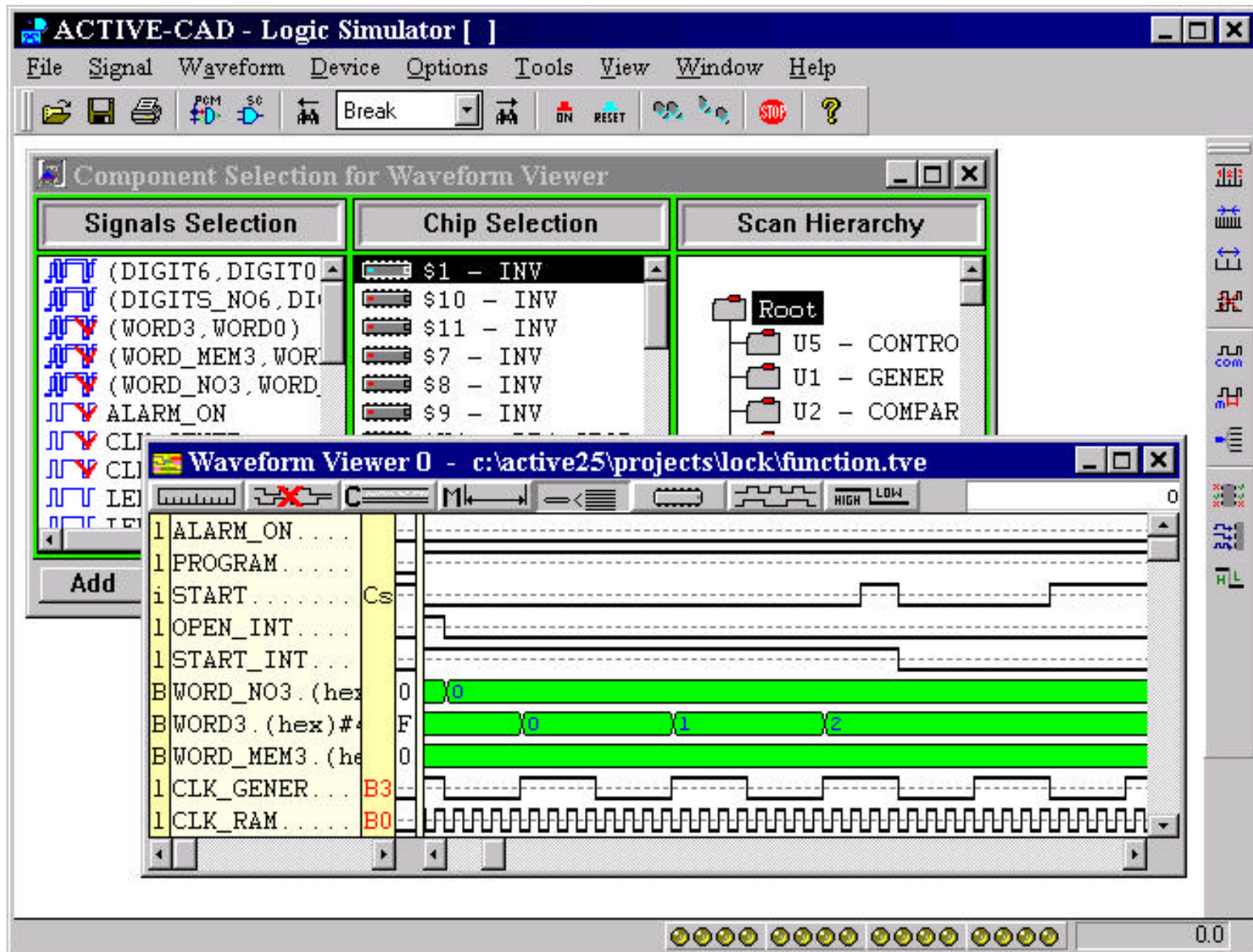
To delete a port select it on the list and click Delete.

Name	Bus	Direction
a		<input type="radio"/> Input <input checked="" type="radio"/> Output <input type="radio"/> Bidirectional
b		
c		
clk		
d		
q[3:0]		
t[7:0]		

Buttons: New, Delete, Advanced...

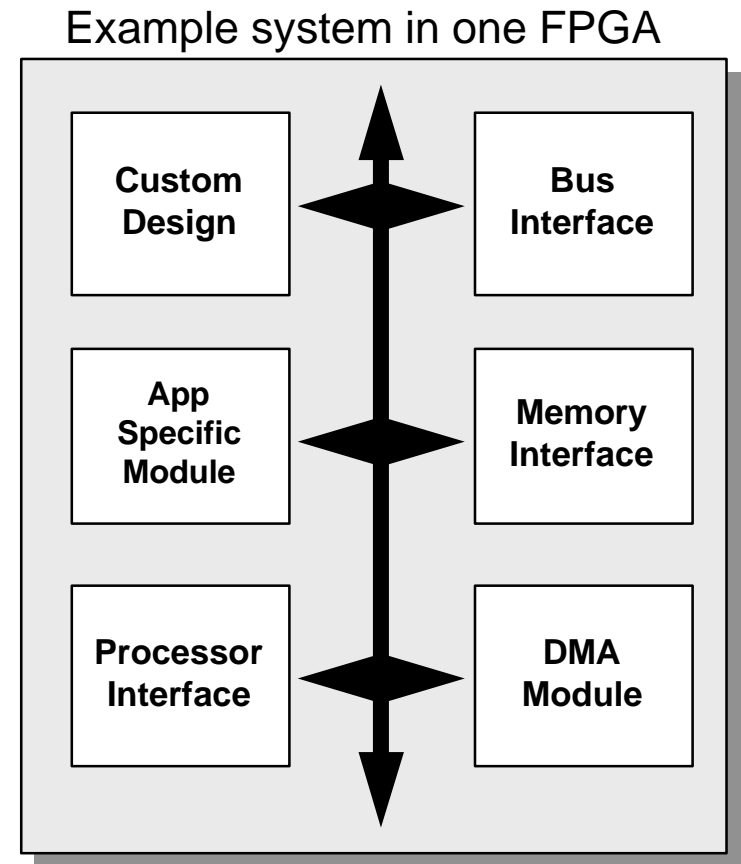
Bottom Buttons: < Back, Finish, Cancel






# COREs are Critical for High-Density FPGA Design

- For 50K+ gate ASICs, COREs are essential
- 50K+ gate FPGAs are here
  - Requires ASIC design methods
- COREs essential for time-to-market
  - Reduce design time & risk
  - Reduce compile time



# Xilinx CORE Solutions

- Expand availability of cores through partnerships
- Provide enabling technologies
- Build support infrastructure - 3rd party design centers

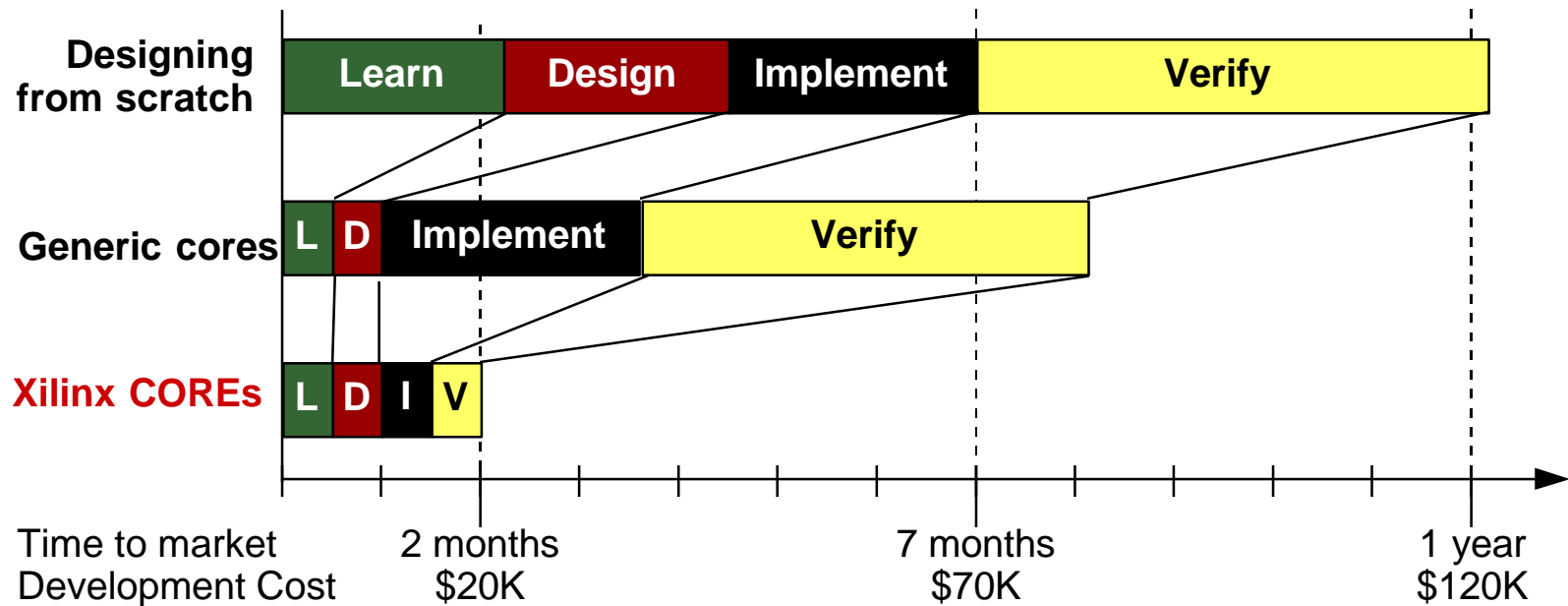
	LogiCORE™	 AllianceCORE	Reference Designs	LogiBLOX	3rd-Party Design Centers
Bus Interfaces	✓	✓			✓
DSP Functions	✓	✓			✓
Communications Networking		✓	✓		✓
Base Functions		✓		✓	



# **Xilinx CORE Solutions Meet FPGA User Needs**

- **Proven performance**
  - Reduced design time
- **Fully verified**
  - Lowest design risk
- **Optimized for Xilinx architecture**
  - Best performance
  - Best utilization
- **CORE generator technology**
  - Industry's first Web-based FPGA tool
  - Easy to customize, integrate
  - EDA tool independent

# Xilinx COREs Reduce Time-To-Market



*What is your real cost of being late to market?*

Note: Data based on 200 licenses of Xilinx PCI LogiCORE over 1 year

# CORE Roadmap: Xilinx and AllianceCORE Partners

## 1997

Standard Bus Interfaces	<ul style="list-style-type: none"> <li>• PCI 32bit (LC)</li> <li>• PCI 64bit (LC)</li> <li>• ISA PnP (RF)</li> <li>• VME</li> <li>• USB (AC)</li> <li>• Cardbus (AC)</li> <li>• PCMCIA (AC)</li> <li>• CAN Bus (AC)</li> </ul>
DSP Functions	<ul style="list-style-type: none"> <li>• DSP building blocks (LC)</li> <li>• Fast multipliers (LC)</li> <li>• FIR, IIR, FFT/DFT, DCT (LC)</li> <li>• Reed-Solomon (AC)</li> <li>• Trig functions, Math</li> </ul>
Communication & Networking	<ul style="list-style-type: none"> <li>• UTOPIA, 25/33MHz (AC)</li> <li>• Cell delineation</li> <li>• HEC</li> <li>• CRC-3C</li> <li>• T1/E1</li> <li>• HDLC</li> </ul>
Base-level Functions	<ul style="list-style-type: none"> <li>• 82xx, UARTs, DMAs, Interrupt controllers (AC)</li> <li>• Memory interfaces (LC)</li> </ul>

LC: LogiCORE, AC: AllianceCORE, RF: Reference Design

Unmarked: Generic COREs available from partners, not fully productized for Xilinx FPGAs

# CORE Roadmap: Xilinx and AllianceCORE Partners

**1998**

<b>Standard Bus Interfaces</b>	<ul style="list-style-type: none"> <li>• PCI 66 MHz (LC)</li> <li>• <b>FireWire (100-400 Mbps) (AC)</b></li> <li>• Emerging interfaces</li> </ul>
<b>DSP Functions</b>	<ul style="list-style-type: none"> <li>• High speed DSP functions &gt;100 MSps</li> <li>• New emerging multimedia applications</li> <li>• Satellite Decoders</li> <li>• MPEG</li> </ul>
<b>Communications &amp; Networking</b>	<ul style="list-style-type: none"> <li>• 100Mb/1Gb Ethernet</li> <li>• ATM SAR</li> <li>• UTOPIA (50 MHz)</li> <li>• ADSL</li> </ul>
<b>Base-level Functions</b>	<ul style="list-style-type: none"> <li>• Micro sequencer</li> <li>• RISC processor</li> <li>• Microprocessor interfaces</li> </ul>

**LC: LogiCORE, AC: AllianceCORE**

Unmarked: Generic COREs available from partners, not fully productized for Xilinx FPGAs

# 19 Xilinx Product Families

XC3000 ⇔ XC3000A

XC3000A popular, no RAM

XC3000L 3.3 V

XC3100 ⇔ XC3100A

XC3100A fast, no RAM

XC3100L 3.3V

XC4000 ⇔ XC4000E

XC4000L 3.3 V

**XC4000E fastest 5-V FPGA**

**XC4000EX 5-V FPGA**

**XC4000XL largest and fastest**

**XC4000XV 2.5 / 3.3 V**

**HardWire Arrays**

**XC5200 low-cost, no RAM**

**XC5200L low-cost, 3.3 V**

XC6200 Reconfigurable co-processor

XC7300 EPROM CPLD

**XC9500 ISP CPLD**

XC17000 Serial PROM

1500+ different  
device / speed / package / temperature  
combinations

## **Not Covered in this Seminar**

- High-Rel and military market
  - Xilinx remains committed
  - Cost-effective replacement for gate arrays
  
- Reconfigurable computing
  - XC6200 family is optimized
  - XC3000 and XC4000 are also popular
  - Web info available (see Appendix A)

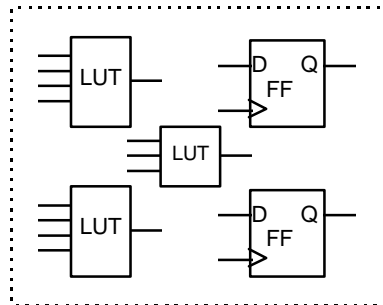
## **Xilinx IC Product Solutions**

- **XC4000X series - Industry's largest and fastest FPGAs**
  - XC4000EX - 0.5  $\mu$ , 5 V devices
  - XC4000XL - 0.35  $\mu$ , 3.3 V devices, 5 V compatible I/O
  - XC4000XV - 0.25  $\mu$ , 2.5 V / 3.3 V devices, 5 V compatible I/O
- **XC4000E - Industry's fastest 5 V FPGA**
- **Low-cost solutions**
  - XC5200
  - HardWire
- **XC9500 - Flash-based ISP CPLD family**
  - Lowest price, best pin locking

# Logic Cells: Industry-Standard Density Metric

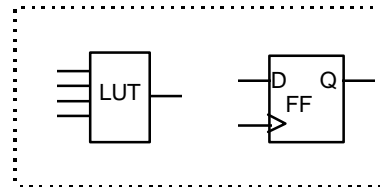
- 1 LC = 4-input LUT + FF
- Unambiguous unit of measurement
- Consistent across families and manufacturers

Xilinx XC4000 CLB



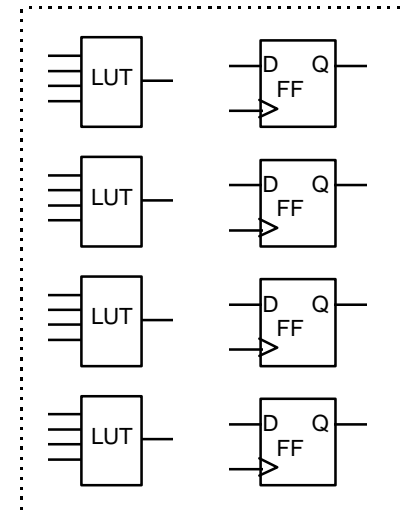
1 CLB = 2.3 LCs

Altera FLEX LE



1 LE = 1 LC

Lucent ORCA2 PFU



1 PFU = 4 LCs

Example devices:

XC40125XV (10,982 LCs)

EPF10K100 (4992 LCs)

ORCA 2C40 (3600 LCs)



# XC4000X Series High Density Leadership

	XC4000EX Family	XC4000XL Family	XC4000XV Family
Logic Cells	2,432 - <b>3,078</b>	466 - <b>7,448</b>	3,078 - <b>10,982</b>
Max Logic Gates	28,000 - <b>36,000</b>	5,000 - <b>85,000</b>	36,000 - <b>125,000</b>
Typ Gate Range (Logic + Select-RAM)	50,000 - 65,000	9,000 - 180,000	72,000 - 250,000
I/O	256 - 288	112 - 448	288 - 544
Number of Devices	2	10	TBD
Power Supply	5 V	3.3 V	3.3 V + 2.5 V
I/O Interface	5 V	5 V / 3.3 V	5 V / 3.3 V

# **XC4000X Solves High-Density Design Issues**

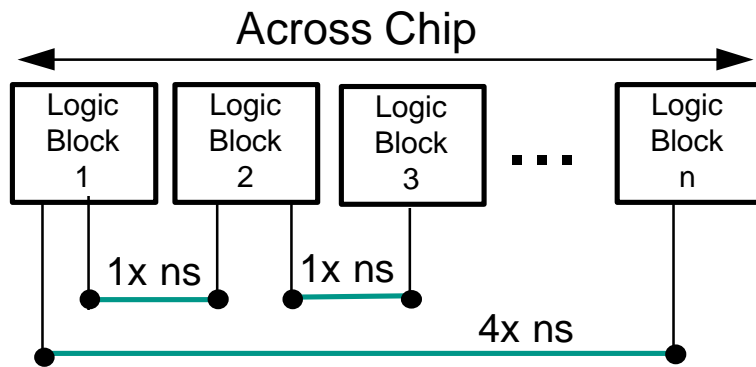
<b><u>Issue</u></b>	<b><u>XC4000X Feature</u></b>	<b><u>User Benefit</u></b>
Routing resources	Twice the resources of XC4000E	High-density designs route easily
Routes get longer	Fast buffered quad lines	Faster performance
Global clock signals get slower	High-speed, multi-level, clocking network Faster I/O blocks	Lower clock skew  Fast chip-to-chip communication

# **XC4000X Solves High-Density Design Issues**

<b><u>Issue</u></b>	<b><u>XC4000X Feature</u></b>	<b><u>User Benefit</u></b>
Design changes	VersaRing I/O interface	Pin assignment flexibility
DSP and arithmetic	Improved carry logic	Higher performance arithmetic functions
Higher system performance	Synchronous single/dual-port SelectRAM	High speed RAMs on-chip (flexible sizes)

# Xilinx Segmented Interconnect Gives Fastest Performance at Lowest Power

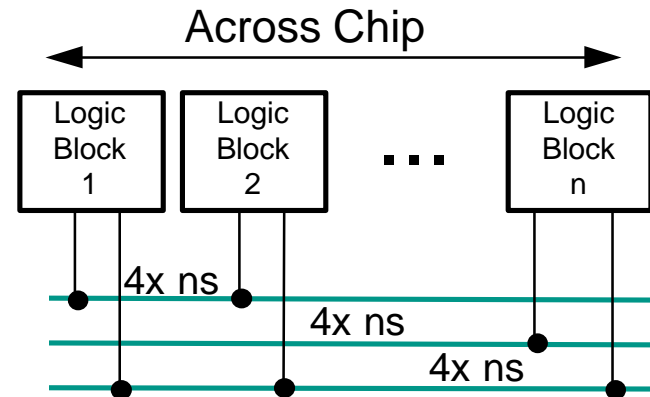
## Xilinx Segmented Interconnect



Optimum-length interconnects

- Lower capacitance
- Higher performance
- Lower power

## Non-Segmented Interconnect

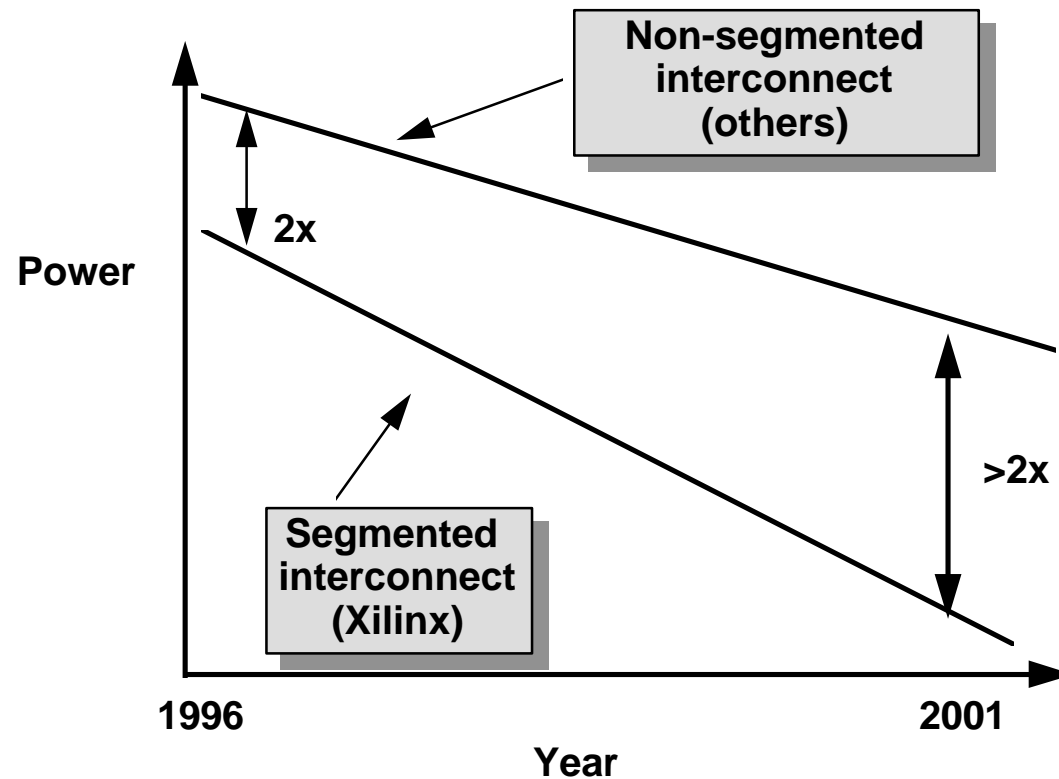


Always worst-case interconnect length

# Xilinx FPGAs Inherently Consume Less Power

## ■ Lower power in XC4000X

- Higher performance
- Higher utilization
- Package flexibility
- Higher reliability



# XC4000XL 3.3 V, 0.35 $\mu$ FPGA Series

**Available  
Now**

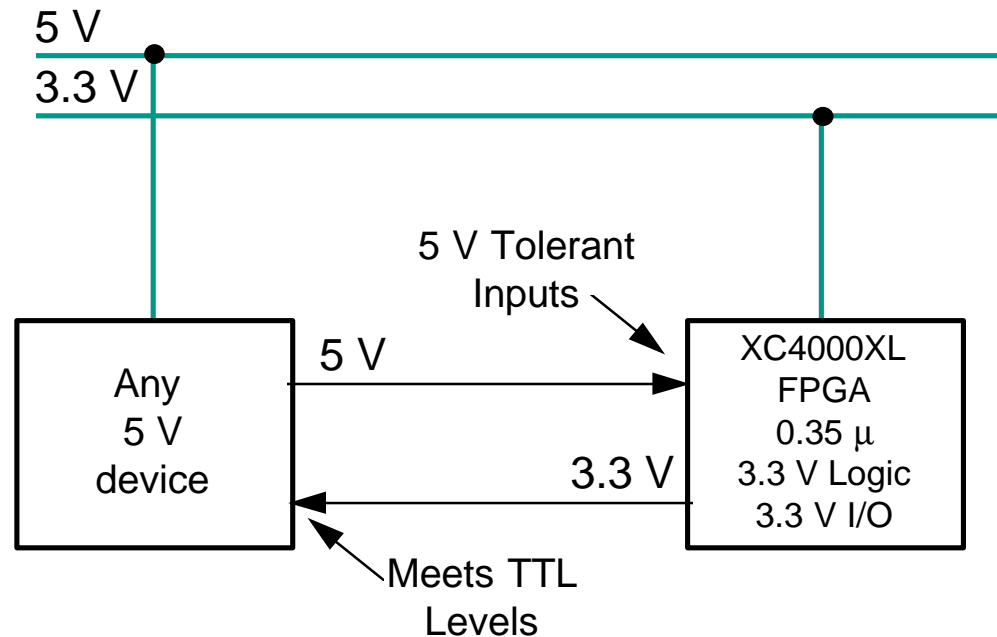
	4005XL	4010XL	4013XL	4020XL	4028XL
Logic Cells	466	950	1,368	1,862	2,432
Max Logic Gates	5,000	10,000	13,000	20,000	28,000
Gate Range* (Logic + Select-RAM)	3 - 9K	7-20K	10-30K	13-40K	18-50K
Max. RAM bits (no Logic)	6K	13K	18K	25K	33K
Max I/O	112	160	192	224	256

	4036XL	4044XL	4052XL	4062XL	4085XL
Logic Cells	3,078	3,800	4,598	5,472	7,448
Max Logic Gates	36,000	44,000	52,000	62,000	85,000
Typ Gate Range* (Logic + Select-RAM)	22-65K	27-80K	33-100K	40-130K	55-180K
Max. RAM bits (no Logic)	42K	51K	62K	74K	100K
Max I/O	288	320	352	384	448

\* 20-30% of CLBs as RAM

# XC4000XL 3.3 V, 0.35 $\mu$ FPGA

## 5 Volt Compatible



- Accepts 5 V inputs
- Drives standard TTL levels
- Totally compatible in 5 V environment

# XC4000XL Series Footprint Compatibility

4005XL	4010XL	4013XL	4020XL	4028XL	4036XL	4044XL	4052XL	4062XL	4085XL
--------	--------	--------	--------	--------	--------	--------	--------	--------	--------

PC84	PC84								
------	------	--	--	--	--	--	--	--	--

PQ100	PQ100								
-------	-------	--	--	--	--	--	--	--	--

VQ100									
-------	--	--	--	--	--	--	--	--	--

TQ144	TQ144	HT144	HT144	→					
-------	-------	-------	-------	---	--	--	--	--	--

PQ160	PQ160	PQ160	PQ160	HQ160	HQ160	HQ160			
-------	-------	-------	-------	-------	-------	-------	--	--	--

	TQ176	HT176	HT176	→					
--	-------	-------	-------	---	--	--	--	--	--

PQ208	PQ208	PQ208	PQ208	HQ208	HQ208	HQ208			
-------	-------	-------	-------	-------	-------	-------	--	--	--

		PQ240	PQ240	HQ240	HQ240	HQ240	HQ240	HQ240	
--	--	-------	-------	-------	-------	-------	-------	-------	--

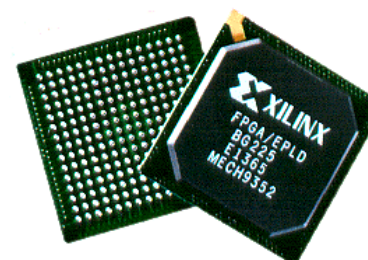
	BG256	BG256	BG256	BG256	→				
--	-------	-------	-------	-------	---	--	--	--	--

		←	BG352	BG352	BG352	→			
--	--	---	-------	-------	-------	---	--	--	--

			←	BG432	BG432	BG432	BG432		
--	--	--	---	-------	-------	-------	-------	--	--

←	Future extensions	→							
---	-------------------	---	--	--	--	--	--	--	--

					BG560	BG560	BG560		
--	--	--	--	--	-------	-------	-------	--	--



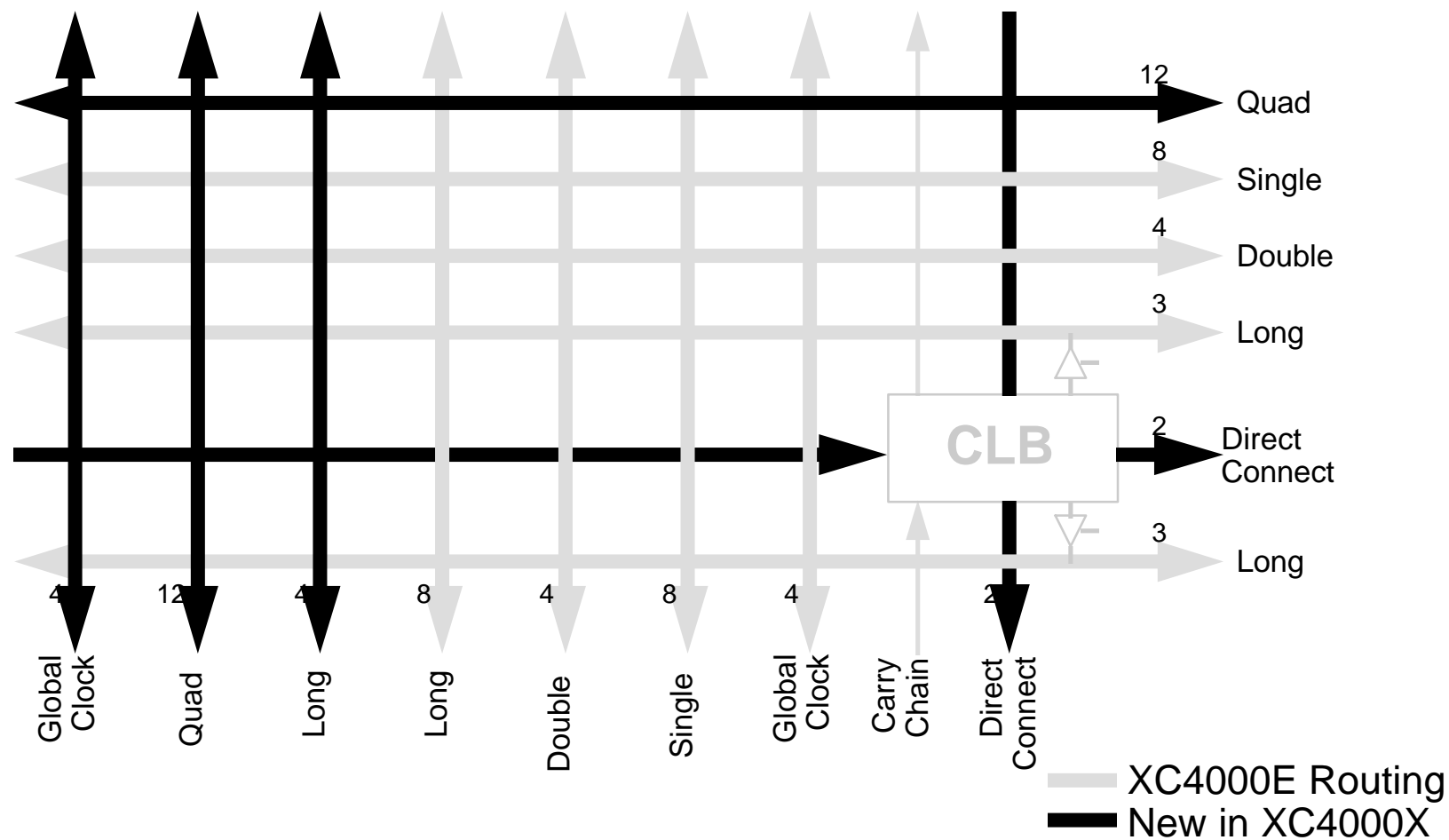


## **XC4000XL Delivers High Performance at 3.3 V**

- 80 MHz internal speed (3-4 LUT levels)
- 66 MHz internal speed (4-5 LUT levels)
- I/O performance

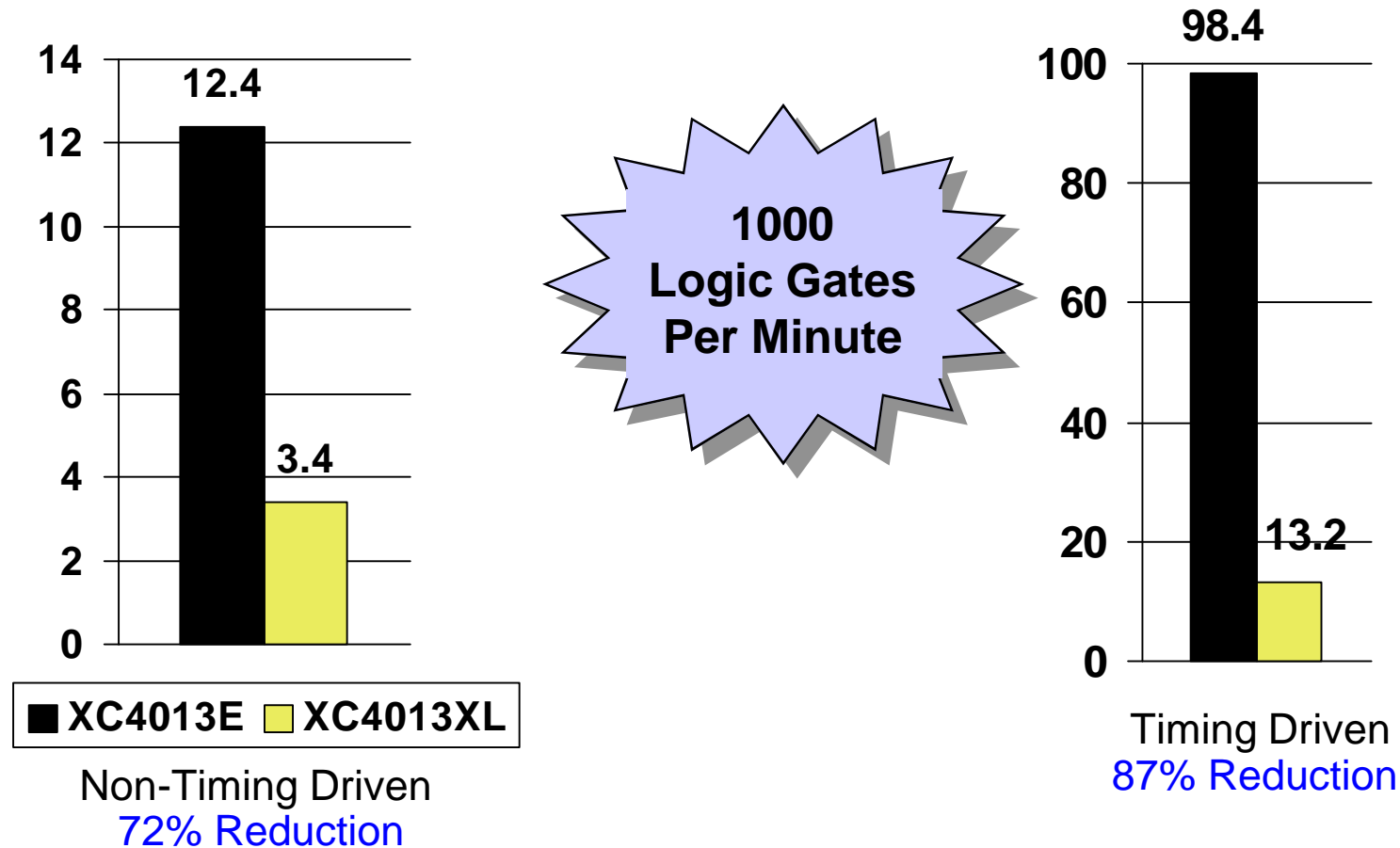
	XC4013XL	XC4036XL
– Tco (output register)	6.4 ns	6.4 ns
– Tsu (input register)	4.5 ns	5.4 ns
– Th (input register)	0 ns	0 ns
– Max I/O frequency	92 MHz	85 MHz

# XC4000X Series Doubles Routing of XC4000E



# XC4000X Architecture Reduces Runtimes

## XC4013XL Place and Route Times in Minutes



Average data from 30+ designs (80% avg utilization) run on 200 MHz Pentium Pro

# The XC4000XV - Industry's First 0.25 $\mu$ FPGA

- Extends XC4000X architecture to 0.25  $\mu$ , 5-layer metal CMOS technology
- XC40125XV: 10,982 logic cells (125,000 logic gates)
- Performance summary

	XC4036XV
– Internal operation (3-4 LUT levels)	100 MHz
– Tco (output register)	6 ns
– Tsu (input register)	4 ns
– Th (input register)	0 ns
– Max I/O frequency	100 MHz

## **XC4000X Series High-Density FPGAs**

- Complete 3.3 V family with 5 V tolerant I/O
- Up to 100 MHz system performance
- 100% PCI compliant
- Lowest power per gate in the industry
- SelectRAM (single / dual-port)
- Software support for popular EDA tool flows
- Fast place-and-route times
- Complete library of system-level COREs
- HardWire migration path for cost reduction
- 10,982 logic cells (125,000 logic gates) in 1997

# XC4000E Family: 5 V Performance Leadership

**Fast SelectRAM**

**System performance to 66 MHz**

**100% PCI compliance**

**Low-cost migration to HardWire**

**Complete VHDL/Verilog support**

**Industry's fastest 5 V FPGA**

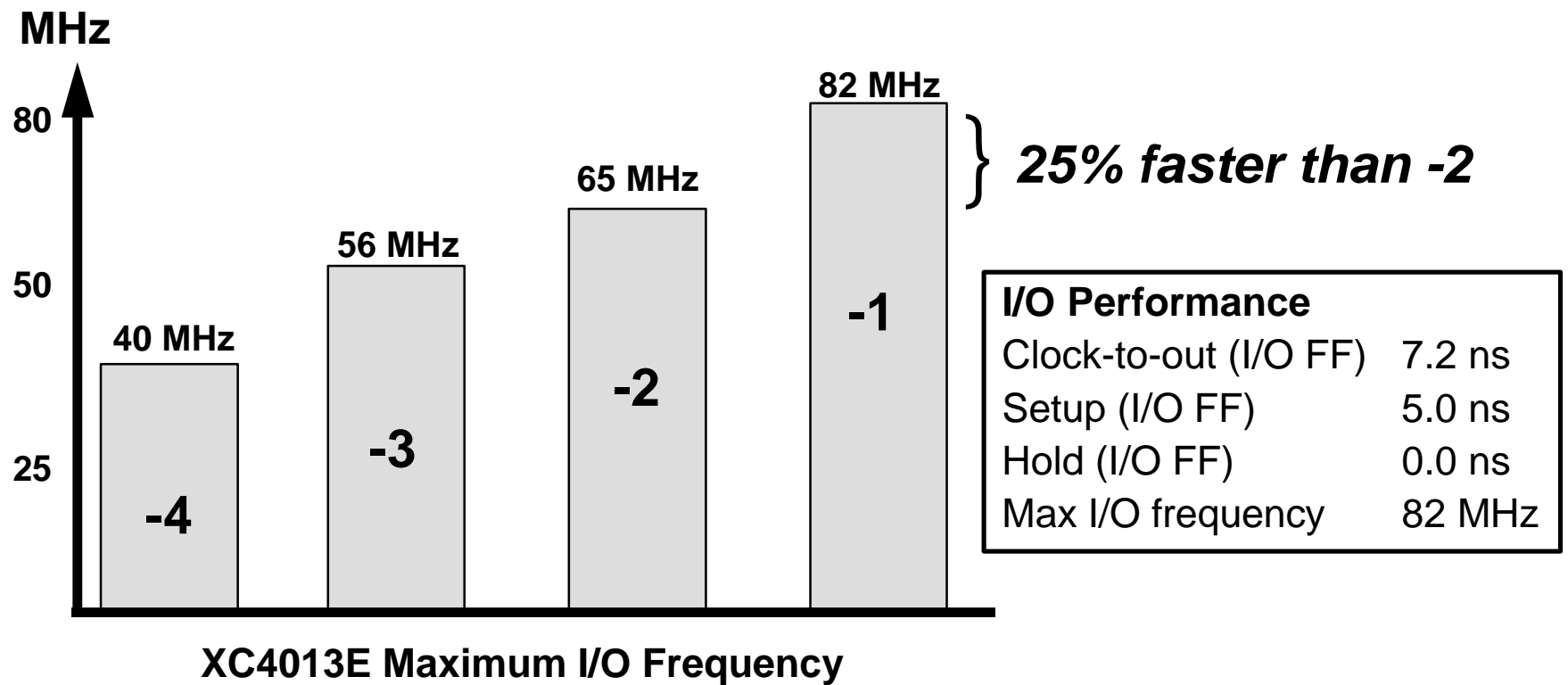
**100% footprint compatibility**

**LogiCore system-level libraries**

## XC4000E Family

Logic Cells	217 - 2,432
Max Logic Gates	3,000 - 25,000
Typ Gate Range (Logic + Select-RAM)	5,000 - 48,000
Max I/O	64 - 256
Number of Devices	8

# ***XC4000E-1: Industry's Fastest 5 V FPGA***



Max. I/O frequency =  $1/(\text{clock-to-out} + \text{I/O set-up})$

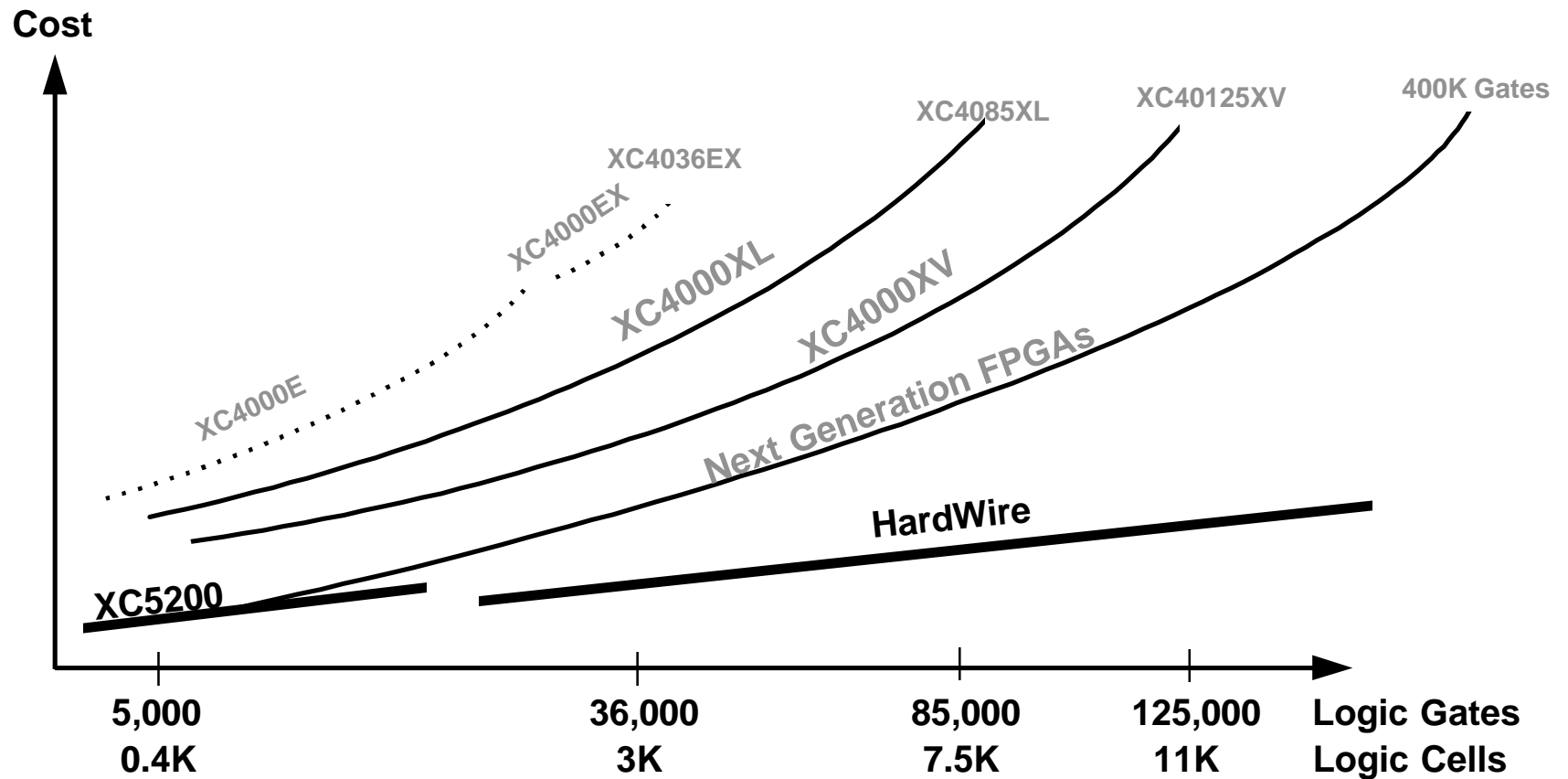
# XC4000E Fastest 5 V FPGA Family

	4003E	4005E	4006E	4008E	4010E	4013E	4020E	4025E
<b>Logic Cells</b>	238	466	608	770	950	1,368	1,862	2,432
<b>Max Logic Gates</b>	3K	5K	6K	8K	10K	13K	20K	25K
<b>Typ Gate Range*</b> (Logic + Select-RAM)	2-5K	3-9K	4-12K	6-15K	7-20K	10-30K	13-40K	15-45K
<b>Max I/O</b>	80	112	128	144	160	192	224	256
<b>Packages:</b>	PC84 TQ100 PQ100	PC84 PQ100 TQ144	PC84 TQ144 PQ160	PC84 PQ160	PC84 PQ160	PQ160	PQ160	PQ160
<b>100% Footprint Compatible</b>		PQ208	PQ208	PQ208	PQ208	PQ208	HQ208 HQ240	HQ240 HQ304
	PG120	PG156	PG156	PG191	PG191	PG223	PG223	PG223
					BG225	BG225		PG299

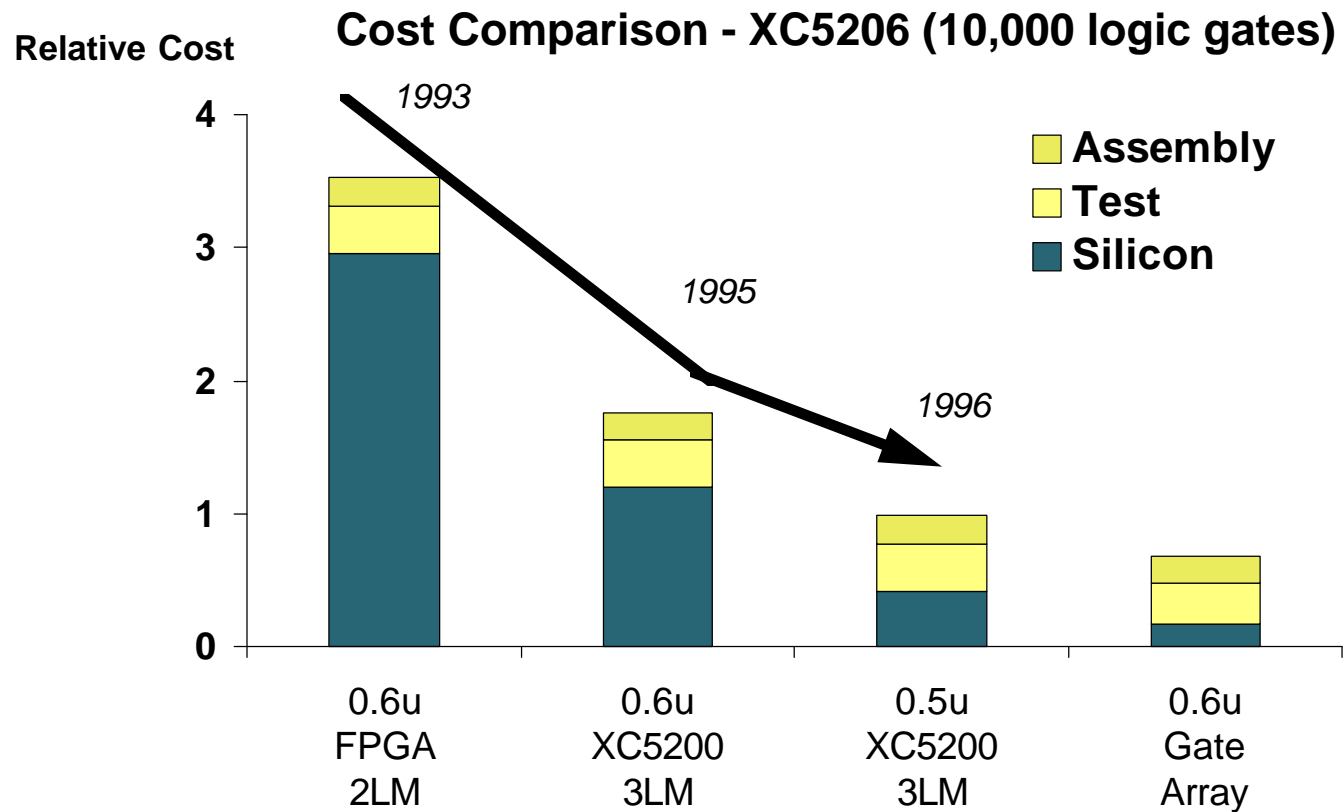
\* 20-25% of CLBs as RAM



# Continuous Cost Reduction

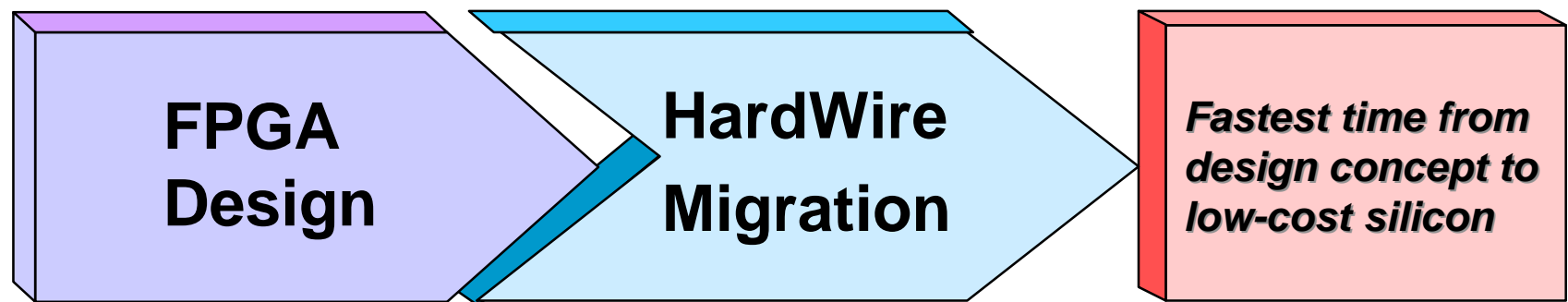


# XC5200 Less than Twice Gate Array Cost



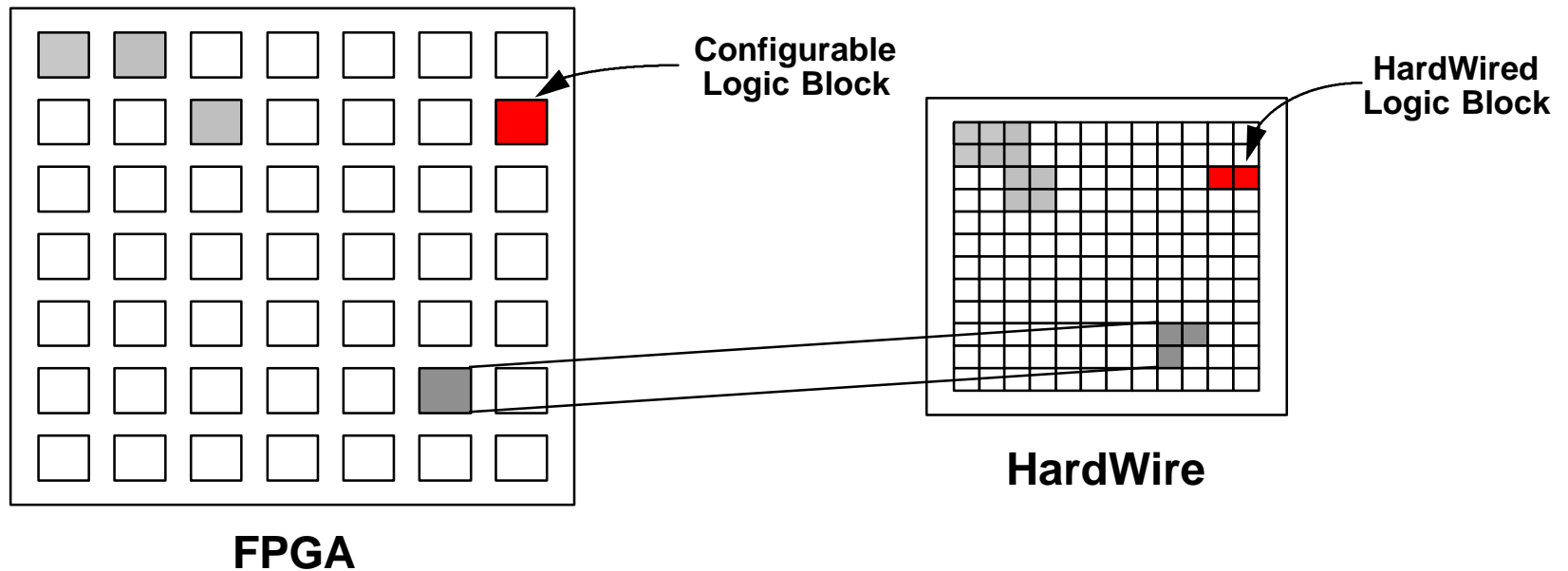
***No need for gate arrays below 20,000 gates!***

# Design Once: The HardWire Advantage



- Fast development
- Time-to-market
- Concurrent engineering
- Flexibility
- No customer re-design
- No customer vectors
- All FPGA features
- Mask programmed pricing

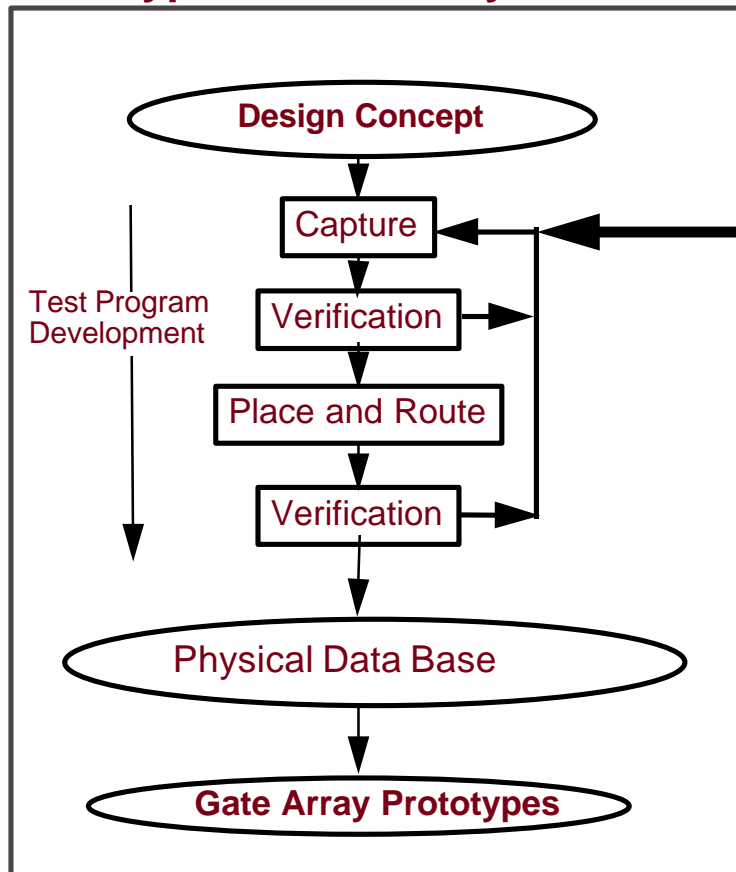
# All FPGA Features and Structures Preserved During HardWire Conversion



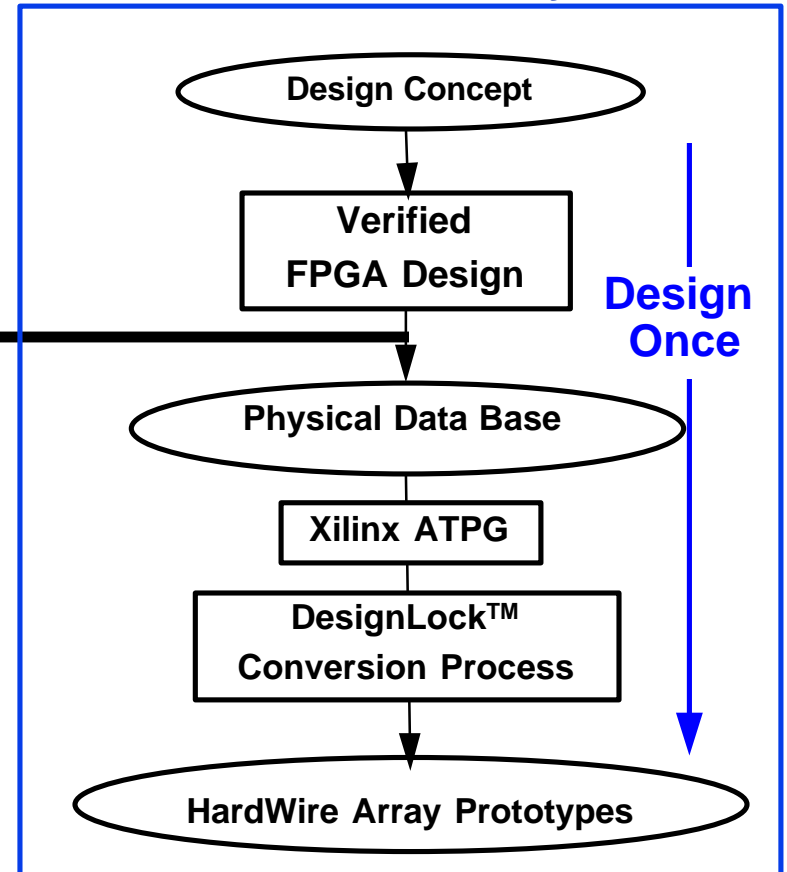
- CLB structure and nets are preserved - No netlist transformation
- CLBs and nets are maintained in the same relative location on the die
- ALL FPGA features (e.g., configuration emulation, POR, JTAG, etc.)

# Design Once for FPGA to HardWire

## Typical Gate Array Flow



## Xilinx HardWire Array Flow



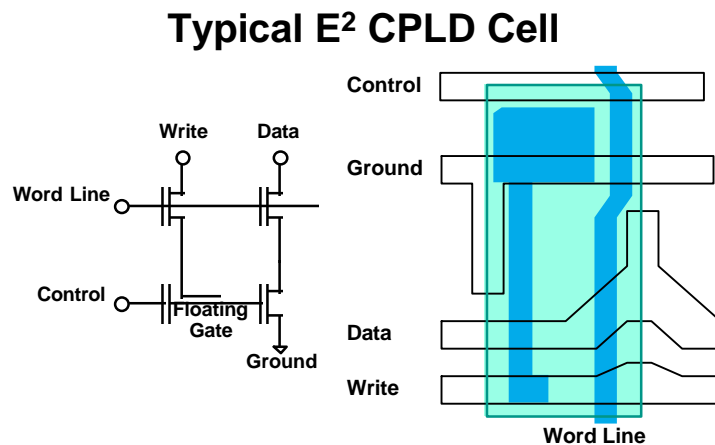
Gate Array  
Re-targeting  
Alternative

# **XC9500: The Industry's First 5 V Flash CPLD**

- Lowest price per macrocell of any CPLD
- 5 V in-system programmable (ISP) CPLDs
  - Total product life cycle support
- High performance: 5 ns pin-to-pin
- Up to 288 macrocells
- Industry's best pin-locking architecture
- Most extensive IEEE 1149.1 JTAG for ISP and test
- Highest endurance
  - 10,000 program / erase cycles

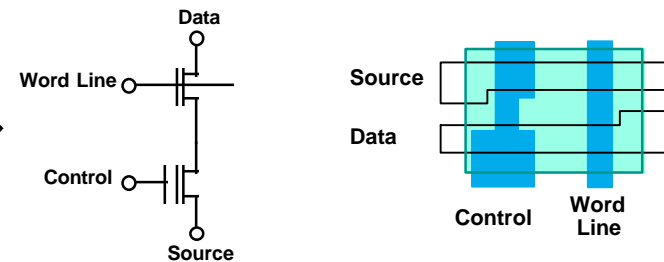


# XC9500: Superior FastFLASH Technology



**1/3  
Area**

## XC9500 FastFLASH Cell



- Far more routing switches than competitors
  - Superior routing
  - Superior pin-locking capability
- Lowest price per macrocell

## **XC9500 ISP CPLDs Bring Total Product Life Cycle Support to CPLDs**

- Easily change your design during development
  - No wasted devices
  - No programmer necessary
- No sockets
- No need to handle a device to program it
  - Program devices as part of normal manufacturing flow
- Virtually unlimited design modification in the field

***Brings advantages of reprogrammable FPGAs to CPLDs***



# **Leadership XC9500**

## **Volume Price Projections**

<b>Part Number</b>	<b>Projected 1Q98 Volume Pricing</b>
<b>XC9536</b>	<b>\$1.40</b>
<b>XC9572</b>	<b>\$2.20</b>
<b>XC95108</b>	<b>\$5.85</b>
<b>XC95216</b>	<b>\$18.45</b>
<b>XC95288</b>	<b>\$29.30</b>

# XC9500 Product Family Overview

	9536	9572	95108	95144	95216	95288
<b>Macrocells</b>	<b>36</b>	<b>72</b>	<b>108</b>	<b>144</b>	<b>216</b>	<b>288</b>
<b>Usable Gates</b>	<b>800</b>	<b>1600</b>	<b>2400</b>	<b>3200</b>	<b>4800</b>	<b>6400</b>
<b>t<sub>PD</sub> (ns)</b>	<b>5</b>	<b>7.5</b>	<b>7.5</b>	<b>7.5</b>	<b>10</b>	<b>10</b>
<b>Registers</b>	<b>36</b>	<b>72</b>	<b>108</b>	<b>144</b>	<b>216</b>	<b>288</b>
<b>Max I/O</b>	<b>34</b>	<b>72</b>	<b>108</b>	<b>133</b>	<b>166</b>	<b>192</b>
<b>Packages</b>	VQ44 PC44	PC44 PC84 TQ100 PQ100	PC84 TQ100 PQ100 PQ100 PQ160 PQ160		PQ160 HQ208 BG352	HQ208 BG352

# Xilinx Product Solution Summary

- New M1 software solutions
  - Alliance Series - EDA vendor integration
  - Foundation Series - complete, ready-to-use solution
- Xilinx CORE solutions
- XC4000X Series - industry's largest and fastest FPGAs
  - XC4000XL 0.35  $\mu$ , 3.3 V FPGAs (5K-85K gates)
- XC4000E - industry's fastest 5 V FPGA
- Low-cost solutions
  - XC5200 / HardWire
- XC9500 - FastFLASH ISP CPLD family
  - Lowest cost CPLD solution