

Case Studies

- DRAM Controller: XC9500 ISP CPLD
- Universal Serial Bus: XC4000E/X FPGA
- **Peripheral Component Interconnect: XC4000E/X FPGA**
- Digital Signal Processing: XC4000XL FPGA

Case Study #3 - PCI XC4000E/X

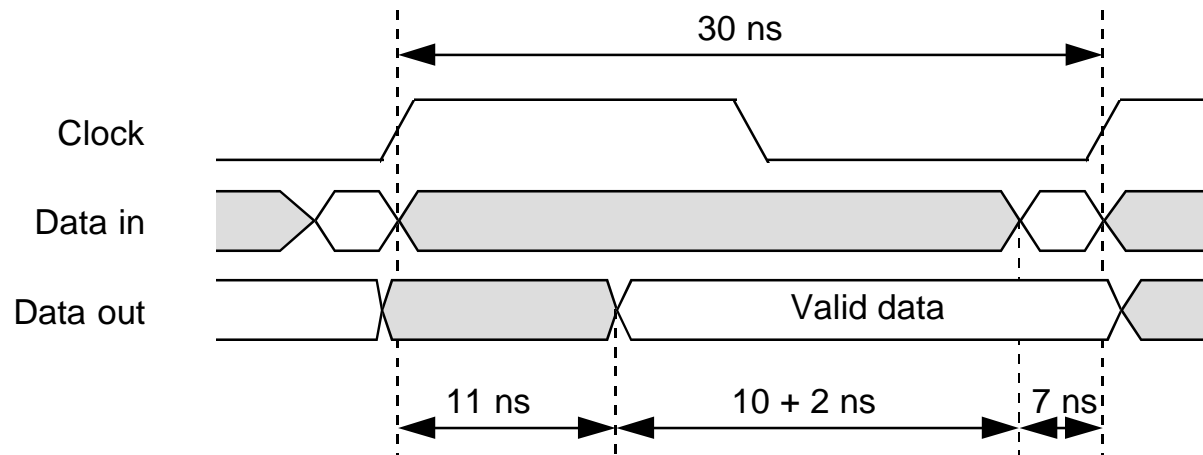
- High-performance PCI interface is available as firm CORE
- Demonstrates design efficiency and XC4000E/X capabilities

What is the Right Bus Interface?

- Many FPGA designs are looking for a standardized fast bus interface
- PCI is a perfect match
 - Popular, widely supported
 - Well-documented
 - High-performance up to 132 MB per second
 - 33 MHz clock (66 MHz in the future)
 - 32 bits wide (64 bits in the future)
 - Low cost
 - Unterminated (uses reflected wave)

PCI Design Challenges: Speed

- 33 MHz data on unterminated backplane requires:
 - Max 11 ns clock-to-output delay
 - Max 7 ns input set-up time
 - Max 2 ns allowed for clock skew
 - Max 10 ns allowed for signal wave reflection
- Transaction controls cannot be pipelined,
 - Must be decoded during the set-up time



PCI Design Challenges: Functionality

- Independent 3-state controls for outputs
 - 4 for target
 - 7 for target / initiator
- Internal bidirectional datapath:
 - 32 bits wide (64 bits in the future)
- Up to 64 bytes of configuration registers
- On-chip asynchronous FIFOs
 - Decouple user logic from the bus
 - Usually one FIFO per direction
 - Typical depth: 16 or 32 words
 - Simultaneous read and write requires dual-port RAM

PCI Challenge: User Configuration Options

Basic configuration

- Master (Initiator & Target)
- Slave (Target-only)
- Burst
- No-burst
- Enable interrupts
- Ignore interrupts
- FIFO number and size

Configuration Register

- Base Address Register 0
- Base Address Register 1
- Base Address Register 2
- Expansion ROM Base Addr.
- Device ID
- Vendor ID
- Subsystem ID
- Subsystem Vendor ID
- Class Code
- Revision ID

Don't Re-Invent the Wheel

- This demanding interface design has been completed
- Don't waste your time and energy duplicating an existing design that is available
- Xilinx offers a proven, tested and verified solution:

LogiCORE™ PCI

Xilinx Provides A Complete Solution for PCI

■ XC4000E/X FPGA

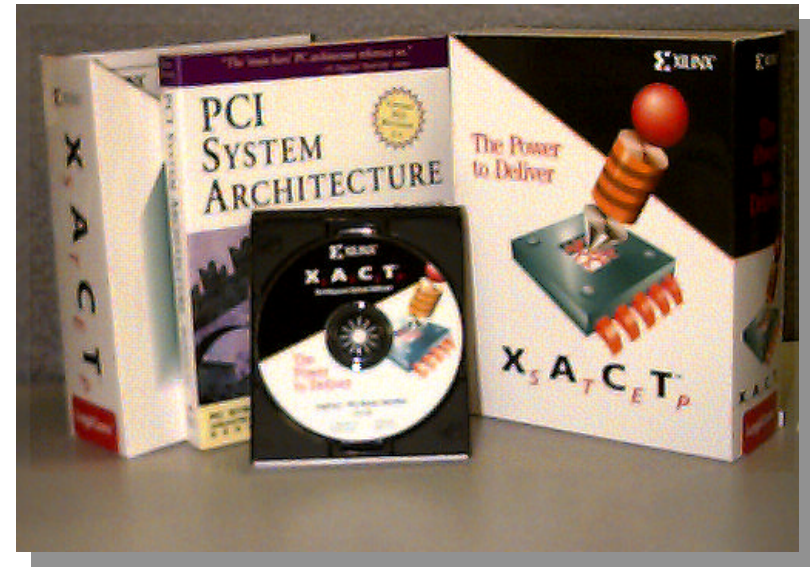
- Integrates PCI plus room for 5-30K user gates
- HardWire at \$19.50*

■ LogiCORE PCI

- “Firm” CORE, proven and fully verified
- 200+ users (April '97)

■ Web-based CORE tool for PCI

- Easy CORE configuration and integration
- Gives instant access to new enhancements



* PCI, two 32x16 dual-port FIFOs and 10K user gates in 25K units, PQ208 package

XC4000E/X - Best FPGAs for PCI

■ Big enough

- PCI interface + on-chip FIFO leaves user space of:
- 50% of XC4013E 65% of XC4020E
75% of XC4028EX/XL 82% of XC4036EX/XL
- i.e. 5K-30K logic gates for user logic

■ Fast enough

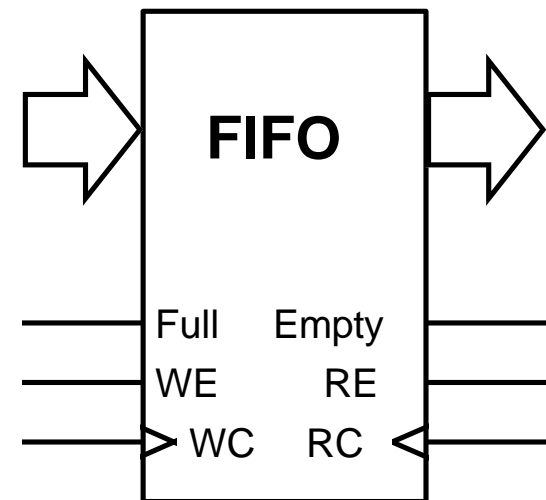
- Meets clock-to-output, set-up and hold time requirements
- Supports burst transfers

■ Powerful architectural features

- Multiple 3-state output controls to support PCI protocol
- On-chip bussing to support PCI datapath
- SelectRAM for multiple FIFOs

Build FIFOs Using XC4000E/X SelectRAM

- FIFO scalable to fit user requirements
 - Uses dual-port SelectRAM
 - 16-deep, 32-bit wide FIFO uses 88 logic cells
- Up to 66 MHz operation
- Simultaneous read and write
- Independent read and write clocks



Ready-to-Use **LogiCORE™** PCI

- 32 bit, 33 MHz PCI CORE
 - Fully compliant with PCI Spec version 2.1
 - Target-only (Slave) and Initiator/Target (Master)
 - Well-defined back-end interface to custom logic
- Pre-defined to cut development time
 - Constraints embedded to assure critical timing
 - Highly optimized for XC4000E and XC4000EX (XC4000XL in 3Q97)
- Fully verified to minimize design risk
 - Verified with VirtualChip VHDL PCI simulation model
 - Hardware-proven in many customer designs

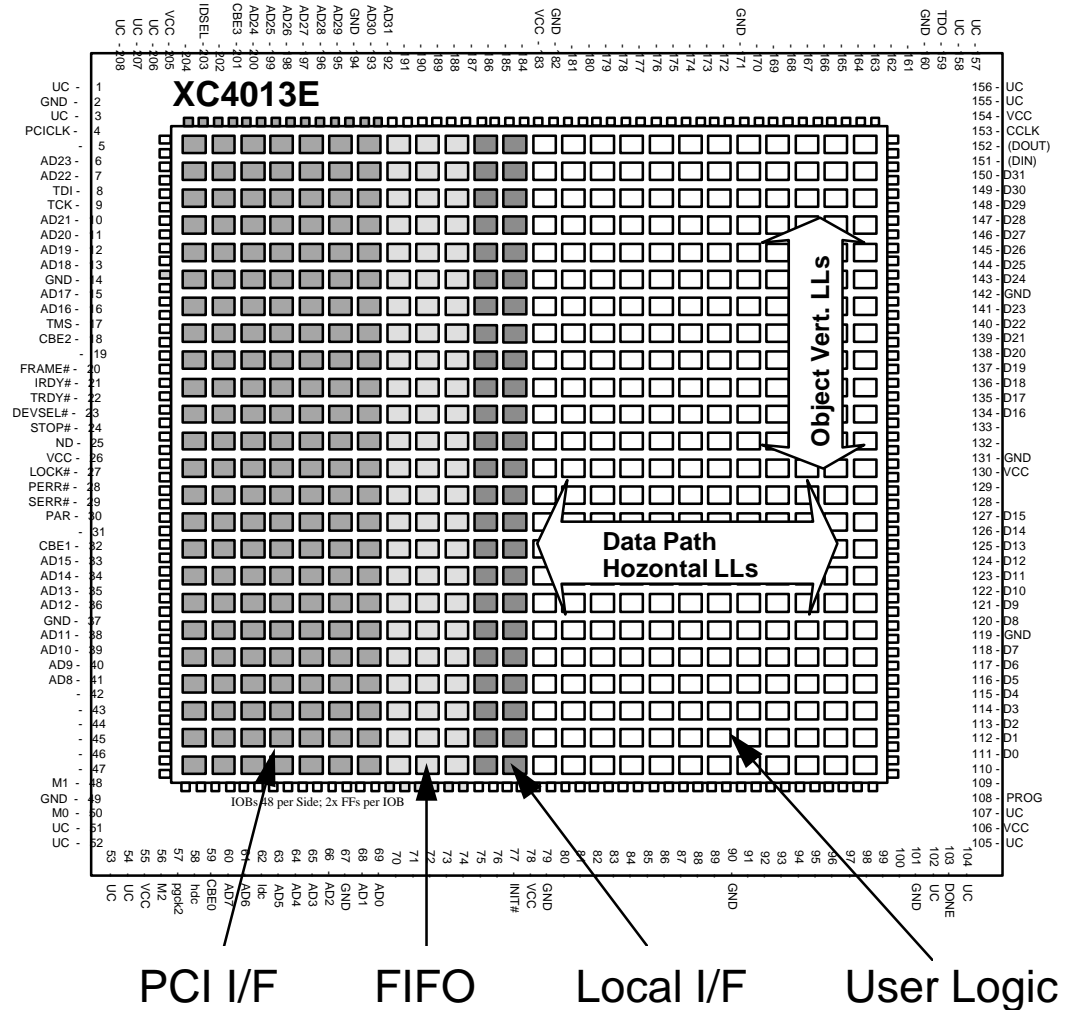
Pre-Defined Implementation in XC4013E

Completed in CORE:

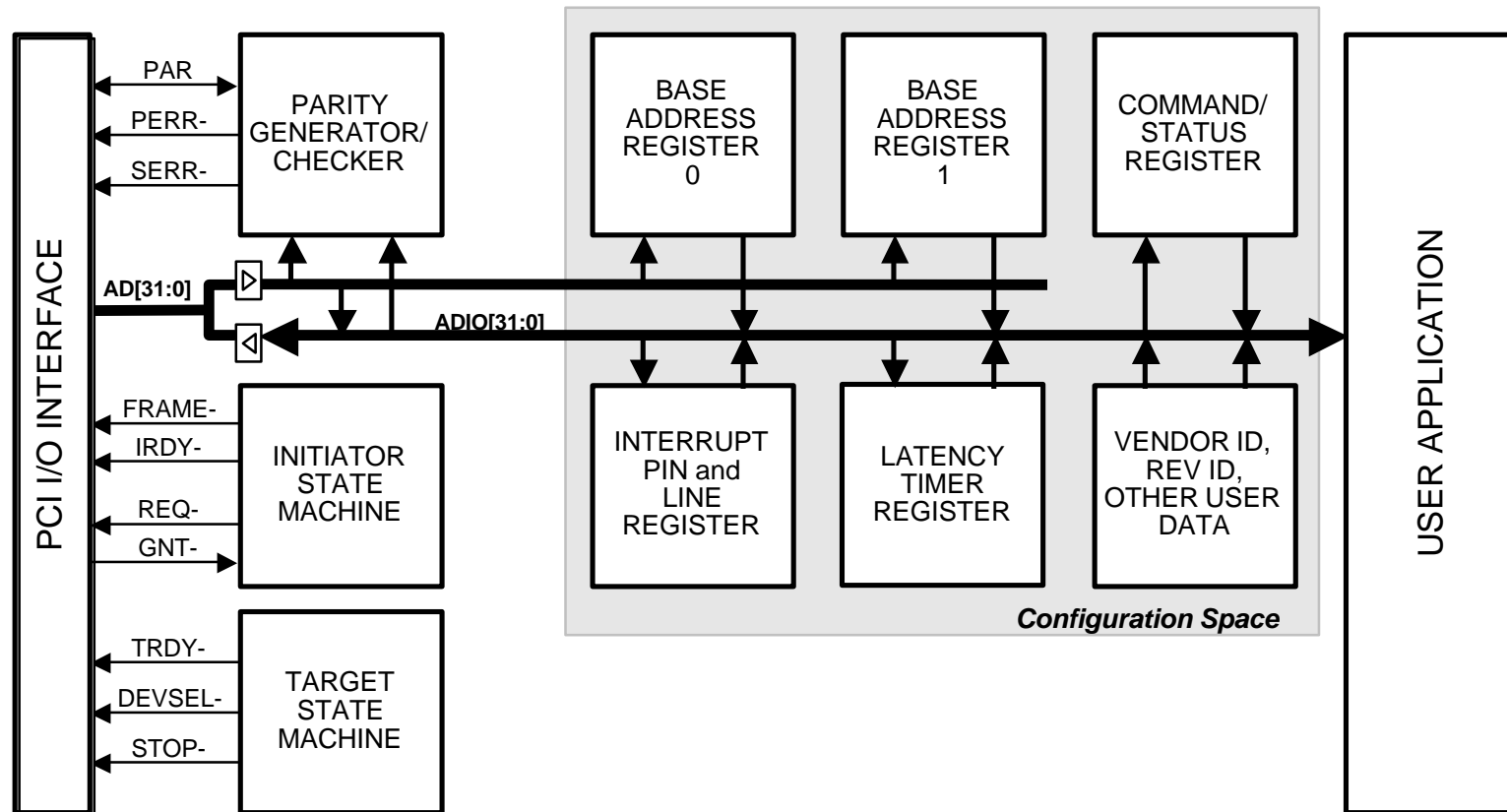
- Relative placed macros (RPMs) assisted placement
- Guide files defined routing
- Timespecs constrained all critical paths

Result:

- Predictable functionality and timing



LogiCORE™ PCI - Block Diagram



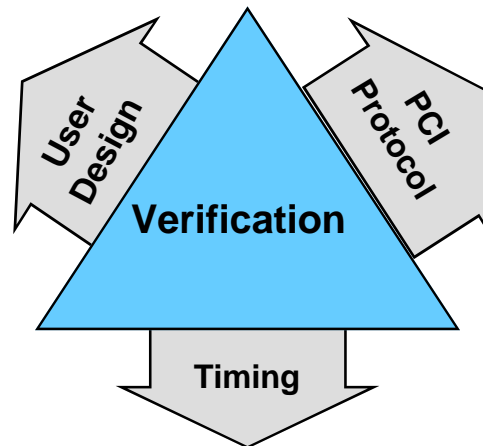
LogiCORE™ PCI - Verification

Xilinx PCI Testbench

- 6,913 lines of code
- Included in LogiCORE PCI products
- Matches PCI-SIG checklist
- Additional test patterns to test target terminations

VirtualChips™ PCI Testbench

- 19,357 lines of VHDL test code
- Extensive Test Coverage for Target & Initiator
- PCI SIG Test Scenarios
- Used with Synopsys VSS



Static Timing Analysis

- 5,224 paths verified

CORE Configuration Tool for PCI

- Industry's first Web-based FPGA tool
- Design methodology for FPGA COREs
 - GUI for entry of CORE parameters
 - Generates optimized design files
- Executable on the web
 - Instant access to design tips and CORE enhancements
 - Java-enabled browser
 - Platform independent

Enabling technology for FPGA COREs

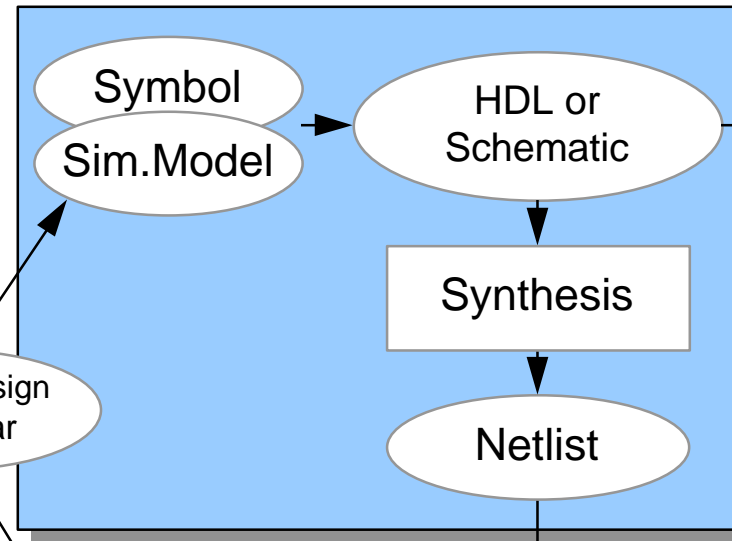
LogiCORE™ PCI Design Flow

CORE Configuration

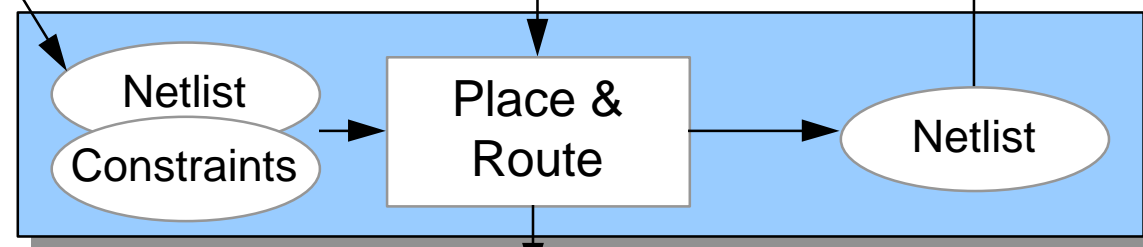
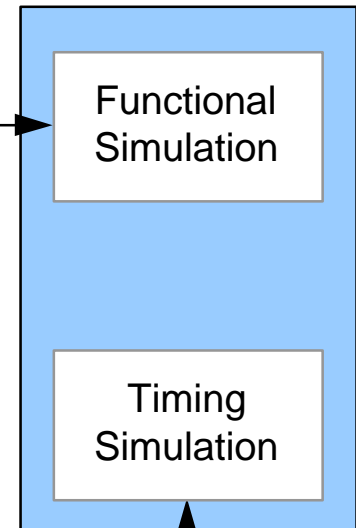


CORE Design
zip or tar

Design Entry



Design Verification



Design Implementation



LogiCORE™ PCI Roadmap

- Make PCI easier to design
- Continuous performance improvements

Release	Key Feature	Family	When
v1.2	PCI CORE generator VHDL and Verilog HDL support	XC4000E	NOW
v2.0	Second generation LogiCORE PCI <ul style="list-style-type: none"> • Higher density - up to 30K user gates • Standardized local bus - easier to integrate user logic 	XC4000EX	3Q97
v2.x	3 V / 5 V Compliance <ul style="list-style-type: none"> • Higher performance (100% burst) 	XC4000XL (3 V only)	3Q97
		XC4000XL/XV (3 V / 5 V)	4Q97
		XC4000XL/XV	4Q97
	64 bit / 33 MHz		
	66 MHz (32 / 64 bit)	Next Generation	1998

Xilinx PCI Solution Summary

- **Cost effective single-chip FPGA and HardWire**
 - XC4000 Series - best FPGAs for high-performance applications such as PCI
- **LogiCORE PCI interfaces minimize development effort**
 - Proven and fully-verified CORE
- **Web-based CORE tool simplifies configuration and integration**
 - Allows easy access to improvements and updates