

Agenda

- The Future of Programmable Logic
- Product Overview
- Design Methodology Case Studies
- The Next Generation
- **Summary / Q&A**

Summary

■ Why programmable logic?

- Shorter time-to-market
- Need for product differentiation
- Reduced risk

■ Today's programmable logic solutions

- Performance: 80 MHz system clock rate
- Density: 7,000 Logic Cells (85,000 logic gates) + RAM
- Cost: low cost FPGAs, HardWire, lowest-cost CPLDs
- Voltage: complete 3.3 V family with full 5 V compatibility
- Design methodology: ASIC design flows, synthesis, COREs

The Pace of Technology is Accelerating

Xilinx is the Leader in Programmable Logic Innovation

■ Process technology - SRAM and FLASH

- 0.35u ➡ 0.25u ➡ 0.18u ➡ 0.13u

■ Circuit design

- Low-skew clock structures, PLLs
- Fast, flexible I/O

■ Architecture

- SelectRAM, block RAM
- Hierarchical interconnect

■ Design methodology

- Behavioral design entry
- Intellectual property (COREs)

Imagine the Possibilities...

*Our innovation helps you
succeed in your business*

Thank you for your time and attention.