

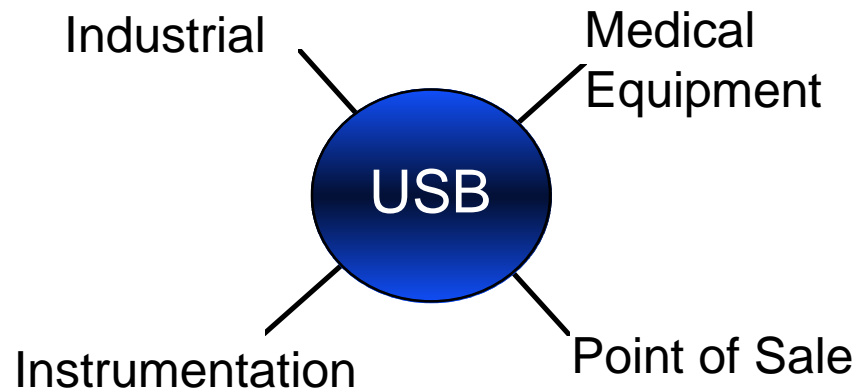
## Case Studies

- DRAM Controller: XC9500 ISP CPLD
- **Universal Serial Bus: XC4000E/X FPGA**
- Peripheral Component Interconnect: XC4000E/X FPGA
- Digital Signal Processing: XC4000XL FPGA

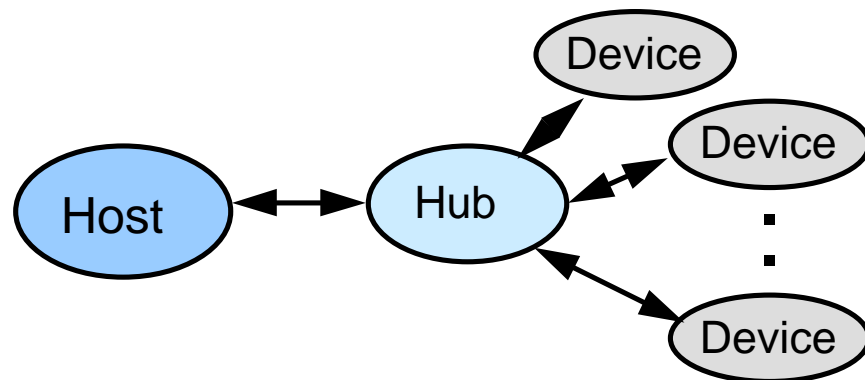
## **Case Study #2 - Universal Serial Bus XC4000E/X**

- USB controller design is technology-independent and device-independent
- Demonstrates constraints controlling device performance from the Verilog HDL level

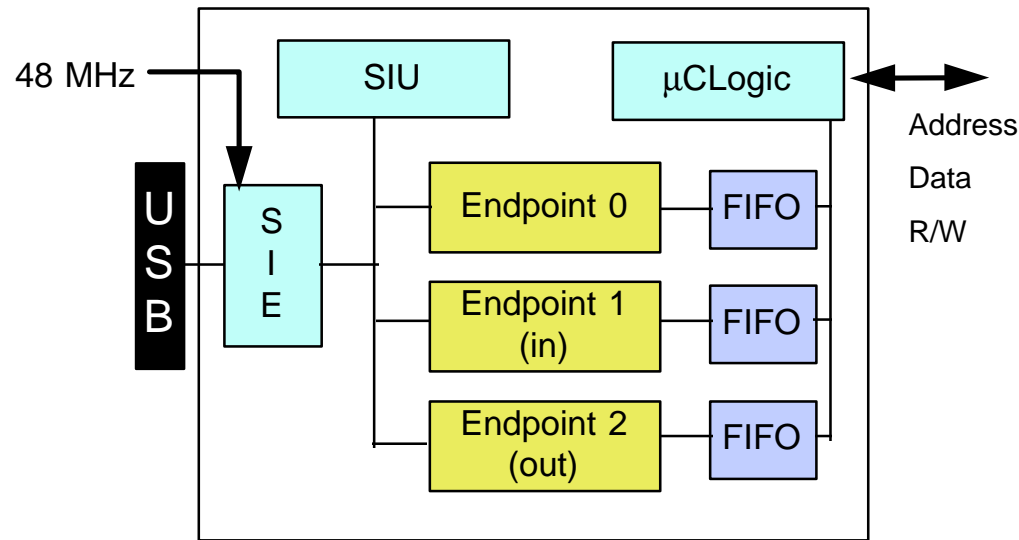
# USB Universal Serial Bus Case Study



- Standardized serial bus
- 2 wires, differential data
- Plug and play functionality
- 1.5 Mbps (low speed)  
12 Mbps (full speed)
- Up to 127 devices



# USB Function Controller



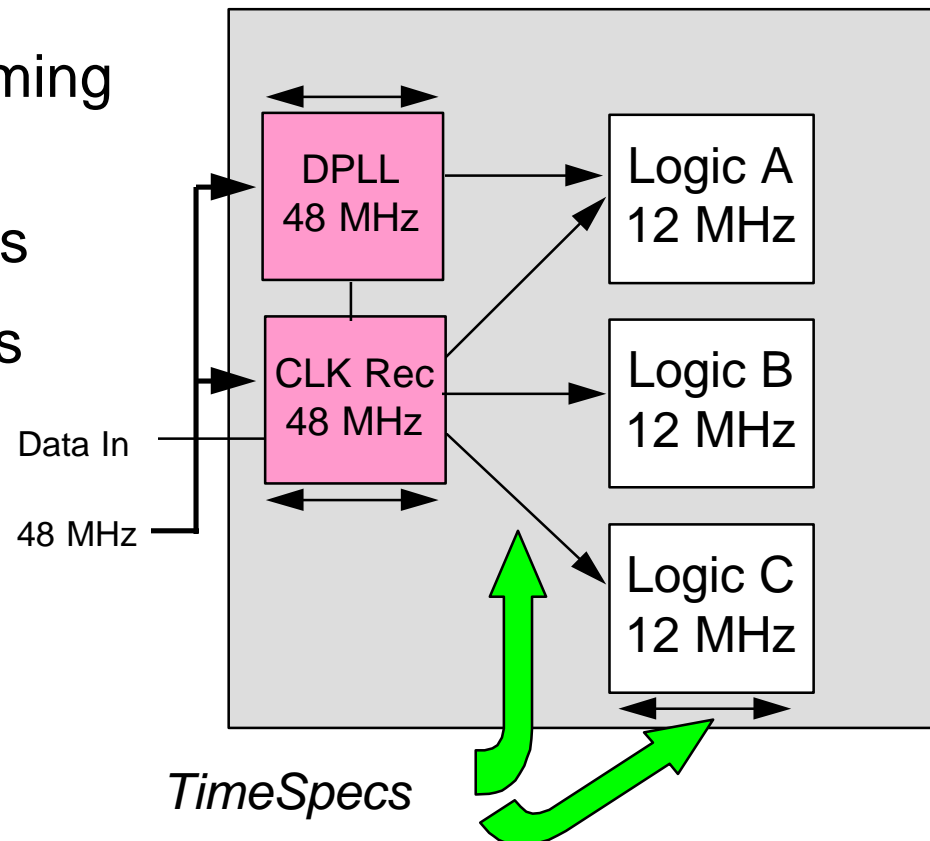
- Serial Interface Engine
  - State machine intensive
- 12 Mbps => 12 MHz operation
  - Clock recovery => 48 MHz operation (small section)
- Endpoint = register ports

## **Goal: Constraint-Directed, Technology-Independent Design**

- Technology-independent design methodology
  - Verilog HDL with constraints applied during synthesis
  - Retarget with logic synthesis
- Use synthesis tool to pick state machine options
  - One-hot, Grey, binary
- Design implementation directed by constraints
  - No hand placement
- Re-use bus interface with different back-end logic

# USB System Timing Analysis

- Look at the design from a timing point of view
- Identify blocks of logic as “timing groups”
- Design with pipeline registers
- Establish timing relationships within and between blocks
  - Use group timing constraints



# Applying Global Constraints

Global constraints apply to the entire design

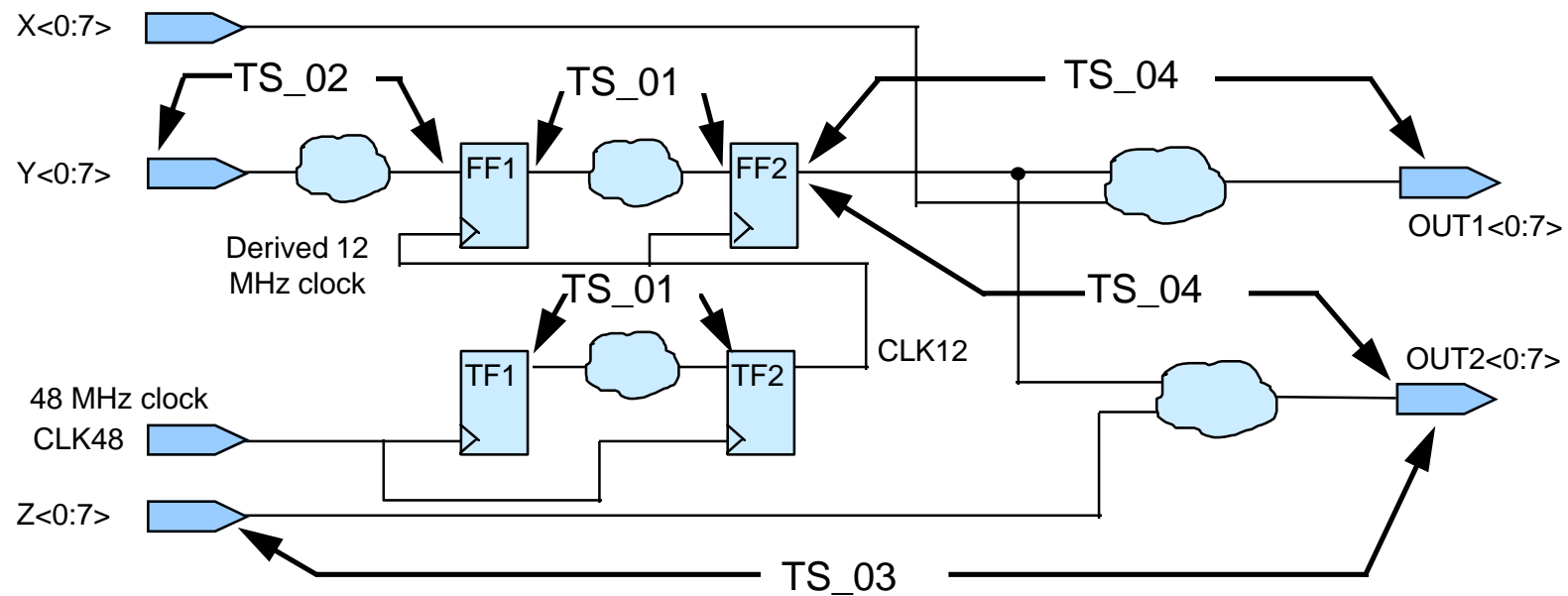
TIMESPEC command using predefined groups:

```
TIMESPEC TS_01 = FROM : FFS : TO : FFS : 80;
```

```
TIMESPEC TS_02 = FROM : PADS : TO : FFS : 25;
```

```
TIMESPEC TS_03 = FROM : PADS : TO : PADS : 30;
```

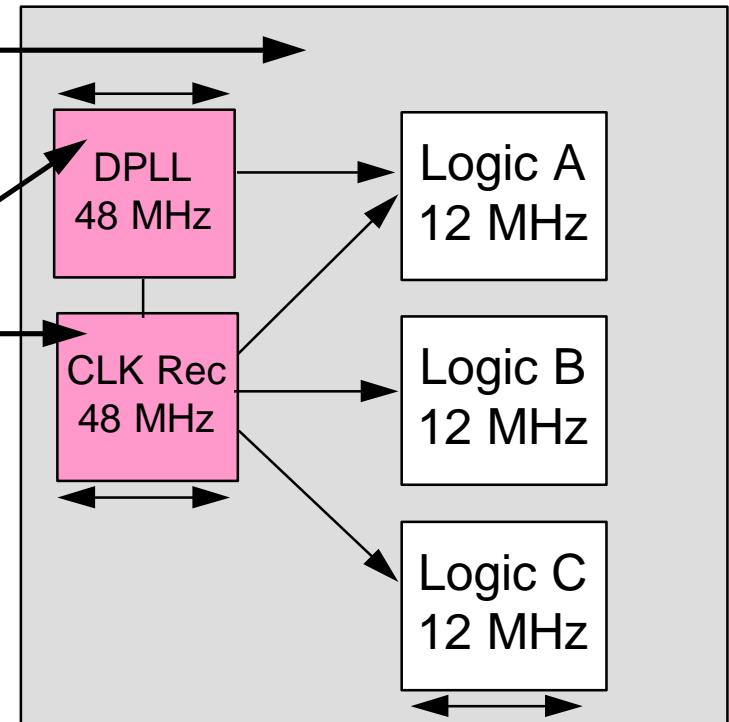
```
TIMESPEC TS_04 = FROM : FFS : TO : PADS : 15;
```



# Applying Global and Group Constraints

Global 12 MHz constraints  
applied to entire design

Group constraints (48 MHz)  
applied to timing-critical blocks





## Overriding Global Constraints

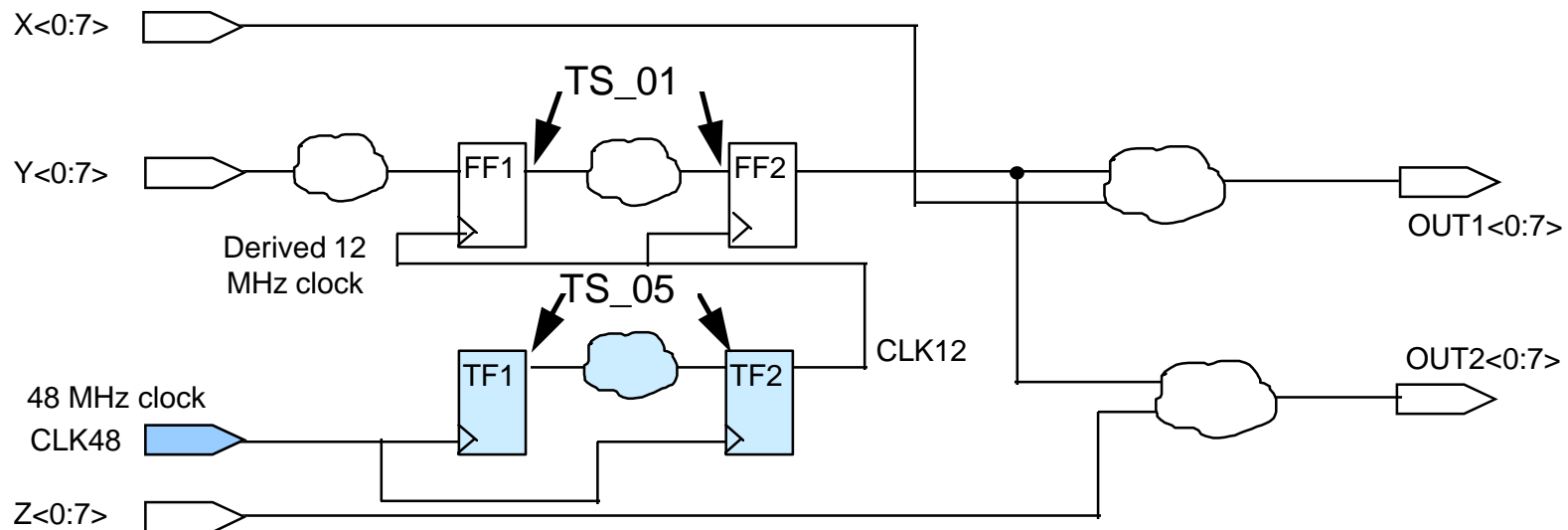
- Consider TS\_01 from the global example:

```
TIMESPEC TS_01 = FROM : FFS : TO : FFS : 80;
```

- TS\_01 is applied to both groups of flip flops (FF\* and TF\*)

- Constrain TF1 to TF2 path separately to be realistic

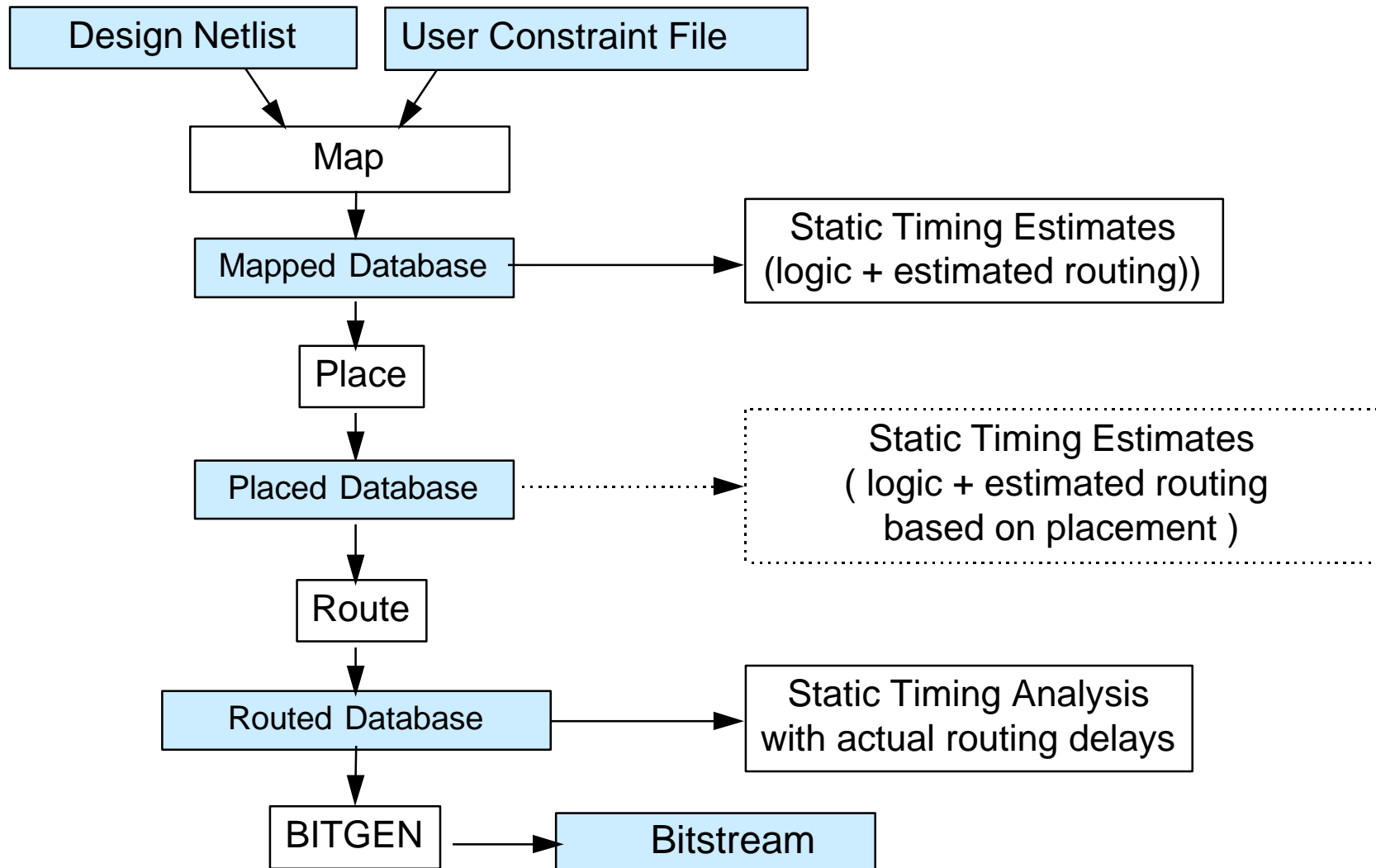
**TIMESPEC TS\_05 = FROM : FFS(TF\*) : TO : FFS(TF\*) : 20;**



# Group Constraints Achieve Desired Performance

- Most group constraints use a similar syntax as global constraints
  - Endpoints may now be user-defined groups
- User-defined groups may be:
  - Components, pins, nets, primitives, or macros
  - Groups of components, pins, etc.
  - Subsets of pre-defined groups
  - Subsets of sub-groups
- Use group constraints to be selective
  - Don't over-constrain designs

# Timing Analysis In M1 Design Flow



# Assess Timing Results Early for Fastest Design Turnaround

- TRCE Static Timing Analyzer computes worst-case logic path delays
  - Can compare timing to user constraints
- Use TRCE before, during and after PLACE AND ROUTE (PAR)
  - Before PAR (after MAP): Block delays + estimated net delays
  - During PAR (after placement): Block delays + estimated net delays based on placement
  - After PAR: Actual block and routing delays

# Sample Timing Analyzer Summary Report

-----  
Timing Analyzer M1.2.11

Copyright (c) 1995-1997 Xilinx, Inc. All rights reserved.

Design file: C:\mldemo\XPROJ\ver1\rev1\Flash.ncd

Physical constraint file: C:\mldemo\XPROJ\ver1\rev1\Flash.pcf

Device, speed: xc4003e, -2

Report level: error report, limited to 1 item per constraint

=====

Timing constraint: TS01 = MAXDELAY FROM TIMEGRP "FFS" TO TIMEGRP "FFS" 30 nS ;

37 items analyzed, 0 timing errors detected.

Maximum delay is 7.177ns.

Minimum period is 0.000ns.

-----  
Timing constraint: TS02 = MAXDELAY FROM TIMEGRP "BOUNCE8" TO TIMEGRP "8LED\_OUT"

30 nS ;

8 items analyzed, 0 timing errors detected.

Maximum delay is 12.124ns.

-----  
Timing constraint: TS03 = MAXDELAY FROM TIMEGRP "CLKIN" TO TIMEGRP "HALF\_CLK"

30 nS ;

5 items analyzed, 0 timing errors detected.

Maximum delay is 16.285ns.

-----  
All constraints were met.

# Sample Timing Analyzer Report (verbose)

Timing Analyzer M1.2.11

Copyright (c) 1995-1997 Xilinx, Inc. All rights reserved.

Design file: C:\mldemo\XPROJ\ver1\rev1\Flash.ncd  
Device, speed: xc4003e, -2  
Report level: verbose report, limited to 1 item per constraint

=====

Timing constraint: PATH "PATHFILTERS" = FROM TIMEGRP "SOURCES" TO TIMEGRP  
"DESTINATIONS" ;

41 items analyzed, 0 timing errors detected.

Maximum delay is 7.177ns.

-----

Delay: 7.177ns BOUNCE8/SEL to Q0 (4.757ns delay plus 2.420ns setup)

Path BOUNCE8/SEL to Q0 contains 2 levels of logic:

Path starting from Comp: CLB\_R8C9.K (from CLK)

To	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
-----			
CLB_R8C9.XQ	Tcko	2.820R	BOUNCE8/SEL
			BOUNCE8/SEL
CLB_R6C10.G3	net	1.937R	BOUNCE8/SEL
	Tick	2.420R	Q0
			BOUNCE8/\$1N68
			Q1

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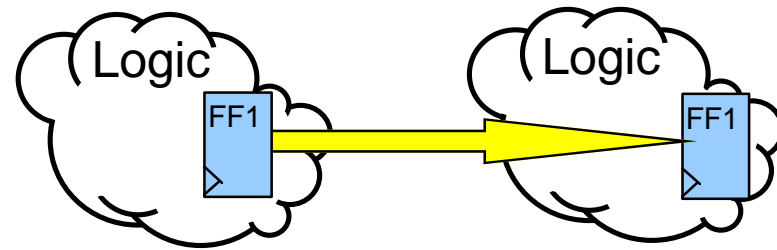
Total (73.0% logic, 27.0% route) 7.177ns (to CLK)

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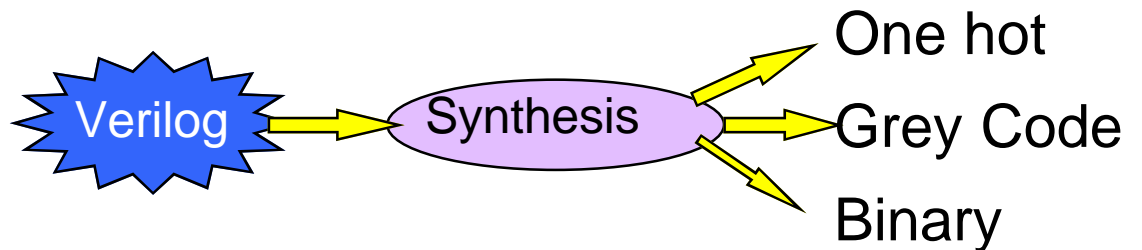
All constraints were met.

## More Tips For Controlling Timing

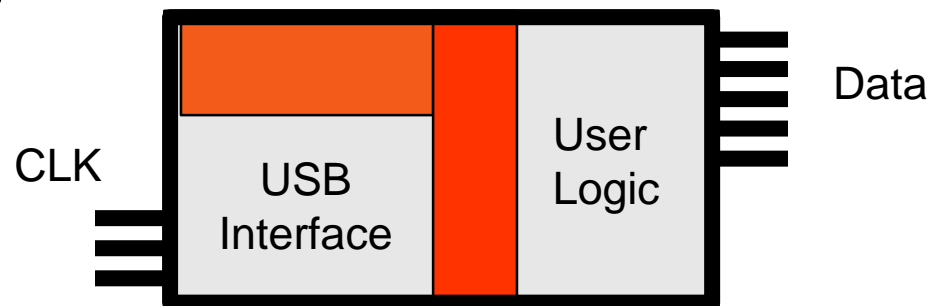
- Use pipeline registers
- Apply timing constraints to synthesis



- Let synthesis do state machine selection



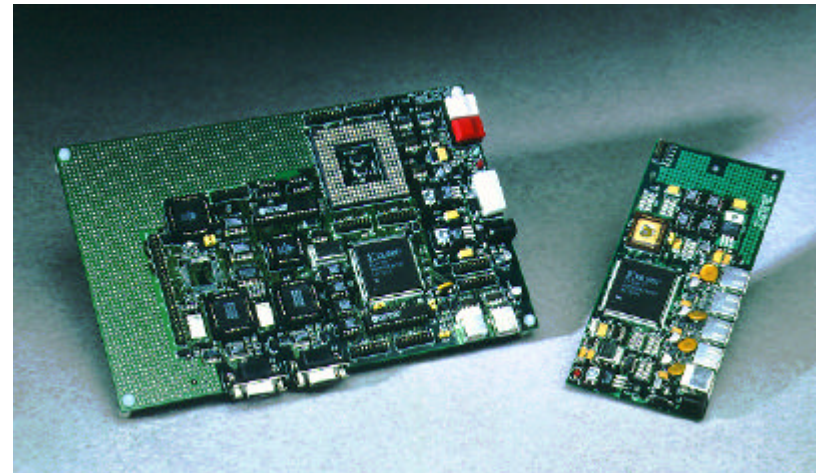
- Define broad area constraints
- Lock pins intelligently
  - Clock inputs
  - High speed data paths



# USB AllianceCORE



- Inventra (originally CAE Technologies)
  - IP business unit of Mentor Graphics
- Available USB Modules:
  - Low-speed (1.5 Mbps) function controller
  - Full-speed (12 Mbps) function controller
  - 3-port hub controller
- Supporting development tools
  - USB full system simulation model
  - Function and hub evaluation boards





# USB Case Study Summary

- Design captured in Verilog HDL
  - No architecture dependence in HDL code
- Push-button design flow using TIMESPECs
  - Let constraints drive synthesis and place-and-route tools
  - M1 Alliance Series tools follow constraint-driven methodology with robust verification capabilities
- Verified design and development tools available as AllianceCORE module from Inventra Systems