

August 6, 1996 (Version 1.1)

In anticipation of the market shift from 5 V to 3.3 V products, Xilinx introduced the Zero+ product line, the industry's first 3.3 V FPGAs, in 1993. The number of 3.3 V product offerings has since tripled and includes high-performance devices with system clock speeds of 85 MHz, high-density devices, and mixed-voltage devices.

Complete data sheets for the products mentioned below can be found in Chapters 3, 4, and 5 of this Data Book. 3.3 V versions of the Serial PROM devices also are available (see Chapter 6).

FPGAs

The Zero+ Family of Ultra Low Power Devices: XC3000L, XC4000L

The Zero+ Product Line includes two major families: the XC3000L and XC4000L FPGAs. These devices have quiescent supply currents below 1mA, with some below 50 μ A. This is important in systems where prolonged battery life is critical.

3 V PCI-Compliant FPGA: XC3100L

The XC3100L is the highest performance 3.3 V FPGA, and is the only 3.3 V FPGA family that meets the stringent specifications of 3.3 V PCI applications.

High-Density FPGAs With On-Chip RAM: XC4000L and XC4000XL

Ranging from 5,000 to over 60,000 gates, the XC4000L and XC4000XL FPGA families represent the broadest 3.3 V product line in the industry.

High-Density FPGAs Without On-chip RAM: XC5200L

The XC5200L family features 5 V compatible inputs and densities from 2,000 to 23,000 gates.

5 V Compatible Inputs on 3.3 V Devices

Conventional 3.3 V device inputs cannot or should not be driven substantially higher than 3.6 V. The new XC5200L inputs can, however, be driven up to 5.5 V, provided that the 5 V supply voltage is connected to one dedicated bias supply pin, called V_{TT} , on the 3.3 V device.

All Xilinx device inputs maintain their excellent protection against Electro-Static Discharge (ESD), typically 10,000 V, even in mixed-voltage applications.

5 V SRAM FPGAs for Mixed-Voltage Systems: XC4000E and XC4000EX

While the market slowly shifts from 5V systems to 3.3V systems, a need exists for devices to function in dual environments. The 5 V XC4000E and XC4000EX FPGA families feature a unique output structure which makes them suitable for mixed-voltage system applications. When configured in TTL mode, the XC4000E and XC4000EX can be directly mixed with 3.3 V devices without the aid of external components such as current limiting resistors. This is described in more detail under, "Interfacing Between 5 V and 3.3 V Devices" on page 7-2.

CPLDs

5 V CPLDs for Mixed-Voltage Systems: XC7300 and XC9500

Xilinx CPLDs are an excellent fit for 5 V only and mixed-voltage systems. The Input/Output (I/O) ring can be powered by either a 5 V V_{CCIO} or a 3.3 V V_{CCIO} . Independent of the V_{CCIO} voltage level, the inputs can accept 5 V and 3.3 V inputs. The rail-to-rail output level is defined by V_{CCIO} . These single-chip solutions function extremely well in mixed-voltage systems without any performance penalty.

Supply Voltage Options

	Availability	Single 3.3 V Supply	Single 5 V Supply	Dual Supply	Mixed-Voltage Applications			Key Features
					Core VCC = 5 V I/O VCC = 3.3 V Inputs are 5 V Compatible	VCC = 5 V Inputs are 3.3 V Compatible	VCC = 3.3 V Inputs are 5 V Compatible ¹	
Reconfigurable FPGAs						Yes		
XC3000A	Now		Yes					Low quiescent current
XC3000L	Now	Yes						μA powerdown current and μA quiescent current
XC3100A	Now		Yes			Yes		Highest performance 5 V FPGA
XC3100L	Now	Yes						Highest performance 3.3 V FPGA
XC4000E	Now		Yes			Yes		Mixed voltage system capable
XC4000L	Now	Yes						High Density 3.3 V FPGAs
XC4000EX	2H96		Yes			Yes		Mixed voltage system capable
XC4000XL	2H96	Yes		Note 2			Note 2	Highest Density 3.3 V FPGA
XC5200	Now		Yes			Yes		Best value and broadest density FPGAs
XC5200L	4H96	Yes		Yes			Yes	Best 3.3 V FPGA value
CPLDs								
XC7300	Now		Yes	Yes	Yes	Yes		Mixed voltage system capable
XC9500	2H96		Yes	Yes	Yes	Yes		Mixed voltage system capable

Notes: 1. Provided VTT pin is connected to 5 V supply.

2. Initial XC4000XL devices do not have 5 V tolerant inputs. Future XC4000XL devices will have 5 V tolerant inputs. Contact the factory.

Interfacing Between 5 V and 3.3 V Devices

This section discusses the compatibility issues between devices with different supply voltages, and explains how 5 V XC4000E/EX devices are directly compatible with 3.3 V devices.

In the past, almost all digital logic devices used a 5 V supply voltage. To reduce chip size and meet the demand for higher integration and lower power consumption, the semiconductor industry has started the transition to 3.3 V logic. In the future, 3.3 V will become the dominant supply voltage. Today, many designs must accommodate both types of ICs on the same board. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

3.3 V Devices Driving Inputs on 5 V Devices

The lowest output High voltage (VOH) of the 3.3 V device must exceed the VIH requirements of the 5 V device. This is not a problem if the 5 V device uses TTL-compatible input thresholds, available on all Xilinx devices. If, however, the 5 V device has CMOS input thresholds, an external pull-up resistor to 5 V on each such input will assure a sufficiently high input voltage. The resistor should be somewhere between 10 kΩ and 1 kΩ in value. The upper limit causes the rising input transition to be slow; the lower limit is set by the output current sinking capability of the 3.3 V device output. In the High state, the voltage will be clamped by the ESD protection diode of the 3.3 V device, as

described later in this application note. With less than 1.5 V across this resistor, the current will be fairly small, but care should be taken that the sum of these pull-up currents does not exceed the 3.3 V supply current, thereby reverse-biasing the power supply and raising the 3.3 V supply voltage to an undefined level (but obviously lower than the 5 V VCC minus a diode drop of ~0.7 V).

5 V Devices Driving Inputs on 3.3 V Devices

The highest 5 V device output voltage must not force excessive current into the input of the 3.3 V device. If the 5 V device has a truly complementary CMOS output (like all Xilinx FPGAs and CPLDs except the XC4000 family devices have), then the input current must be limited by a series resistor of no less than 150 Ω. This guarantees an input current below 10 mA, flowing through the ESD input protection diode backwards into the 3.3 V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3 V supply voltage above its 3.6 V maximum whenever a large number of active High inputs drive the 3.3 V device, potentially causing the 3.3 V supply current to go negative.

If the 5 V device has “totem-pole” n-channel-only outputs, VOH is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5 V supply does

not exceed 5.25 V. This is described in detail in the following section.

XC4000E/EX is Fully Compatible With 3.3 V Logic

As a default option, all XC4000E/EX have a TTL-like input threshold (compatible with 3.3 V output levels) and an n-channel-only “totem-pole” or TTL-like output structure with an n-channel transistor pulling the output to a VOH level that is one threshold below V_{CC} .

At a nominal 5.0 V V_{CC} , the unloaded output High voltage VOH is <3.7 V. When applied to the input of a device with a nominal 3.3 V V_{CC} , there is no additional input current, and the input level does not violate the conventional specification that prohibits input voltages more than 0.5 V above V_{CC} . See [Figure 1](#).

If both 5 V and 3.3 V supply voltages track reasonably between their max and min values, there will never be any additional input current in excess of 1 μ A at any commercial or industrial operating temperature.

A worst-case analysis of the interface might assume the (unrealistic) condition where the 5 V supply is at its max value (5.25 V for commercial applications), while the 3.3 V supply is at its min value of 3.0 V. Under these conditions, the interface violates the conventional specification, and drives current into the input of the 3.3 V device, as shown in figure 2. The following paragraphs explain that this interface is nevertheless reliable.

For protection against electro-static discharge (ESD), all CMOS inputs and I/O pins usually have a diode between the pin and the nearest V_{CC} connection. This diode prevents the input from going substantially more positive than V_{CC} , which might destroy the input transistor by rupturing its gate oxide. At room temperature, this ESD protection diode conducts negligible current at < 0.6 V forward bias, and conducts ~1 mA at ~0.7 V forward bias, typical for any silicon junction diode. These voltages have a predictable negative temperature coefficient of -2 mV per degree C. At 85 degrees C, these voltages are, therefore 120 mV lower.

Figure 1 superimposes the output characteristic of the XC4000E/EX and the input current characteristic of a typical 3.3 V device input. Both supply voltages are at their nominal value, but the die temperatures are at their worst-case value of 85 degrees C, and worst-case processing is assumed.

[Figure 2](#) shows the same curves, but with 5.25 V and 3.0 V V_{CC} respectively. The intersection of the two curves defines the worst-case operating point of 3.8 V and 6 mA. That

means that the XC4000E output drives 6 mA into the forward-biased ESD protection diode, raising the input voltage 0.8 V above 3.0 V, the assumed lowest value of the nominally 3.3 V supply voltage.

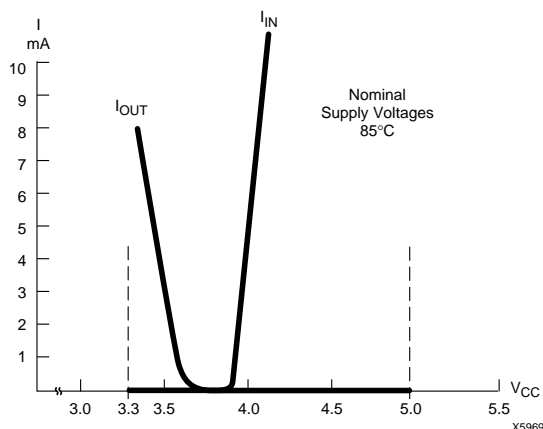


Figure 1: XC4000E Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Nominal Voltage (5.0 V and 3.3 V)

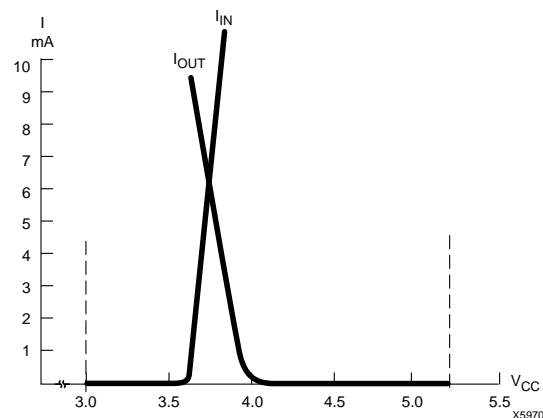


Figure 2: XC4000E Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Extreme Values (5.25 V and 3.0 V)

Although this input condition is not covered by the conventional specification, it does not cause any harm and does not affect reliability. ESD protection diodes are designed to conduct hundreds of mA, and the absolute value of the input voltage with respect to ground will never exceed 3.9 V. If the input pin is part of an I/O structure, there is theoretically possibility of causing latch-up, but all reputable IC manufacturers design their circuits such that latch-up does not occur below 100 mA of input current per pin.

The system designer must estimate the sum of all maximum input currents, and calculate the impact of this current flowing backwards towards the 3.3 V supply. But even if the total 3.3 V supply current goes to zero, V_{CC} for the 3.3 V device is still limited to < 3.6 V (the highest output voltage of the 5 V device minus the forward voltage drop of the ESD diode).

Conclusion

5 V XC4000E/EX devices can be freely mixed with 3.3 V devices, without any current or voltage limiting interface resistors, if the following conditions are met:

- The 5 V XC4000E/EX devices are in their default “TTL mode” with respect to input thresholds and output levels.
- The upper limit on the 5 V V_{CC} is 5.25 V and the lower limit on the 3.3 V supply is 3.0 V, as per standard commercial specifications.
- For industrial operating conditions with higher V_{CC} max, the user must make sure that the absolute difference between the two supply voltages does not exceed 2.20 V. Specifically, if the nominally 5 V V_{CC} is at its max value of 5.50 V, the nominally 3.3 V V_{CC} must not be lower than 3.30 V.