

## Solutions for the DSP Market



KC & PH (Xilinx) June 1996



## Solutions for the DSP Market

**Presenter**

Ken Chapman - Applications Specialist  
Xilinx UK

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# RAM Based Multiplier for FPGAs

## Solutions for the DSP Market

### Agenda

- **Zooming in** - The Xilinx Device Range.
- **Concepts** - Brief Overview of the Xilinx FPGA Architecture.
- **Algorithms** - What are the requirements of DSP?
- **FPGA's vs DSP Requirements** - A closer look at the XC4000E
- **Tradition** - The limit of DSP processors.
- **Back to basics** - building the right blocks.
- **Solutions** - Some case studies from Europe.

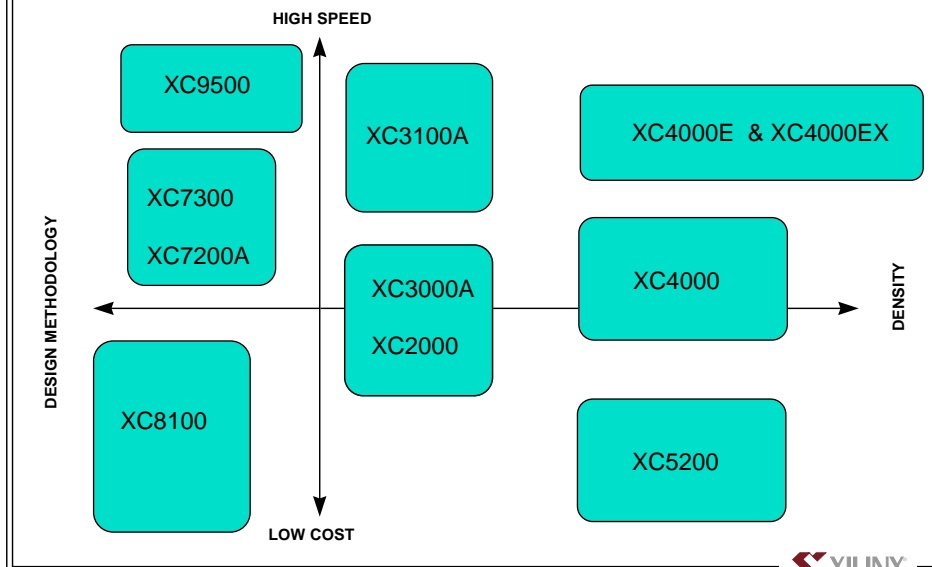
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## Xilinx Components Today...

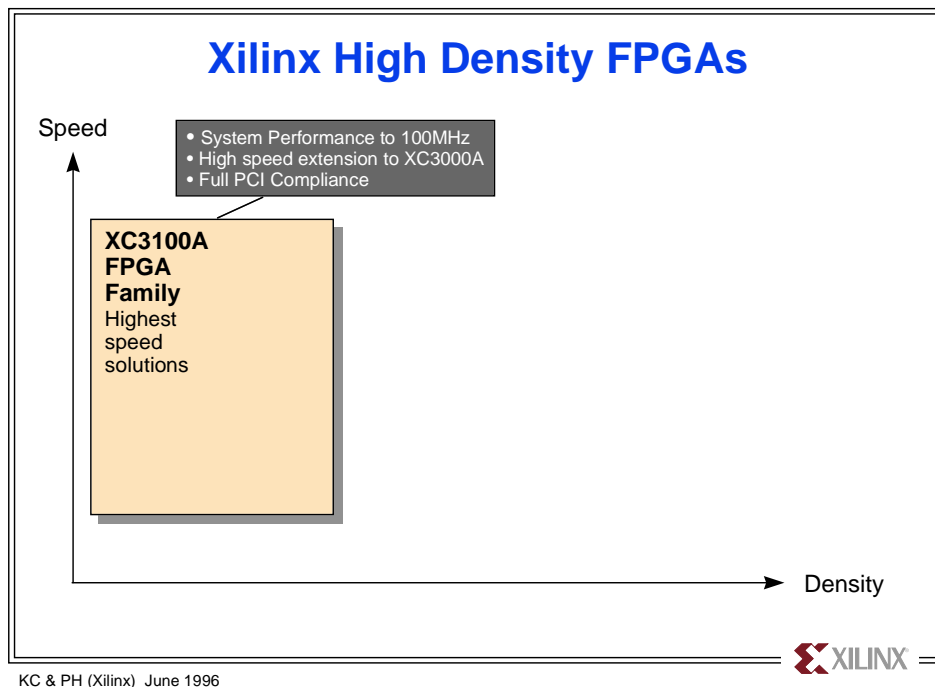
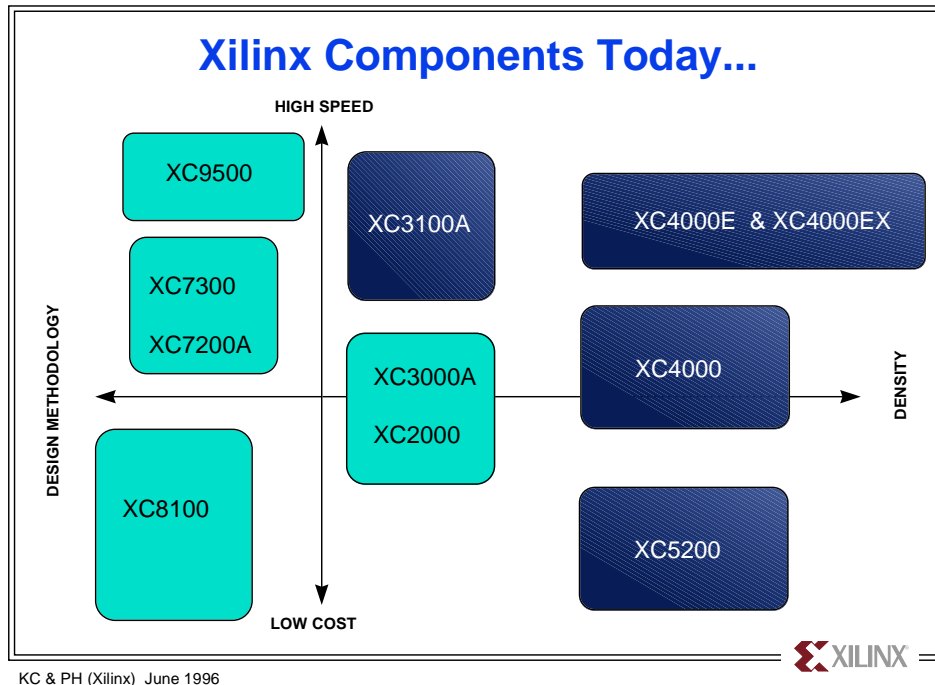


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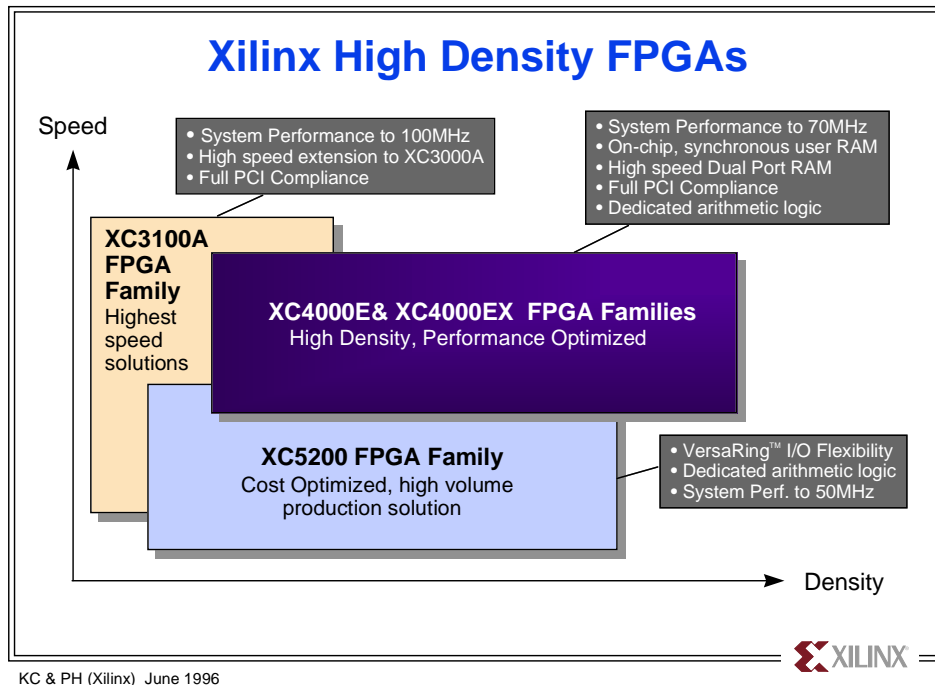
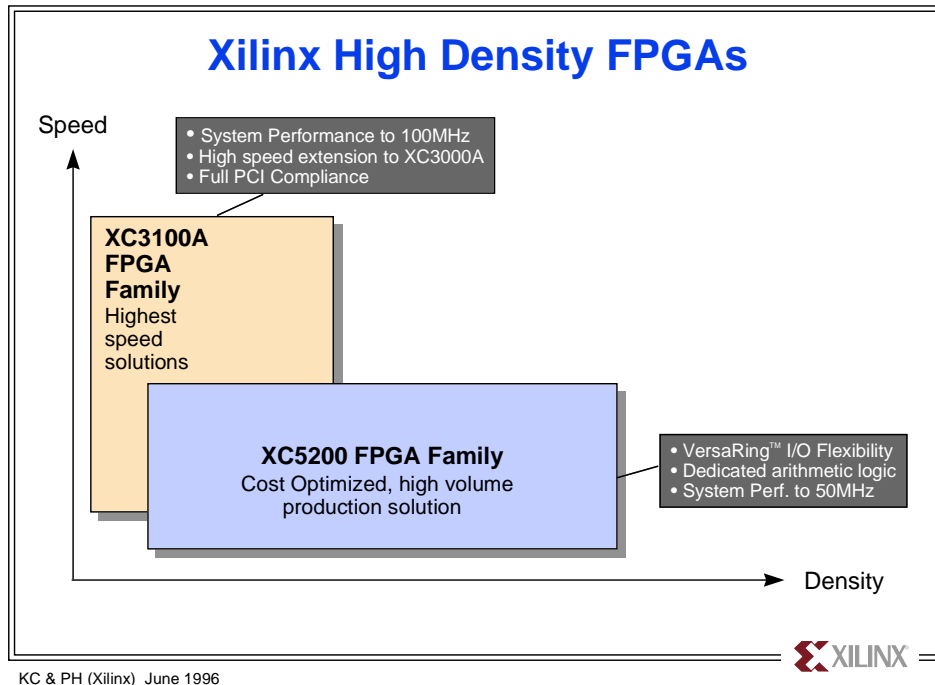


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# RAM Based Multiplier for FPGAs

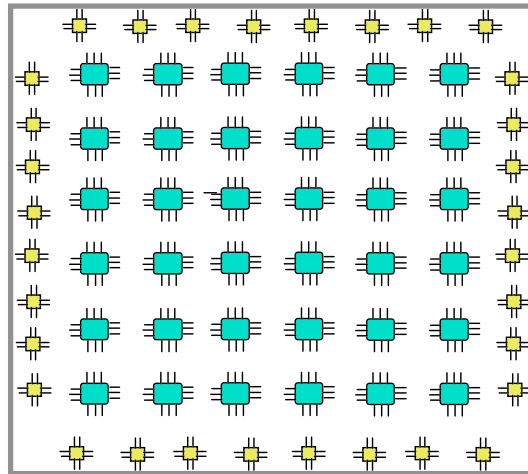


# RAM Based Multiplier for FPGAs



# RAM Based Multiplier for FPGAs

## FPGA Architecture



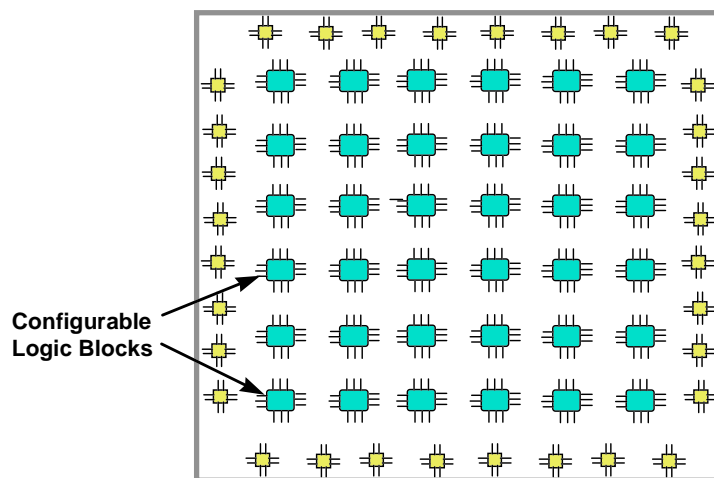
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## FPGA Architecture

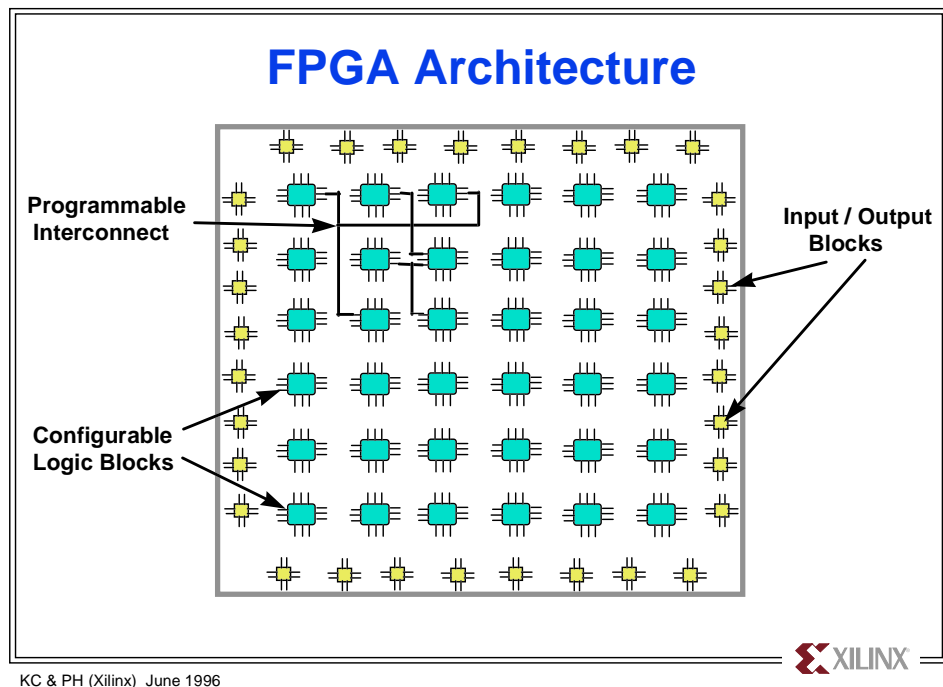
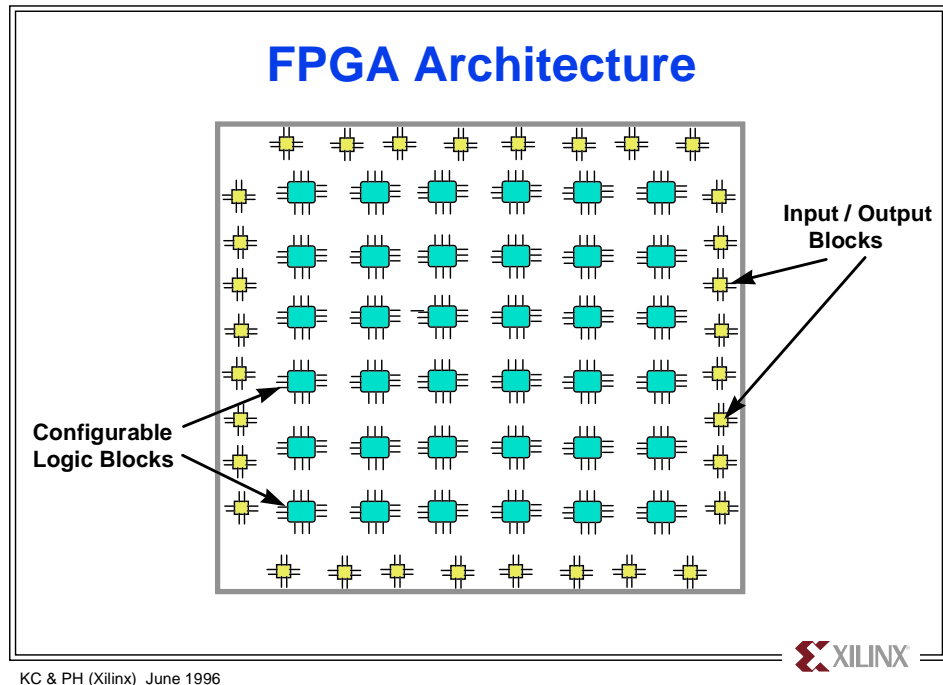


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# RAM Based Multiplier for FPGAs



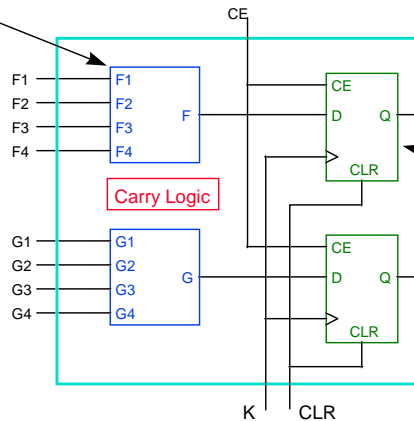
# RAM Based Multiplier for FPGAs

## Configurable Logic Block (CLB)

### Function Generators

- Implement GATES of design
- Can be used as **ROM**
- Various **RAM** Options
- Combine with **Carry Logic** to form many Arithmetic functions

D	C	B	A	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1



### Flip-Flops

- Optional use
- Variety of controls
- Polarity options on control signals



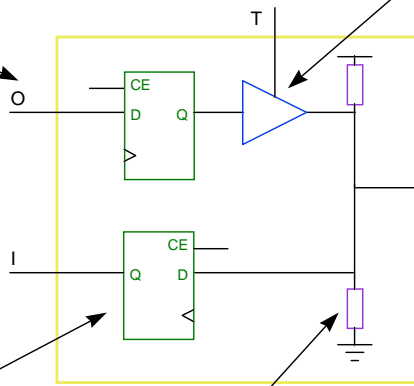
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## Configurable I/O Block (IOB)

Polarity control on data and controls



### Three-State Buffer

- Optional
- Bus signals
- Open Collector

### Pad

- Many package Types
- Sink 12mA
- TTL & CMOS
- Slew rate Control
- Soft start up
- IEEE 1149.1 Boundary Scan

### Flip-Flops

- Optional use
- Clock enable available
- ZERO hold time

### Passive Pull-up & Pull-down

- Optional
- 50-100K Ohm



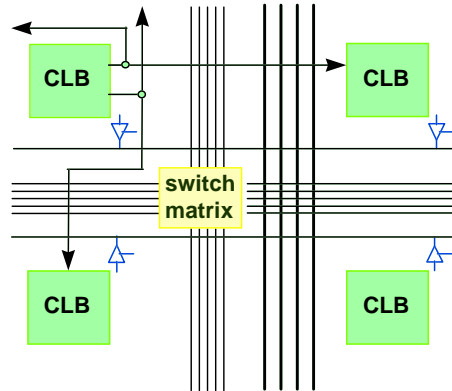
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# RAM Based Multiplier for FPGAs

## Programmable Interconnect

- Resources to create arbitrary interconnection networks
- Hierarchy of interconnect resources
- Programmable switches
- Internal 3-state buffers for busses, mux's, and wide functions
- Dedicated global clock networks
- Global reset and tri-state networks



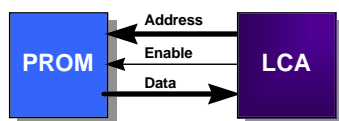
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## Configuration



### FEATURES

- **Master mode**
  - 'Self Configuration' from PROM
  - Parallel (shown) or serial modes
- **Peripheral mode**
  - Dynamic reprogramming via external system (microprocessor)

### BENEFITS

- **Field Upgrades via Software Changes**
- **Built-in System Test/Diagnostic Logic**
- **Adaptable System Design**
  - Hardware changes & tuning possible during prototype AND OPERATION!
- **Examples**
  - Separate Read/Write Logic - Tape Drive
  - Evolving Communications Protocols



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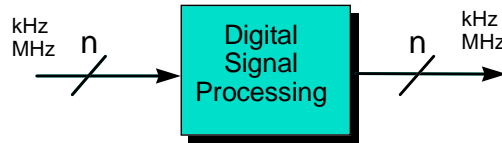
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# RAM Based Multiplier for FPGAs

## Algorithms: What are the requirements for DSP?



There are really only 4 functions:

DELAY

ADDITION/SUBTRACTION

MULTIPLICATION

DATA STORAGE

Question becomes: How BIG and how FAST can these be implemented in an FPGA?

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## FPGA Architectural Requirements

### Operation:

- Delays
- Addition / Subtraction
- Multiplication
- Data Storage

### Preferred Feature:

Register Intensive Part.  
FIFO Capability.

Built-in Arithmetic Capability  
- Improves speed & reduces logic area.

Fast Arithmetic Capability  
On-Board RAM/ROM  
Pipelining Capability

On-Board RAM/ROM

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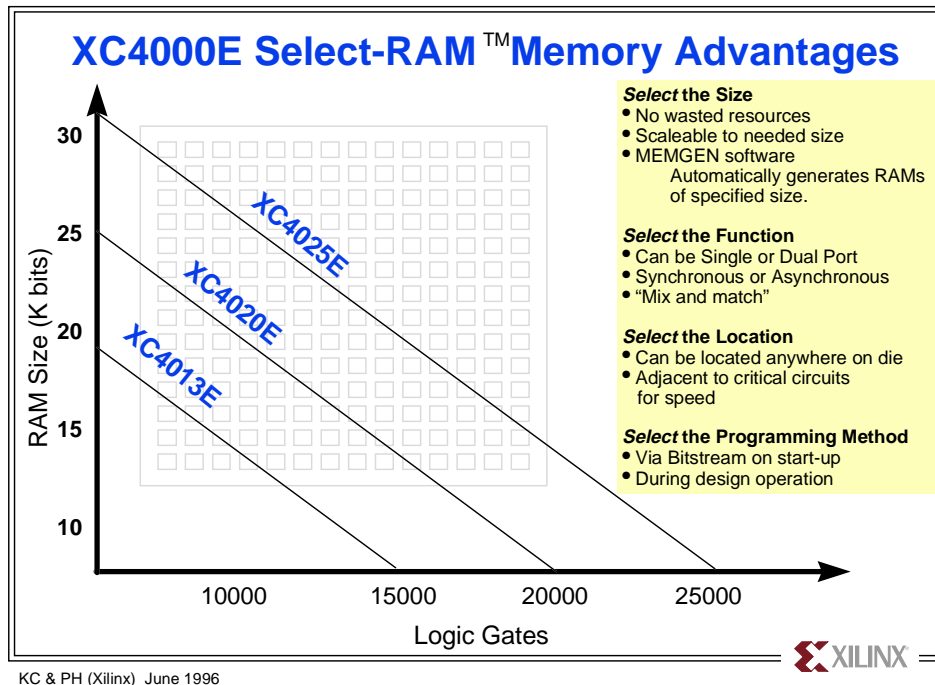
# RAM Based Multiplier for FPGAs

## XC4000E Architectural Features

Features:	Advantage to DSP:
<b>Register Intensive Parts</b> <ul style="list-style-type: none"> <li>• Clock Enable to ALL Flip-flops</li> <li>• Asynchronous Set/Preset to CLB Flip-flops.</li> </ul>	<b>Pipelining &amp; Data Delays</b> <ul style="list-style-type: none"> <li>• Fast system level I/O</li> <li>• &gt;2000 Flip-flops (XC4025E)</li> </ul>
<b>Fast Built-in Carry Logic</b> <ul style="list-style-type: none"> <li>• Fully Reconfigurable.</li> </ul>	<b>Arithmetic Functions</b> <ul style="list-style-type: none"> <li>• Fast Addition / Subtraction 16-bit Add = 17ns (-3)</li> <li>• Fast Comparators</li> <li>• Multipliers</li> </ul>
<b>Select-RAM</b> <ul style="list-style-type: none"> <li>• High Speed.</li> <li>• Synchronous &amp; Asynchronous modes.</li> <li>• Single &amp; Dual Port Operation.</li> <li>• Configurable RAM Content.</li> </ul>	<b>Data Storage &amp; Delays</b> <ul style="list-style-type: none"> <li>• Coefficient Tables.</li> <li>• Cyclic Buffers.</li> <li>• FIFO's.</li> <li>• Multipliers.</li> <li>• Sizable to Application</li> </ul>

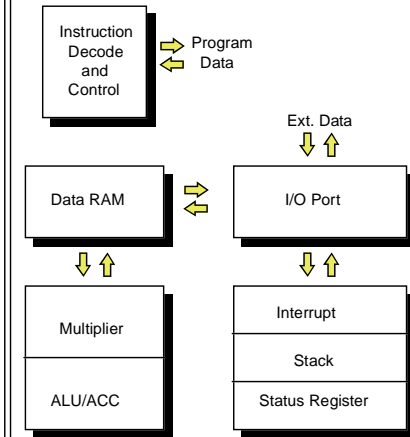
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# RAM Based Multiplier for FPGAs

## Tradition - The limit of DSP Processors



Typical DSP Device Architecture

### Very Good Devices

- Microprocessor Architecture.
- Special Multiply and Accumulate Instruction.
- On chip memory for program and data.
- Programmed by software.
- Instruction times down to 12ns (80MHz).

### Limitations

- Fixed Architecture.
- Fixed bit sizes.
- SEQUENTIAL processing.

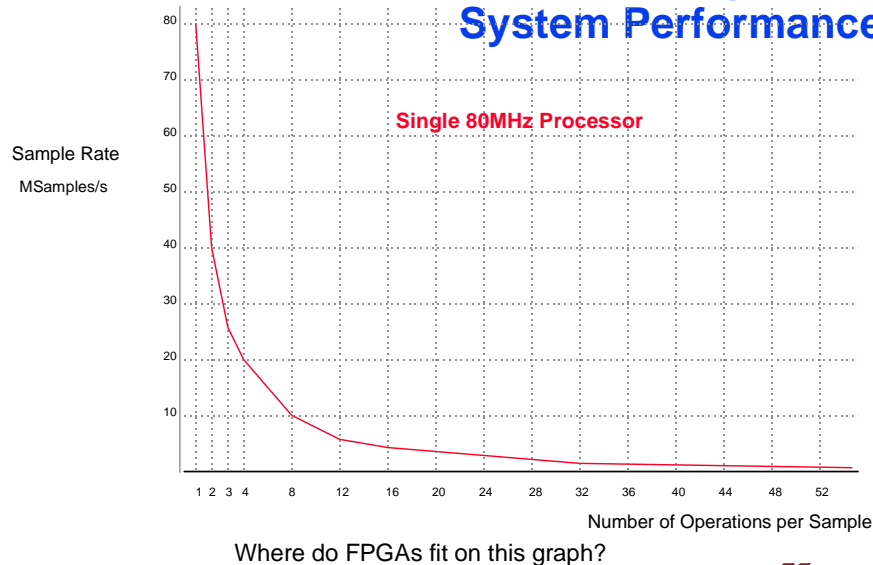
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## Traditional Sequential Processing Limits System Performance



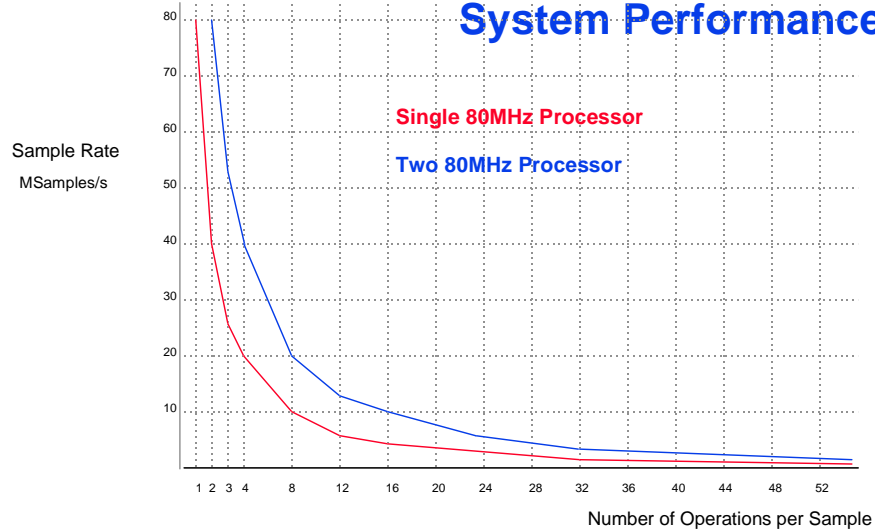
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# RAM Based Multiplier for FPGAs

## Traditional Sequential Processing Limits System Performance



Where do FPGAs fit on this graph?

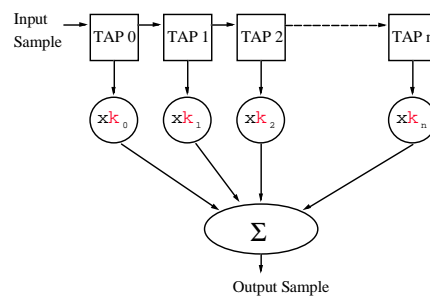


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## DSP Algorithms are Parallel



FIR filter

$$D_{OUT} = \sum_{n=0}^{n=15} k_n t_n$$

### Implementation Method

Sequential (Traditional DSP)

Parallel (Distributed Arithmetic)

### Requirements

ONE full function multiplier

Multiple Constant Coefficient multipliers

### Performance

LOW

HIGH

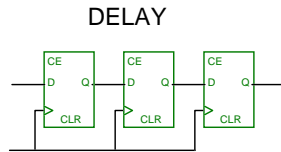


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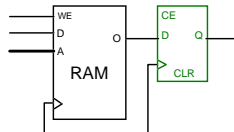
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# RAM Based Multiplier for FPGAs

## Building the right Blocks



2-Bits per CLB

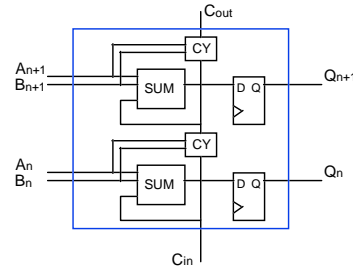


32-Bits per CLB

### DATA STORAGE

Registers - 2 bits per CLB  
RAM / ROM - 32-Bits per CLB

### ADDITION/SUBTRACTION



2-Bit Add/Subtract per CLB

### MULTIPLIERS

These require a little more effort.....

All Functions expand to SIZE REQUIRED at point in Algorithm



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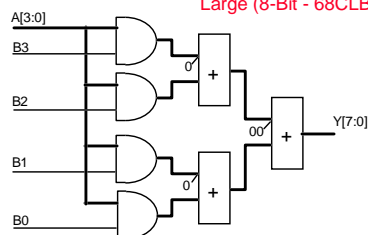
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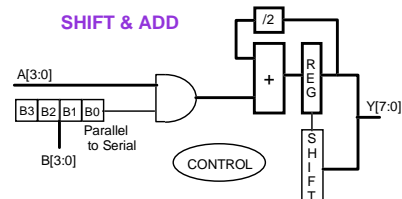
## MULTIPLICATION - Typically 4 Methods

### ADDER TREE

Fast (8-Bit - 65MHz)  
Large (8-Bit - 68CLB)



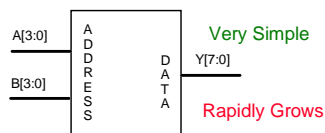
### SHIFT & ADD



Compact (8-Bit - 20CLB)  
Slow (multi-cycle)  
8MHz SYSTEM performance may be high!

### LOOK-UP TABLE

A ROM is pre-programmed with all possible answers



Very Simple  
Rapidly Grows

### LOGICAL TREE

A huge exercise in Boolean Algebra!  
Each bit out is an equation of the inputs.

Can be Fast Complex & Very Large



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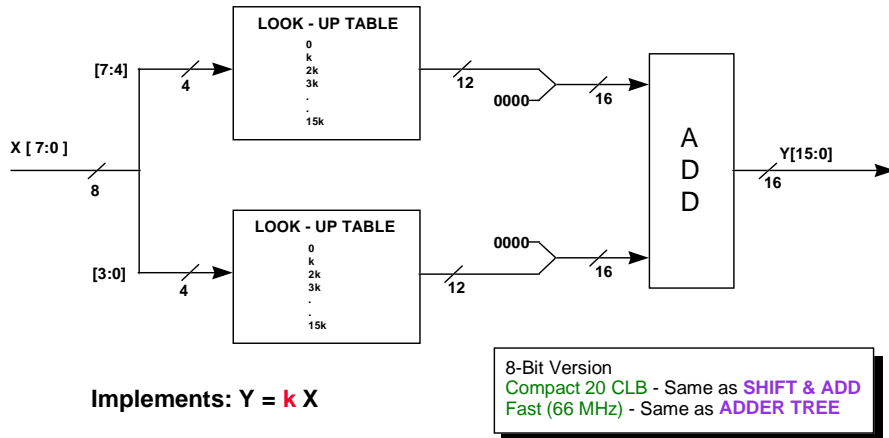
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# RAM Based Multiplier for FPGAs

## Method 5 - The Hybrid Multiplier

Constant (k) Coefficient Multiplier (KCM)

Effectively performs a **HEXADECIMAL** multiplication



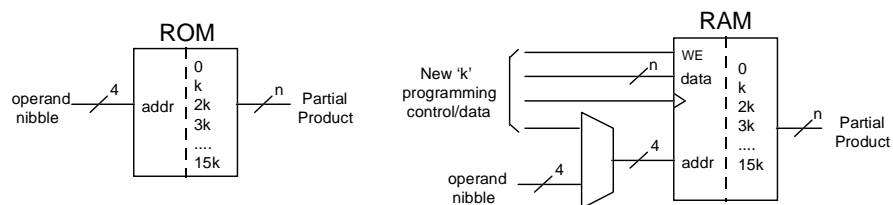
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## Implementation of Look-Up Tables



**Fixed Constant**  
(variable by configuration!)

**Variable Constant !**

**What is required?**

- Option to use ROM and yet still 'tune' value by ISP
- Ability to choose RAM if required
- Ability to build RAM of exact width required
- Ability to build RAM/ROM exactly where it is needed on the die
- Ability to build as many blocks of memory as required
- Ability to preset an initial value on configuration

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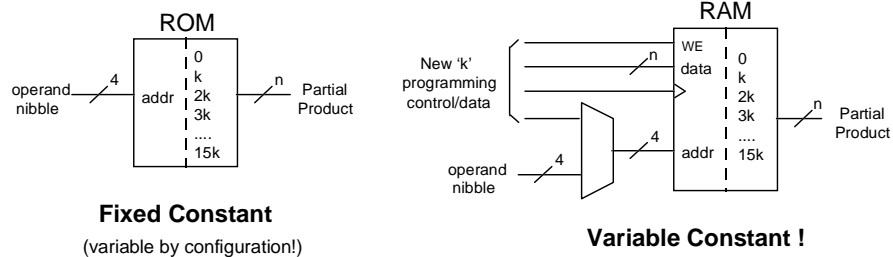
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# RAM Based Multiplier for FPGAs

## Implementation of Look-Up Tables



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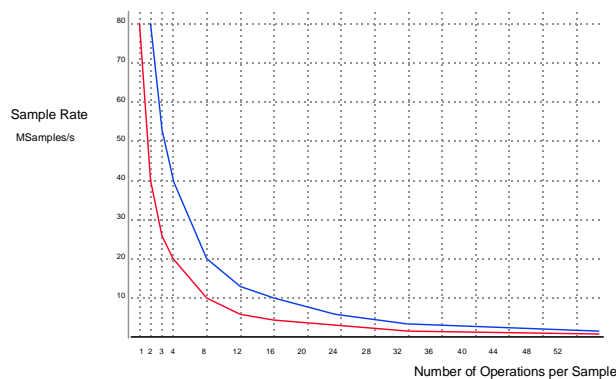
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## Performance of KCM's

Results for the fully available -3 speed grade ( -2 speed offering ~14% improvement)

Operand Size	Combinatorial Delay (ns)	CLB's	Pipelined Performance (MHz)	No. of Stages	CLB's
8	19	19	66.5	2	20
10	29	39	58.2	2	40
16	41	75	50.0	3	80



Figures are worst case and measured IN-SYSTEM

Defines the upper SYSTEM performance and size for Xilinx DSP Solutions

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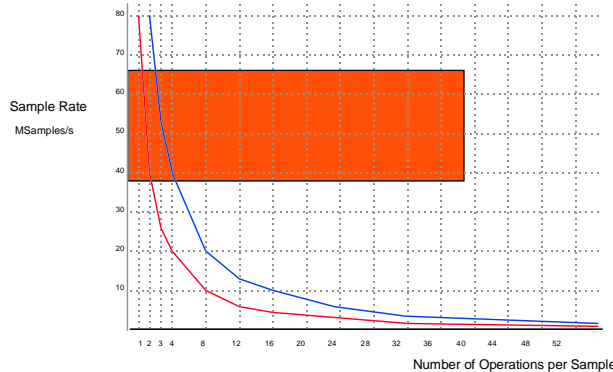


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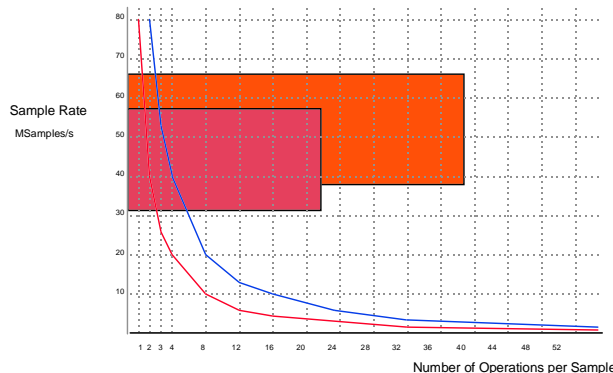
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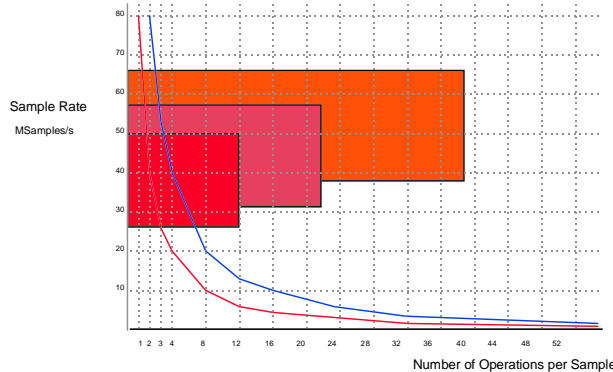


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16-Bit MACs/XC4025-3



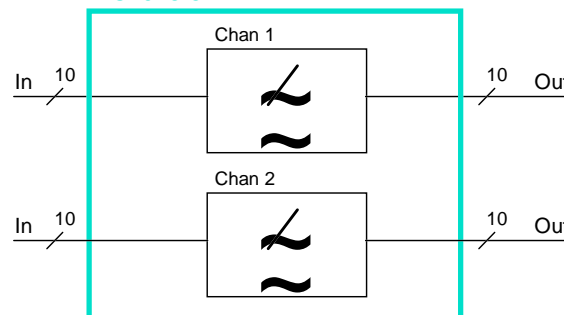
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## Real Solution 1 - 55MHz Low Pass Filters

XC4013-3



**Application** • Front end filters for Measurement Equipment.

**Requirement** • Each filter required 6 taps FIR (symmetrical) with 10-bit data and coefficients.  
• Sample rate of 55 Msamples/second.  
• Coefficients to be fixed after initial system tuning phase.

**Solution** • Single device solution offering 30% of device for additional system logic.  
• Full parallel Processing - Equivalent to over 600 MOPs processing.  
• Implementation performed completely by customer.



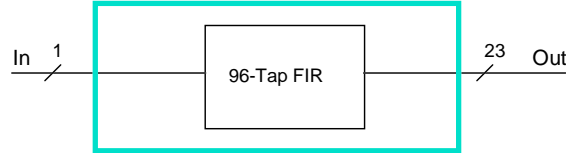
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# RAM Based Multiplier for FPGAs

## Real Solution 2 - 2.2MHz Bit-Filter/Correlator

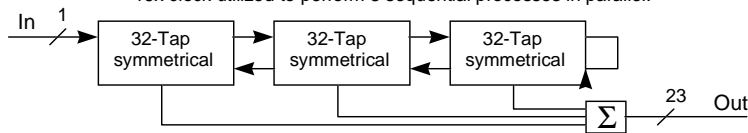
XC4005E-4



**Application** • Base-Station Communications Bitstream processing.

**Requirement** • A 96-Tap FIR filter structure (symmetrical) with 16-bit coefficients  
• Coefficients liable to modification during life time of design.  
• Sample rate of just below 2.2 Msamples/second.

**Solution** • Single device solution offering 22% of device for additional system logic.  
• Slowest speed grade available - Higher data rates instantly available.  
• Distributed RAM and ROM employed for samples and coefficients.  
• Mixed Sequential and Parallel technique - Equivalent to over 200 MOPs processing.  
• Basic Implementation performed by Xilinx.  
• 16x clock utilized to perform 3 sequential processes in parallel.



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## Real Solution 3 - Data Routing & Sequencing

XC4013E-4

**Application**

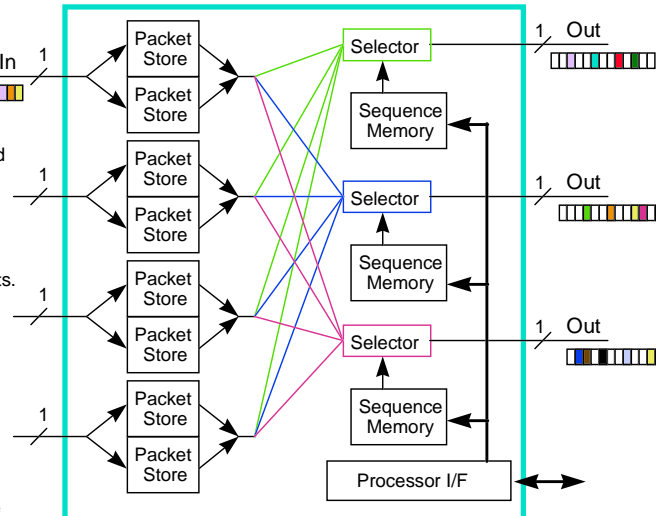
• Communications Noise Reduction System (Spread channel communications).

**Requirement**

• Record 256-bit packets on four 2 MBit/s channels.  
• Segment into 2-bit elements.  
• Route any element to any output at any.  
• Total control from uP.

**Solution**

• Single device solution.  
• 11 blocks of RAM - total of 5760 bits.  
• Implementation performed by customer and Xilinx.  
• System requirements were evolving by the DAY and a 4 week time-scale.



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## Solutions for the DSP Market

### Summary

- **Zooming in** - Large Xilinx Device Range for many applications and methodologies.
- **Concepts** - Xilinx FPGA Architecture offers a completely flexible approach to design.
- **FPGA's vs DSP Requirements**- XC4000E offers the density and performance for DSP.
- **Algorithms** - Consider the algorithm structure to optimize the logic design (cost).
- **Tradition** - Sequential processing and fixed architectures limit system performance.
- **Back to basics** - Mastering the basics and asking the right questions about the algorithm.
- **Solutions** - 2MHz or 55MHz, Multiplication or Data Manipulation, Flexible and Successful.

**Try Xilinx**

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## Solutions for the DSP Market

***THANK YOU***

Xilinx European Applications

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