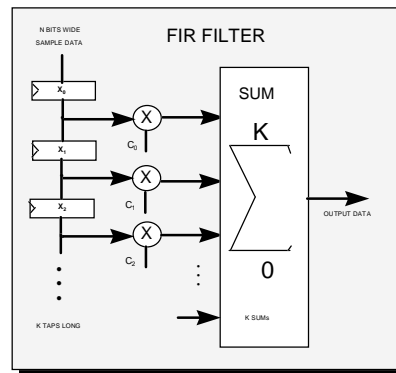


SEMINAR

SIGNAL PROCESSING with XILINX FPGAs

Bruce Newgard



Slide Number 1 9/2/96 19:55 XDSP.PPT

XILINX X.D.S.P.

SIGNAL PROCESSING WITH **XILINX** FPGAs CONFIGURABLE HARDWARE DSP SOLUTIONS

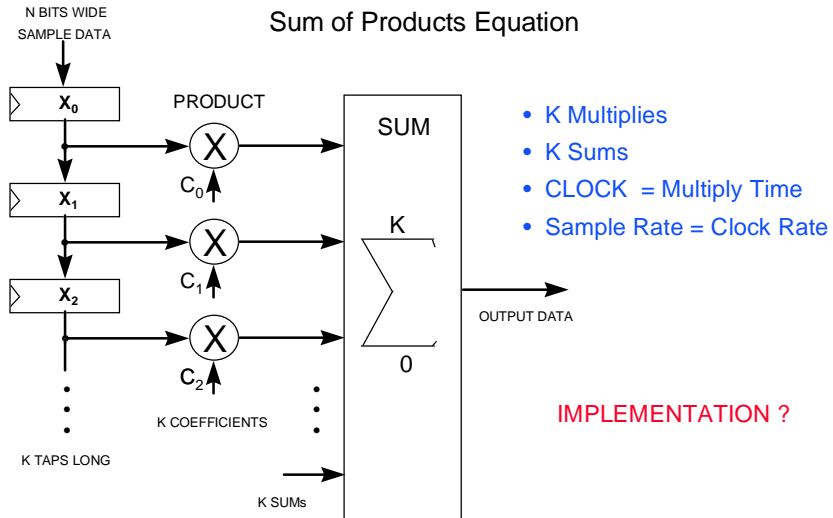
- Distributed Arithmetic
- XC4000 Arch Summary
- DA - FIR filter example
- 8 Tap *SLICE*
- High Speed FIR
- Low Speed FIR
- Decimating FIR
- Interpolating FIR
- IIR Biquad
- Correlators
- XDSP Case Studies
- Design Methodology
- Summary

Slide Number 2 9/2/96 19:55 XDSP.PPT

XILINX X.D.S.P.

FIR FILTER EXAMPLE

Sum of Products Equation

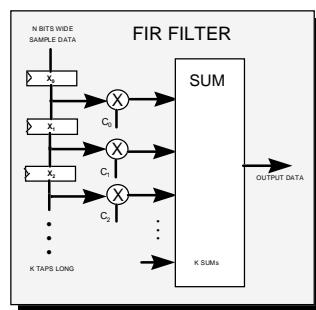


Slide Number 3 9/2/96 19:55 XDSP.PPT

XILINX X.D.S.P.

FIR FILTER EXAMPLE

PROGRAMMABLE DSP CHIP IMPLEMENTATION



SOFTWARE SOLUTION:

- 1 Parallel Multiplier, Accumulator
- Time Share through Microcoding
- Relatively Low Sample Rates
- Multiple Chip Solution
- No Migration Path
- Complex Real Time Programming


FOR EACH SAMPLE DATA WORD
FOR EACH TAP
MULTIPLY $C(i)$ TIMES $X(i)$
ADD RESULT TO ACCUMULATOR

Slide Number 4 9/2/96 19:56 XDSP.PPT

XILINX X.D.S.P.

Distributed Arithmetic Basics


Slide Number 5 9/2/96 19:56 XDSP.PPT

 X.D.S.P.

2's Complement Arithmetic

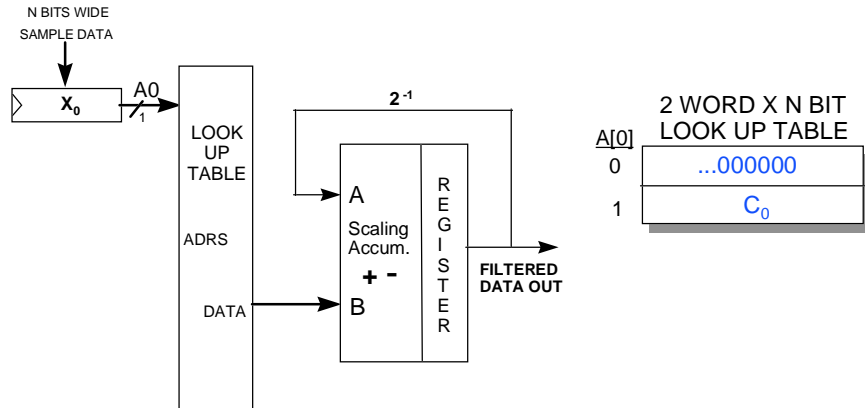
$$\begin{array}{r}
 \begin{array}{c}
 -2^7 \ 2^6 \ 2^5 \ 2^4 \ 2^3 \ 2^2 \ 2^1 \ 2^0 \\
 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ (-127) \\
 \hline
 X \quad 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ (\ 5) \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ \textcolor{red}{1} \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{1} \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 1 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \\
 \quad \quad \quad + \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 \quad \quad \quad \textcolor{red}{1} \ 1 \ 1 \ 1 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \\
 \quad \quad \quad - \textcolor{red}{0} \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \\
 \hline
 1 \ 1 \ 1 \ 1 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 1 \ (FD85 = -635)
 \end{array}
 \end{array}$$

Slide Number 6 9/2/96 19:56 XDSP.PPT

 X.D.S.P.

D.A. ONE TAP FIR FILTER = $X_0 C_0$

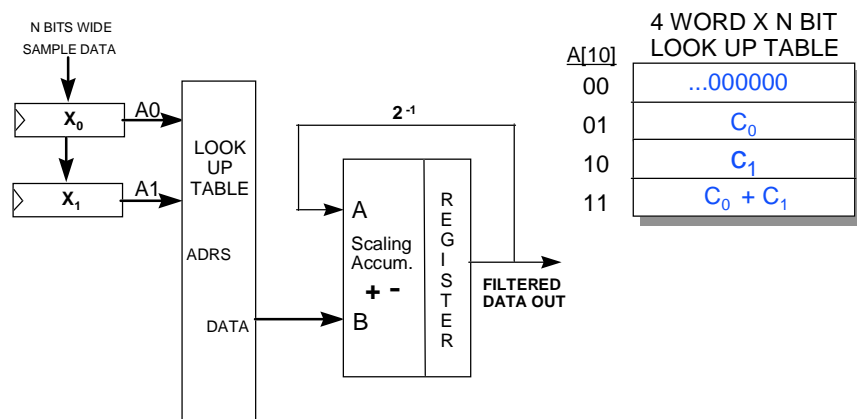
REDUCES TO MULTIPLYING A VARIABLE TIMES A CONSTANT



Slide Number 7 9/2/96 19:57 XDSP.PPT

XILINX X.D.S.P.

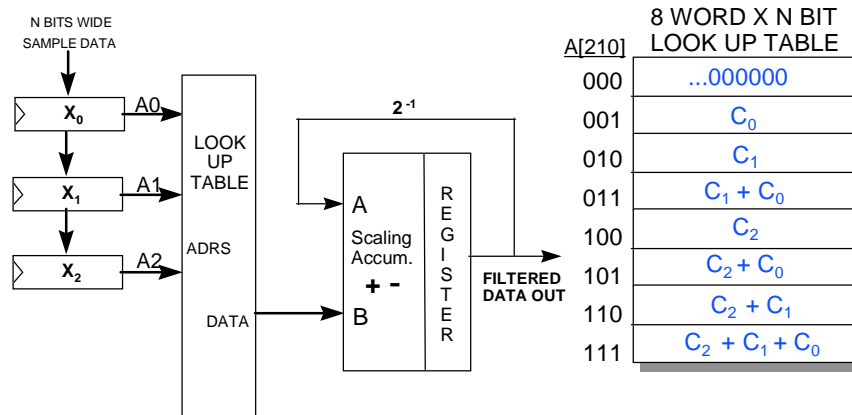
D.A. TWO TAP FIR FILTER



Slide Number 8 9/2/96 19:57 XDSP.PPT

XILINX X.D.S.P.

D.A. THREE TAP FIR FILTER



Slide Number 9 9/2/96 19:58 XDSP.PPT

XILINX X.D.S.P.

XC4000E ARCHITECTURE

Slide Number 10 9/2/96 19:58 XDSP.PPT

XILINX X.D.S.P.



XC4000E Family Profile

Device	4003E	4005E	4006E	4008E	4010E	4013E	4020E	4025E
Gates	3000	5000	6000	8000	10000	13000	20000	25000
Array	10x10	14x14	16x16	18x18	20x20	24x24	28x28	32x32
RAM Bits	3,200	6,272	8,192	10,368	12,800	18,432	25,088	32,768
CLBs	100	196	256	324	400	576	784	1024
Flip Flops	360	616	768	936	1120	1536	2016	2560
Max.I/O	80	112	128	148	160	192	224	256

Slide Number 13 9/2/96 19:59 XDSP.PPT

XILINX X.D.S.P.



XC4000EX High Density Family

	1996					1997	
	4028EX	4036EX	4044EX	4052EX	4062EX	4085EX	40125EX
Typ Logic Gates	28,000	36,000	44,000	52,000	62,000	85,000	125,000
Typ System Gates* (Logic + Select-RAM)	48-56K	60-72K	75-90K	90-110K	105-130K	125-170K	165-200K
Avail RAM bits	32,768	41,472	51,200	61,952	73,728	86,528	115,200
CLB Array	32 x 32	36 x 36	40 x 40	44 x 44	48 x 48	56 x 56	68 x 68
Number CLBs	1,024	1,296	1,600	1,936	2,304	3,136	4,624
Flip-Flops	2,560	3,168	3,840	4,576	5,376	7,168	10,336
I/O	256	288	320	352	384	446	544
Packages:	HQ208						
	HQ240						
100% Footprint Compatible	PG299						
	HQ304	HQ304					
	BG352						
	BG432	BG432	BG432	BG432			
* 20-30% of CLBs as RAM	PG411	PG411	PG411	PG411	PG499	PG499	
				BG596	BG596	BG596	BG596

Slide Number 14 9/2/96 20:00 XDSP.PPT

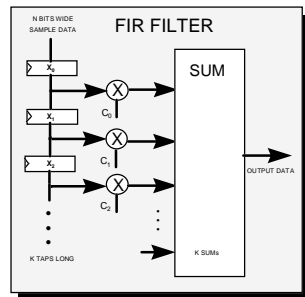
XILINX X.D.S.P.

The Development of a Distributed Arithmetic FIR Filter

10 Bit 10 Tap - XC4000E Family Example

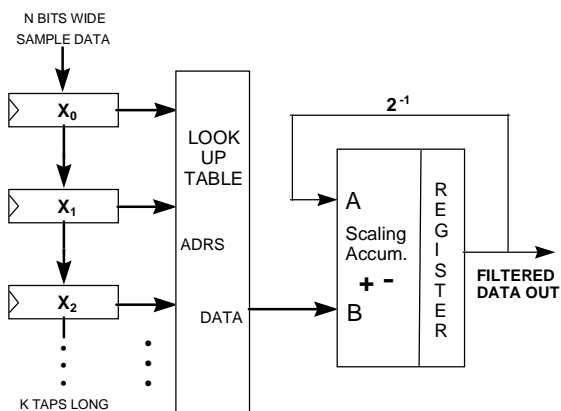
Slide Number 15 9/2/96 20:00 XDSP.PPT

XILINX X.D.S.P.



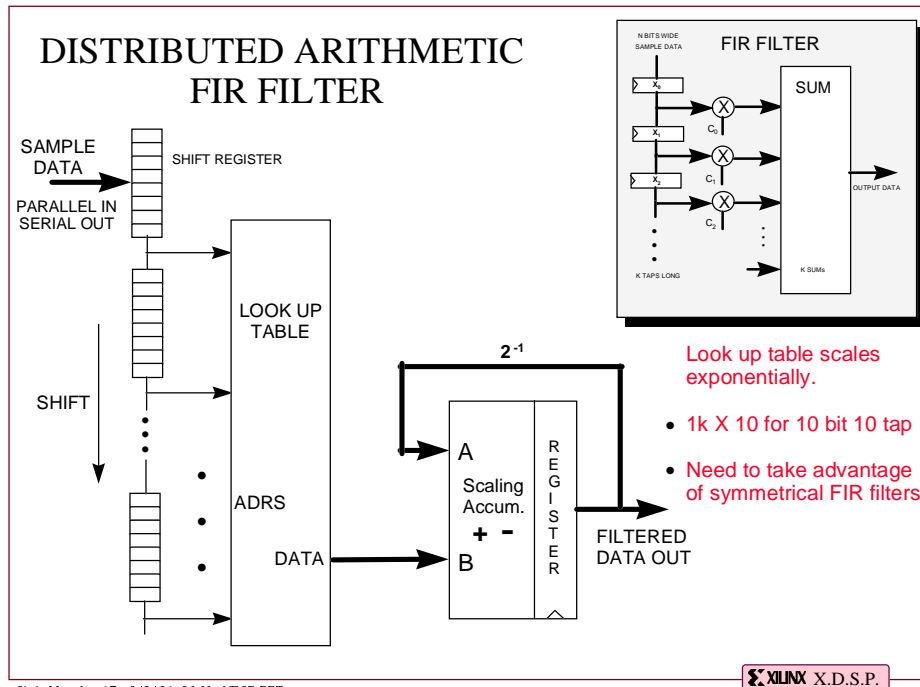
- N Clocks per Sample Word
- Fast Clock
- No Multiplier Required
- Embedded Hardware Solution
- LUT Holds Coefficients & Mult.

FIR FILTER EXAMPLE DISTRIBUTED ARITHMETIC SOLUTION

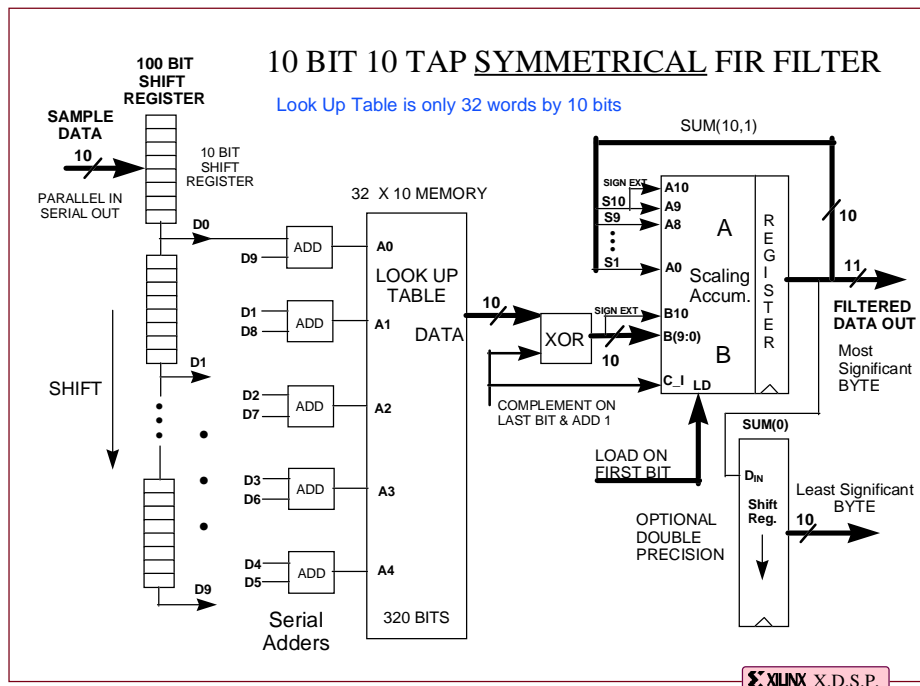


Slide Number 16 9/2/96 20:00 XDSP.PPT

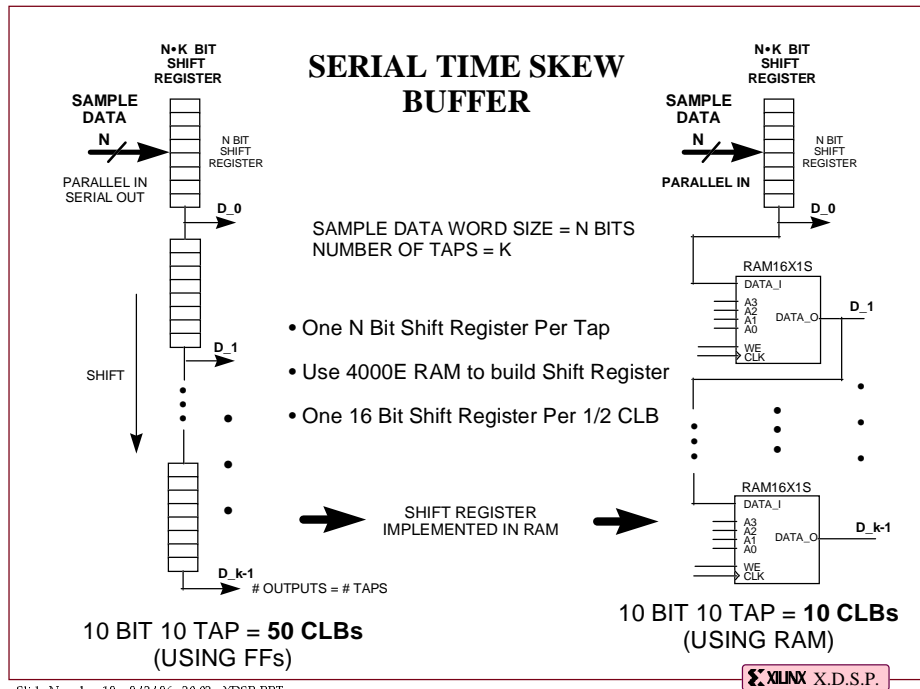
XILINX X.D.S.P.



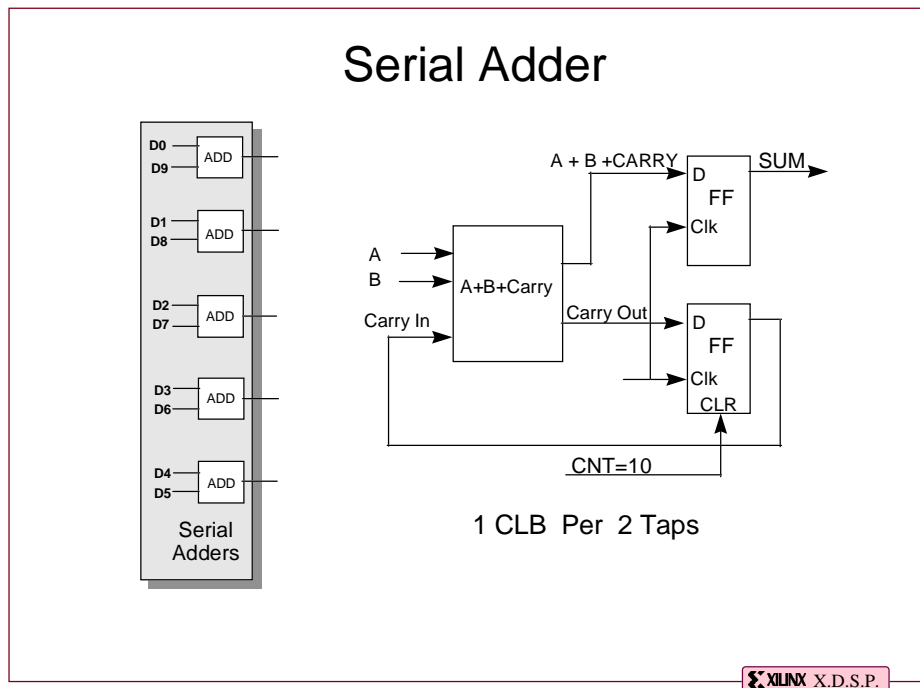
Slide Number 17 9/2/96 20:00 XDSP.PPT



Slide Number 18 9/2/96 20:01 XDSP.PPT

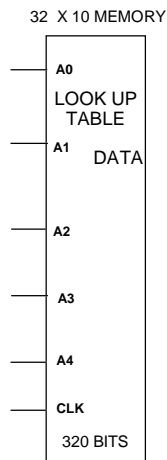


Slide Number 19 9/2/96 20:02 XDSP.PPT



Slide Number 20 9/2/96 20:02 XDSP.PPT

DISTRIBUTED ARITHMETIC LOOK-UP TABLE

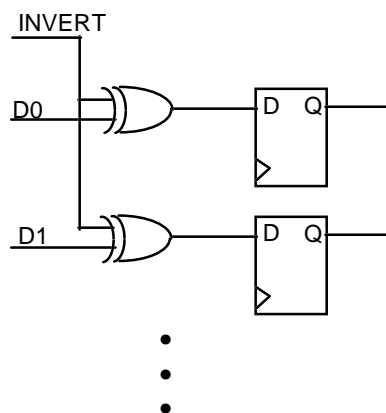


- HOLDS ALL PARTIAL PRODUCTS
- LUT IS AS WIDE AS COEFF
- USE MEMGEN TO BUILD LUT

Slide Number 21 9/2/96 20:03 XDSP.PPT

XILINX X.D.S.P.

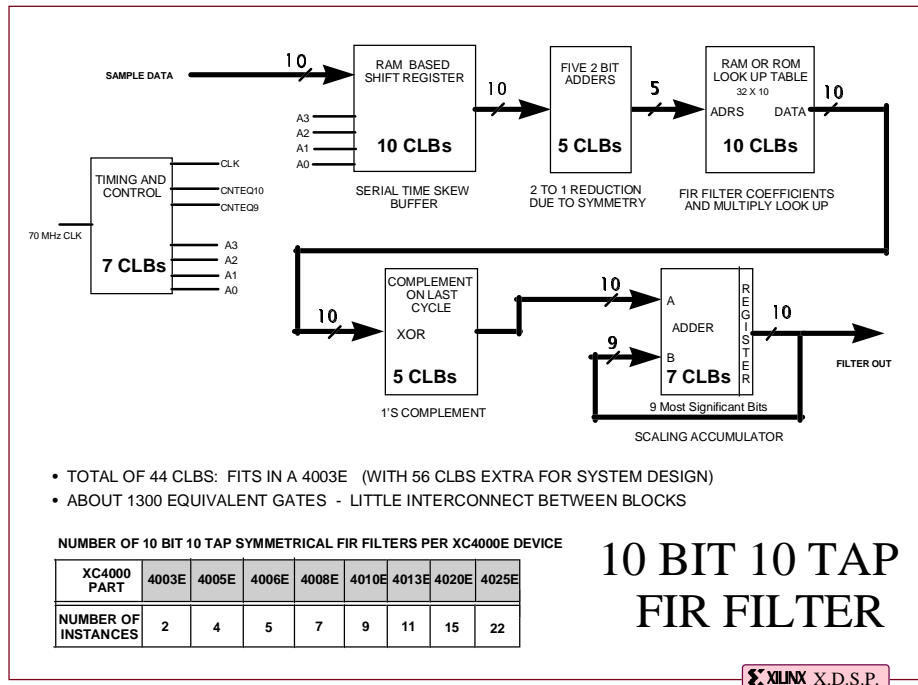
1's COMPLEMENTER



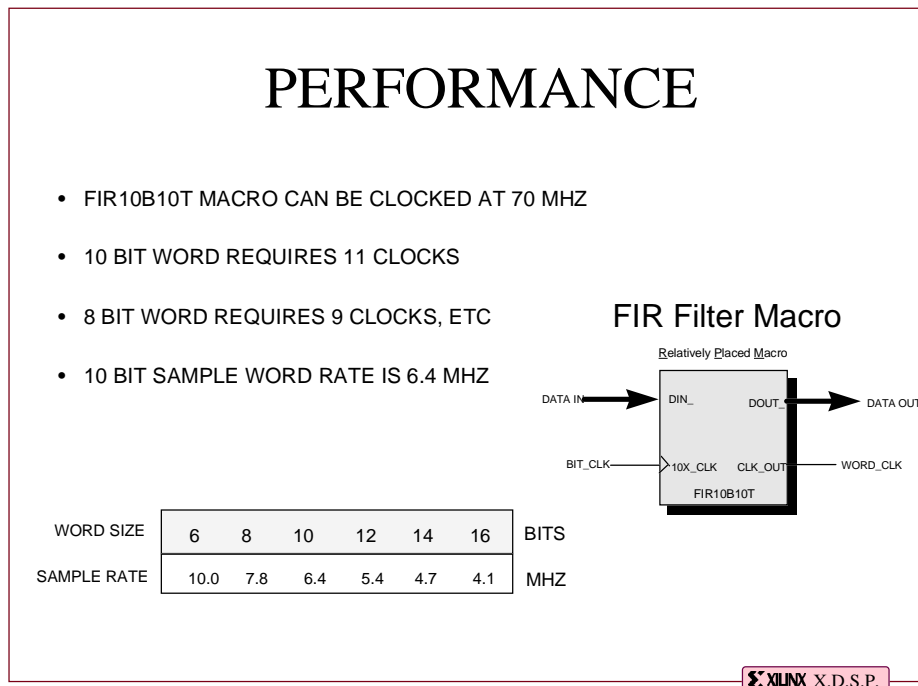
- INVERTS DATA ON LAST CYCLE
- 2 BITS PER CLB

Slide Number 22 9/2/96 20:03 XDSP.PPT

XILINX X.D.S.P.



Slide Number 25 9/2/96 20:04 XDSP.PPT



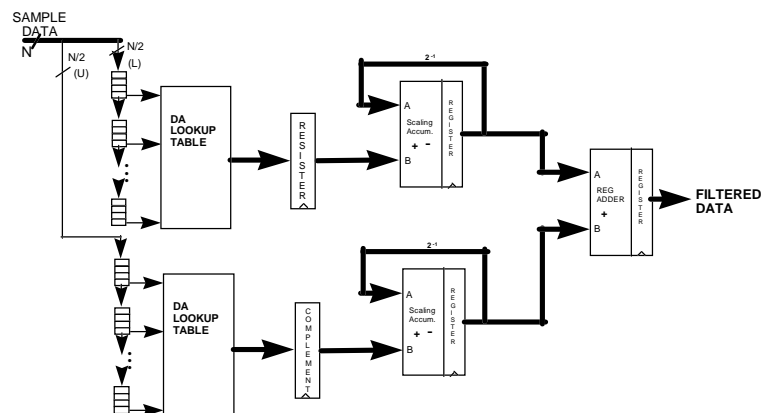
Slide Number 26 9/2/96 20:05 XDSP.PPT

Double-Rate DA FIR Filters

Slide Number 27 9/2/96 20:05 XDSP.PPT

XILINX X.D.S.P.

Higher Sample Rate D.A. FIR Filter



- Process 2 Bits per Clock
- # of Clocks = $(N/2) + 1$

Slide Number 28 9/2/96 20:05 XDSP.PPT

XILINX X.D.S.P.

Double Sample Rate D.A. FIR Filters

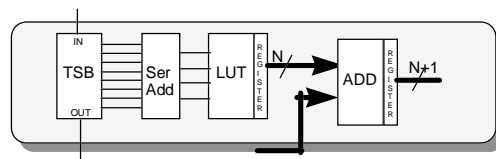
- Two Taps Requires 4 Input LUT without Symmetry
- Four Taps Requires 4 Level LUT with Symmetrical FIR
- Time Skew Buffer is Twice as many CLBs
- Twice the Data Word Sample Rate
- Both LUTs are the same

Slide Number 29 9/2/96 20:06 XDSP.PPT

XILINX X.D.S.P.

Designing Large Multi-TAP Filters

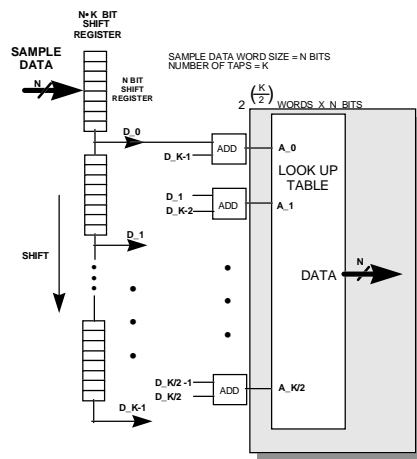
Xilinx 8-TAP FIR Filter *SLICE* Building Blocks



Slide Number 30 9/2/96 20:06 XDSP.PPT

XILINX X.D.S.P.

ISSUE: LUT Scales Exponentially

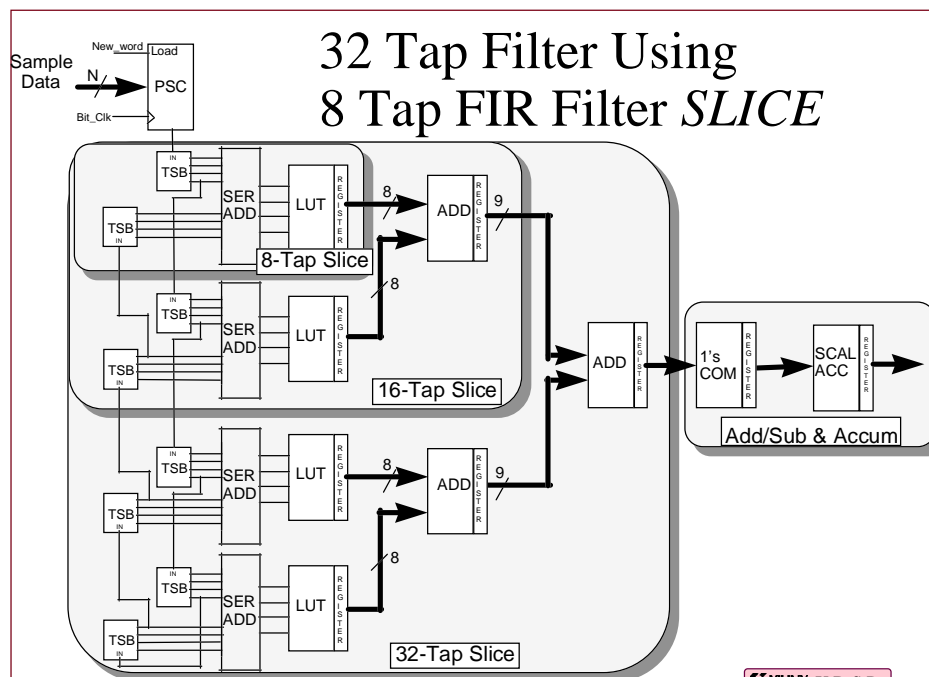


ROM LOOK UP TABLE SIZE

WORD LENGTH	6 TAP	8 TAP	10 TAP	12 TAP	14 TAP
16 BITS	8X16 8 CLB	16X16 8 CLB	32X16 16 CLB	64X16 40 CLB	128X16 80 CLB
14 BITS	16X14 7 CLB	16X14 7 CLB	32X14 14 CLB	64X14 35 CLB	128X14 70 CLB
12 BITS	16X12 6 CLB	16X12 6 CLB	32X12 12 CLB	64X12 30 CLB	128X12 60 CLB
10 BITS	16X10 5 CLB	16X10 5 CLB	32X10 10 CLB	64X10 25 CLB	128X10 50 CLB
8 BITS	16X8 4 CLB	16X8 4 CLB	32X8 8 CLB	64X8 20 CLB	128X8 40 CLB
6 BITS	16X6 3 CLB	16X6 3 CLB	32X6 6 CLB	64X6 15 CLB	128X6 30 CLB

Slide Number 31 9/2/96 20:06 XDSP.PPT

XILINX X.D.S.P.

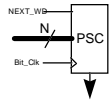


Slide Number 32 9/2/96 20:06 XDSP.PPT

XILINX X.D.S.P.

8 Tap FIR Filter *SLICE* Building Blocks

Parallel to Serial
Converter



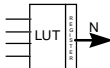
N/2 CLBs

Time Skew Buffer
(Quad)



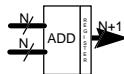
2 CLBs
(Up to 16
bit word)

Look Up Table



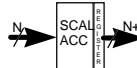
N/2 CLBs

N Bit ADDer



(N/2)+1 CLBs

N Bit SCAL
ACCUM



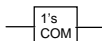
(N/2)+1 CLBs

Serial Adder



1 CLB

1's Complementer



1/2 CLB

Slide Number 33 9/2/96 20:07 XDSP.PPT

XILINX X.D.S.P.

8 Tap FIR Filter *SLICE*

APPROXIMATE NUMBER OF XC4000 CLBs

	6	8	10	12	14	16	18	20	22	24
8 TAPS	26	30	24	38	42	46	54	58	62	66
16 TAPS	45	51	57	63	69	75	93	99	105	111
32 TAPS	82	92	102	112	122	132	166	176	186	196
48 TAPS		139	154	169	184	199	250	265	280	295
56 TAPS		158	175	192	209	226	285	302	319	336
64 TAPS			190	208	226	244	310	328	346	364
96 TAPS			284	311	338	365	464	491	518	545
128 TAPS			363	397	431	465	595	629	663	697

Slide Number 34 9/2/96 20:07 XDSP.PPT

XILINX X.D.S.P.


8 Tap FIR Filter *SLICE*

4KE-3 PERFORMANCE

SAMPLE DATA WORD SIZE	6	8	10	12	14	16	18	20	22	24
MEGA SAMPLES PER SECOND	10.0	7.8	6.4	5.4	4.7	4.1	3.7	3.3	3.0	2.8
DOUBLE RATE PERFORMANCE	17.5	14.0	11.7	10.0	8.8	7.8	7.0	6.4	5.8	5.4

Sample Rate is Independent of the Number of Taps


Slide Number 35 9/2/96 20:07 XDSP.PPT

 XILINX X.D.S.P.

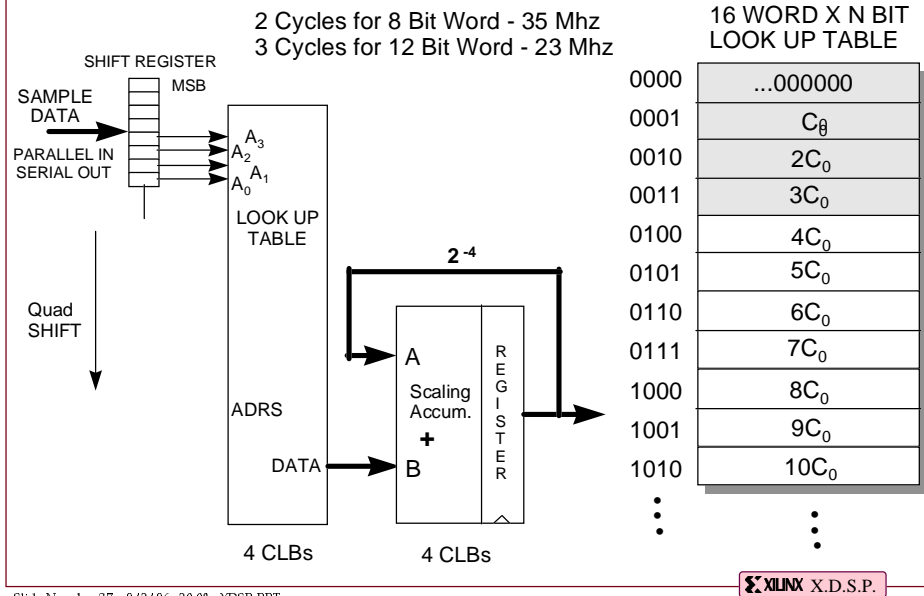
Very High Speed Sample Rates

Multiple Parallel Multipliers

Slide Number 36 9/2/96 20:08 XDSP.PPT

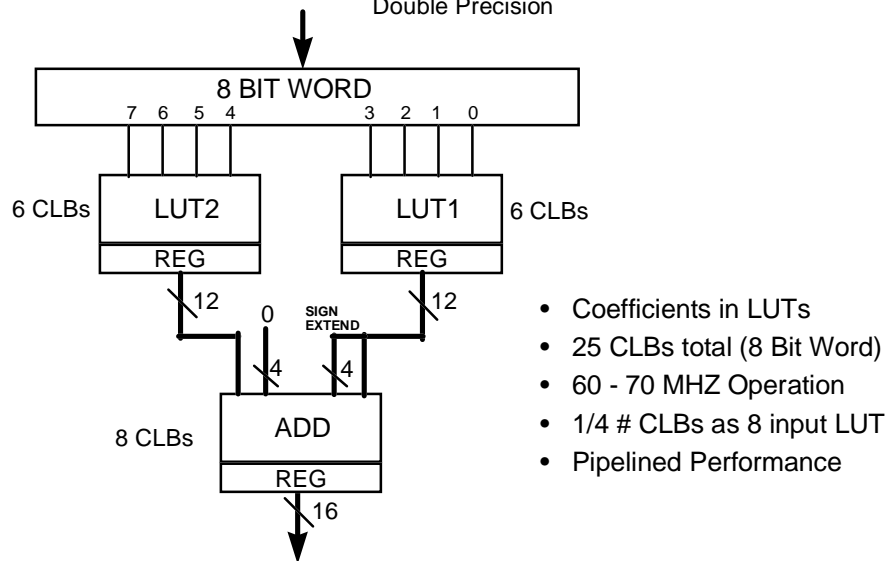
 XILINX X.D.S.P.

Multiply Variable Times Constant



Multiply Variable Times A Constant

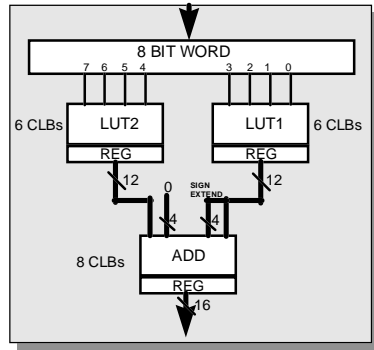
Double Precision



Slide Number 38 9/2/96 20:08 XDSP.PPT

XILINX X.D.S.P.

Multiply Variable times a Constant



$V_7 V_6 V_5 V_4 \quad 0000$ V1
 $0000 \quad V_3 V_2 V_1 V_0$ V0

$$\text{Variable} = V = V1 + V0$$

$$V \times C = (V1 \times C) + (V0 \times C)$$

ADRS	LUT2	LUT1
0	0000	0
1	0001	1 x Const
2	0010	2 x Const
3	0011	3 x Const
4	0100	4 x Const
5	0101	5 x Const
6	0110	6 x Const
7	0111	7 x Const
8	1000	-8 x Const
9	1001	-7 x Const
A	1010	-6 x Const
B	1011	-5 x Const
C	1100	-4 x Const
D	1101	-3 x Const
E	1110	-2 x Const
F	1111	-1 x Const

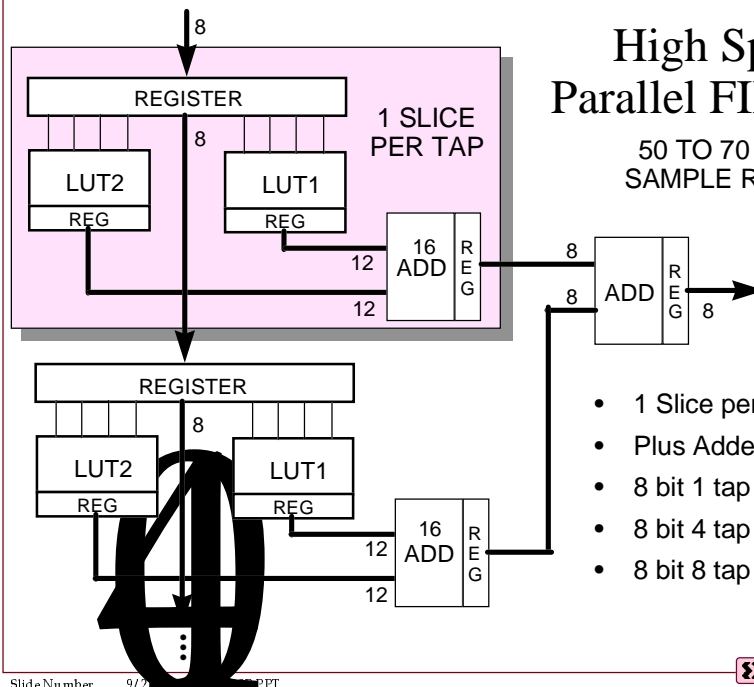
SIGN BIT ↑ Most Sig. 12 Bits Least Sig. 12 Bits

Slide Number 39 9/2/96 20:08 XDSP.PPT

XILINX X.D.S.P.

High Speed Parallel FIR Filter

50 TO 70 MHZ
SAMPLE RATES



- 1 Slice per Tap
- Plus Adder Tree
- 8 bit 1 tap = 25 CLBs
- 8 bit 4 tap = 115 CLBs
- 8 bit 8 tap = 240 CLBs

Slide Number 9/2/96 20:08 XDSP.PPT

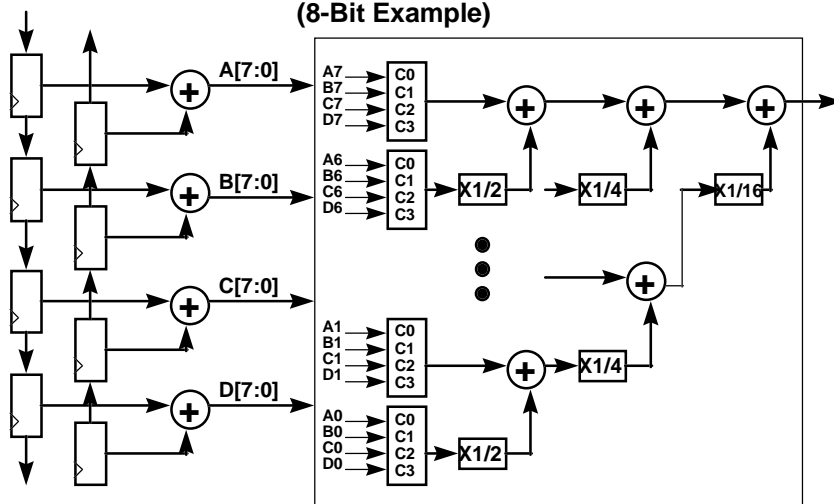
XILINX X.D.S.P.

Fully Parallel Distributed Arithmetic

Slide Number 41 9/2/96 20:10 XDSP.PPT

XILINX X.D.S.P.

8-Tap Slice (8-Bit Example)



Slide Number 42 9/2/96 20:10 XDSP.PPT

XILINX X.D.S.P.

(cont.)

- Supports sample rates of 50-70 MSPS
- Data and coefficient size are independent of each other
- 8-Bit Data, 8-Bit Coeff requires 122 CLBs per 8-Tap Slice
- 16-Tap, 8-Bit filter requires 250 CLBs
- 32-Tap, 8-Bit filter requires 508 CLBs




CLB Count for 8-Tap PDA Slice

Data Size

4	46	53	60	67	74			
6	73	85	97	109	121	133		
8	92	107	122	137	152	167	182	
10		145	166	187	208	229	250	
12			191	215	239	263	287	
14			222	250	278	306	334	
16				278	309	340	371	

APPROXIMATE NUMBER OF XC4000 CLBs



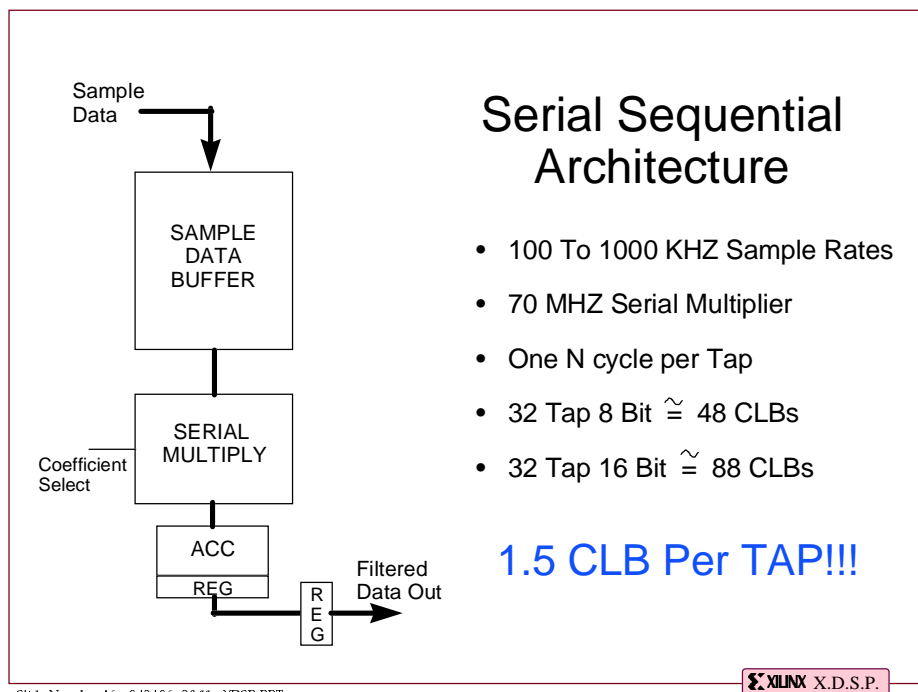
Lower Sample Rate Applications:

Efficient CLB Counts
Large Number of TAPs
Moderate Sample Rates
Non Symmetrical FIR OK

Serial Sequential Architecture

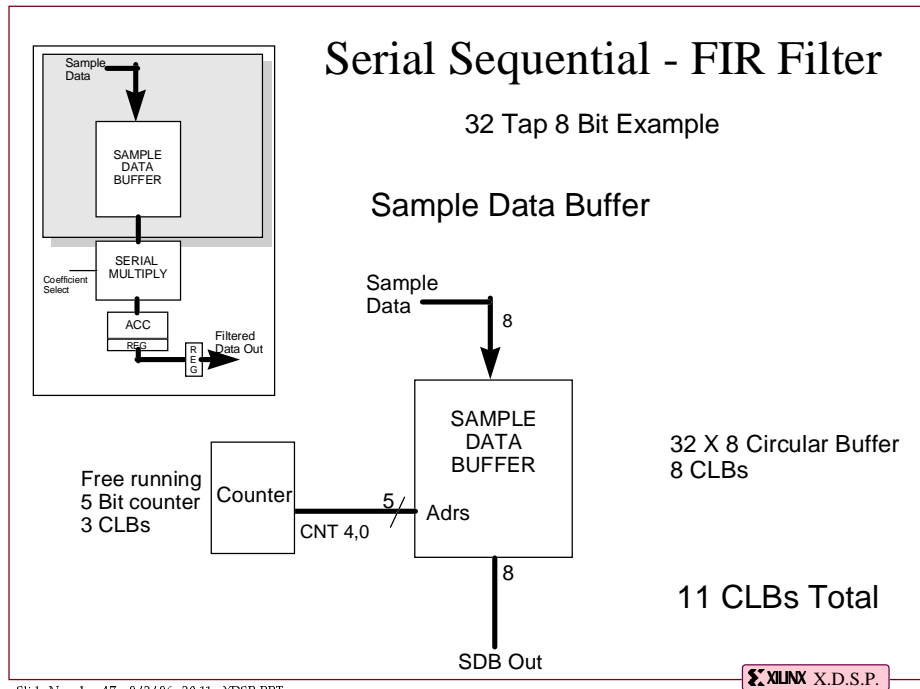
Slide Number 45 9/2/96 20:10 XDSP.PPT

XILINX X.D.S.P.

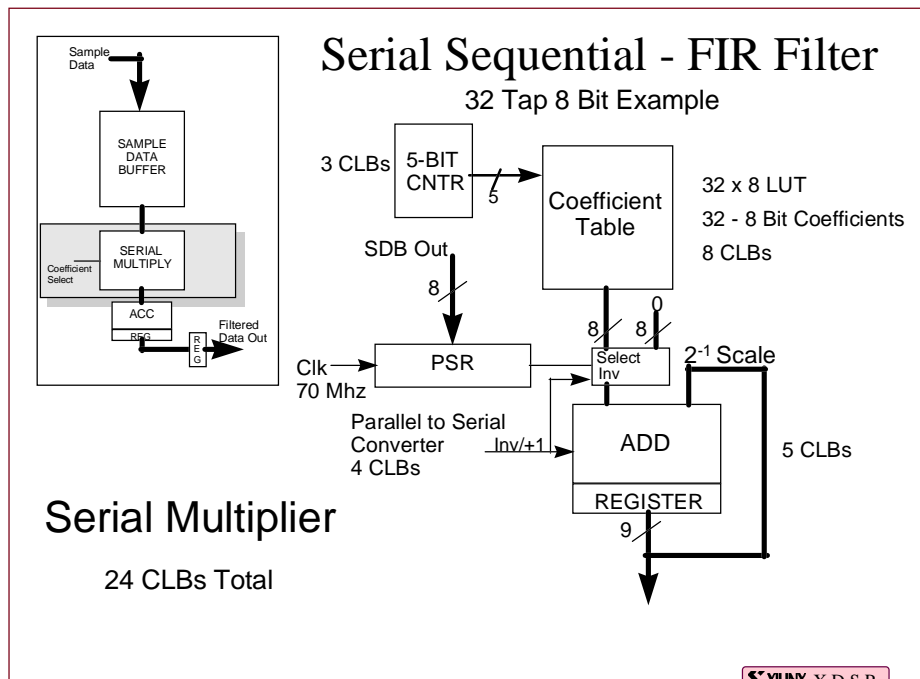


Slide Number 46 9/2/96 20:11 XDSP.PPT

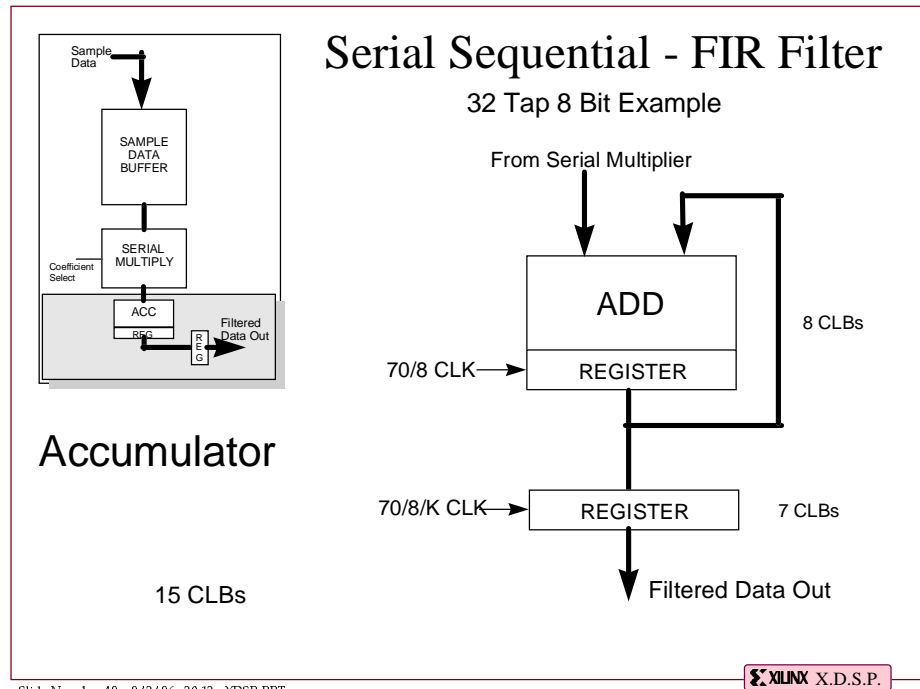
XILINX X.D.S.P.



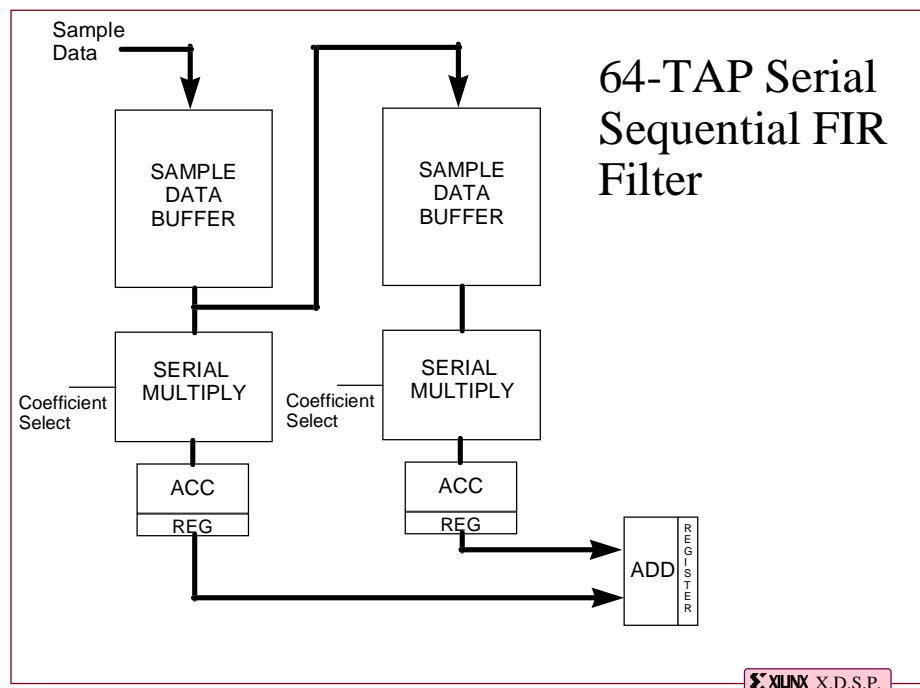
Slide Number 47 9/2/96 20:11 XDSP.PPT



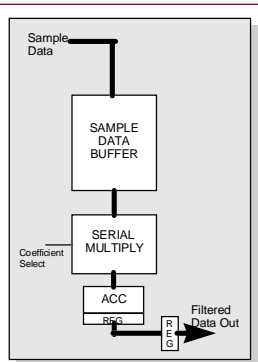
Slide Number 48 9/2/96 20:11 XDSP.PPT



Slide Number 49 9/2/96 20:12 XDSP.PPT



Slide Number 50 9/2/96 20:12 XDSP.PPT



Serial Sequential - FIR Filter

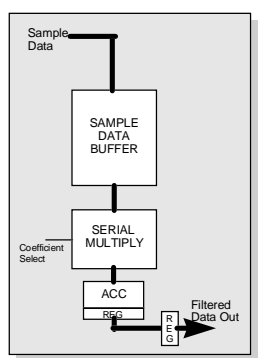
Number CLBs vs. Taps / Word Size

	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
8 Tap	36	43	50	57	64
16 Tap	36	43	50	57	64
32 Tap	44	53	62	71	80
48 Tap	62	77	92	107	122
64 Tap	70	85	100	115	130
80 Tap	97	115	133	151	169
96 Tap	97	115	133	151	169
128 Tap	112	137	162	187	212

- 4003E = 100 CLBs
- 4005E = 196 CLBs
- 4013E = 576 CLBs
- 4025E = 1024 CLBs

Slide Number 51 9/2/96 20:12 XDSP.PPT

XILINX X.D.S.P.



Serial Sequential - FIR Filter

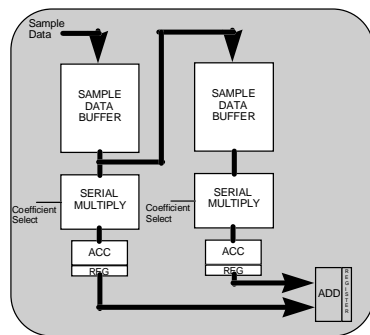
Maximum Sample Rate / Word Size

TAPS	8 Bit	10 Bit	16 Bit
8 Tap	1.1Mhz	875Khz	547Khz
16 Tap	547Khz	438Khz	273Khz
32 Tap	273Khz	219Khz	137Khz
48 Tap	182Khz	104Khz	91Khz
64 Tap	137Khz	109Khz	68Khz
80 Tap	109Khz	88Khz	55Khz
96 Tap	91Khz	73Khz	46Khz
128 Tap	68Khz	55Khz	34Khz

- Serial Mult. Limitations
- Can Use Multiple 16 Tap Building Blocks
- 8X Faster at 128 Taps

Slide Number 52 9/2/96 20:12 XDSP.PPT

XILINX X.D.S.P.



Serial Sequential 16 Tap Slice FIR Filter

Maximum Sample Rate / Word Size

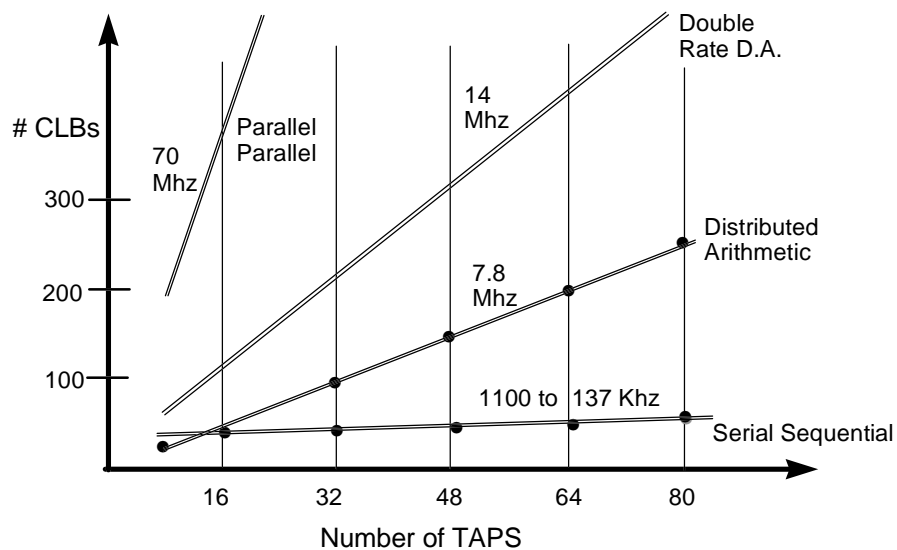
TAPS	8 Bit	10 Bit	16 Bit
16 Tap	547Khz	438Khz	273Khz
32 Tap	547Khz	438Khz	273Khz
48 Tap	•	•	•
64 Tap	•	•	•
80 Tap	•	•	•
96 Tap	•	•	•
128 Tap	•	•	•

- 16-Tap Slice Used
- 32-Tap Slice Uses Less CLBs

Slide Number 53 9/2/96 20:13 XDSP.PPT

XILINX X.D.S.P.

8 Bit Word FIR Filter Structures



Slide Number 54 9/2/96 20:13 XDSP.PPT

XILINX X.D.S.P.

FIR Filter Implementation Options

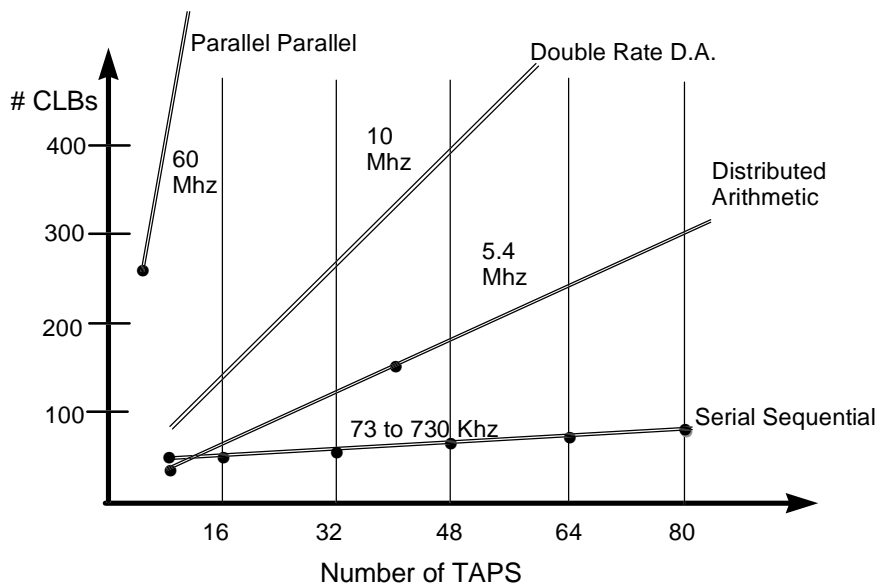
8 Bit Word Example

	Serial Sequential	Distributed Arithmetic	Parallel Parallel
8 Taps	36 CLBs 1100 Khz	30 CLBs 7.8 Mhz	240 CLBs 70 Mhz
16 Taps	36 CLBs 547 Khz	51 CLBs 7.8 Mhz	500 CLBs 70 Mhz
32 Taps	44 CLBs 273 Khz	92 CLBs 7.8 Mhz	
48 Taps	62 CLBs 182 Khz	139 CLBs 7.8 Mhz	
64 Taps	70 CLBs 137 Khz	158 CLBs 7.8 Mhz	

Slide Number 55 9/2/96 20:13 XDSP.PPT

XILINX X.D.S.P.

12 Bit Word FIR Filter Structures



Slide Number 56 9/2/96 20:13 XDSP.PPT


XILINX X.D.S.P.

FIR Filter Implementation Options

12 Bit Word Example


	Serial Sequential	Distributed Arithmetic	Parallel Parallel
8 Taps	50 CLBs 729 Khz	38 CLBs 5.4 Mhz	378 CLBs 60 Mhz
16 Taps	50 CLBs 365 Khz	63 CLBs 5.4 Mhz	762 CLBs 60 Mhz
32 Taps	62 CLBs 182 Khz	112 CLBs 5.4 Mhz	
48 Taps	92 CLBs 122 Khz	169 CLBs 5.4 Mhz	
64 Taps	100 CLBs 91 Khz	208 CLBs 5.4 Mhz	

Slide Number 57 9/2/96 20:13 XDSP.PPT

 XILINX X.D.S.P.

Decimating FIR Filters

Slide Number 58 9/2/96 20:13 XDSP.PPT

 XILINX X.D.S.P.

Decimate 4:1 FIR Filter

- Example: 32-tap decimate 4:1 FIR
- Discard 3 out of 4 output results
- Equivalent to sliding each Sample by 4 taps/clk
- Filter can be decomposed into 4 eight-tap subfilters
- Architect the filter such that no resources are used to calculate discarded outputs
- Increases FIR filter input Sample rate by 4X
- DALUT are composed of every 4th coeff
- Symmetrical filters OK

Slide Number 59 9/2/96 20:13 XDSP.PPT

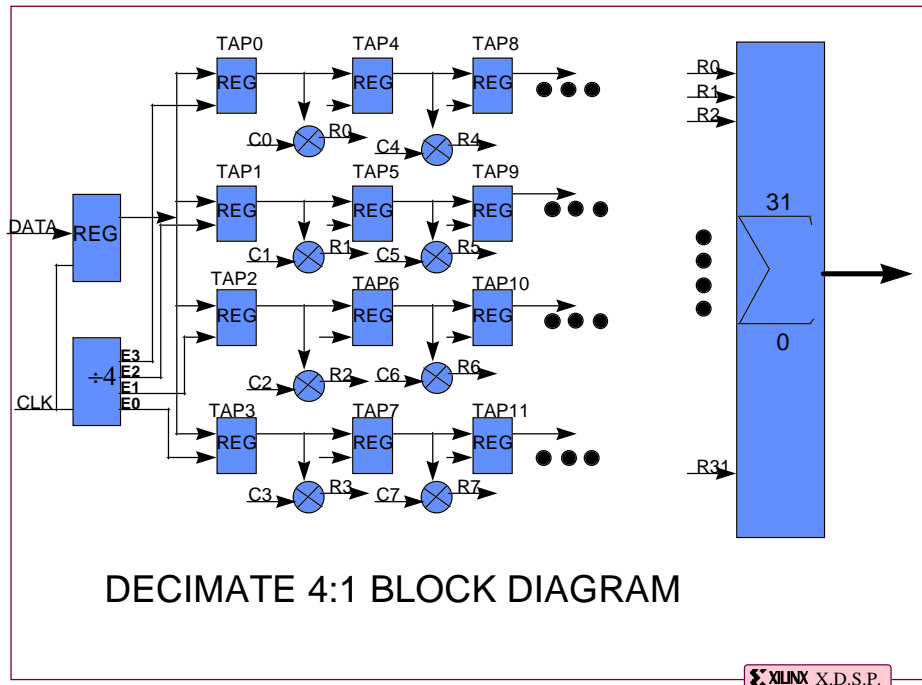
XILINX X.D.S.P.

16-Tap Down-Rate 4:1 Output Sequence

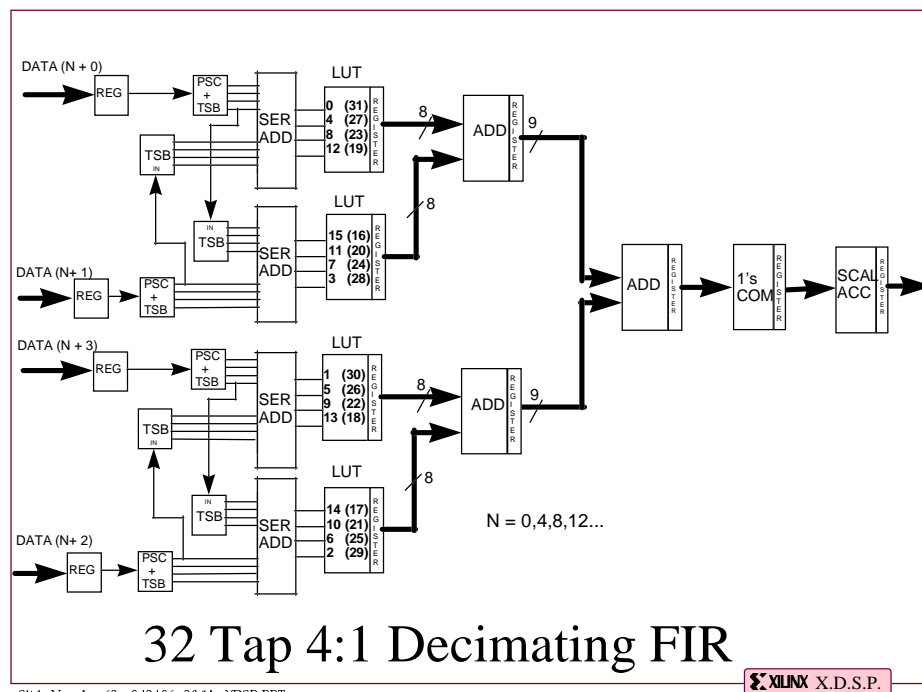
$$\begin{aligned}
 \text{Output (n)} &= D(n)*C0 + D(n-1)*C1 + D(n-2)*C2 + D(n-3)*C3 + \\
 &\quad D(n-4)*C4 + D(n-5)*C5 + D(n-6)*C6 + D(n-7)*C7 + \\
 &\quad D(n-8)*C8 + D(n-9)*C9 + D(n-10)*C10 + D(n-11)*C11 + \\
 &\quad D(n-12)*C12 + D(n-13)*C13 + D(n-14)*C14 + D(n-15)*C15 \\
 \text{Output (n+1)} &= D(n+1)*C0 + D(n)*C1 + D(n-1)*C2 + D(n-2)*C3 + \\
 &\quad D(n-3)*C4 + D(n-4)*C5 + D(n-5)*C6 + D(n-6)*C7 + \\
 &\quad D(n-7)*C8 + D(n-8)*C9 + D(n-9)*C10 + D(n-10)*C11 + \\
 &\quad D(n-11)*C12 + D(n-12)*C13 + D(n-13)*C14 + D(n-14)*C15 \\
 \text{Output (n+2)} &= D(n+2)*C0 + D(n+1)*C1 + D(n)*C2 + D(n-1)*C3 + \\
 &\quad D(n-2)*C4 + D(n-3)*C5 + D(n-4)*C6 + D(n-5)*C7 + \\
 &\quad D(n-6)*C8 + D(n-7)*C9 + D(n-8)*C10 + D(n-9)*C11 + \\
 &\quad D(n-10)*C12 + D(n-11)*C13 + D(n-12)*C14 + D(n-13)*C15 \\
 \text{Output (n+3)} &= D(n+3)*C0 + D(n+2)*C1 + D(n+1)*C2 + D(n)*C3 + \\
 &\quad D(n-1)*C4 + D(n-2)*C5 + D(n-3)*C6 + D(n-4)*C7 + \\
 &\quad D(n-5)*C8 + D(n-6)*C9 + D(n-7)*C10 + D(n-8)*C11 + \\
 &\quad D(n-9)*C12 + D(n-10)*C13 + D(n-11)*C14 + D(n-12)*C15 \\
 \text{Output (n+4)} &= D(n+4)*C0 + D(n+3)*C1 + D(n+2)*C2 + D(n+1)*C3 + \\
 &\quad D(n)*C4 + D(n-1)*C5 + D(n-2)*C6 + D(n-3)*C7 + \\
 &\quad D(n-4)*C8 + D(n-5)*C9 + D(n-6)*C10 + D(n-7)*C11 + \\
 &\quad D(n-8)*C12 + D(n-9)*C13 + D(n-10)*C14 + D(n-11)*C15
 \end{aligned}$$

Slide Number 60 9/2/96 20:14 XDSP.PPT

XILINX X.D.S.P.




Slide Number 61 9/2/96 20:14 XDSP.PPT



Slide Number 62 9/2/96 20:14 XDSP.PPT

Interpolating FIR Filters


Slide Number 63 9/2/96 20:14 XDSP.PPT

 XILINX X.D.S.P.

Interpolation 1:2 FIR Filter

- Example: 16-tap up-rate by 2 FIR
- Insert zeros between every other data sample
- Filter data output rate equals 2x input data rate
- Architect filter such that no resources are used to calculate zero * tap coeff
- 16-tap filter can be decomposed into two 8-tap parallel filters
- DALUT are composed of every other coeff

Slide Number 64 9/2/96 20:14 XDSP.PPT

 XILINX X.D.S.P.

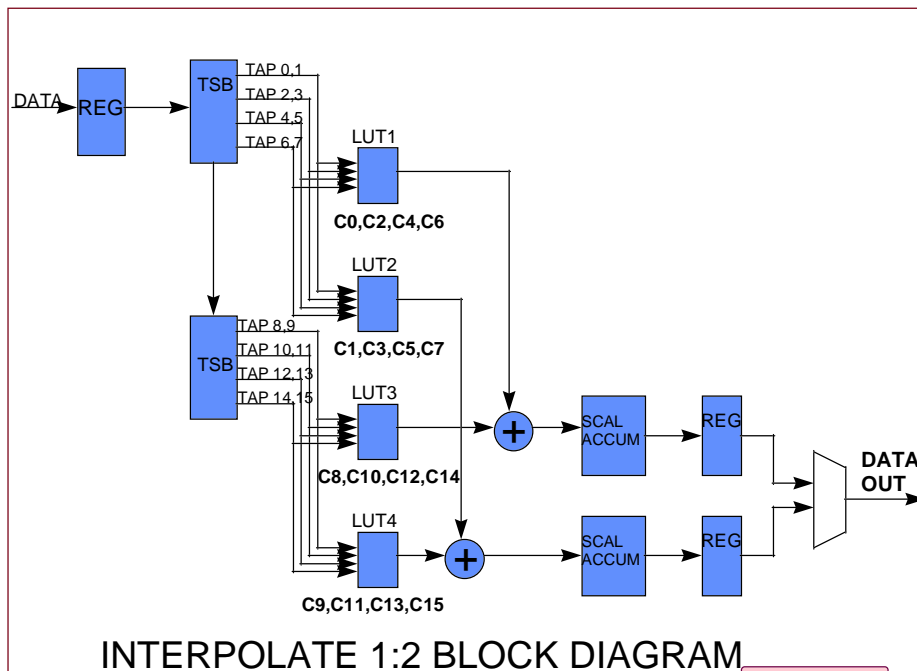
16-Tap 1:2 Interpolation Output Tree

$$\begin{aligned} \text{Output (n)} = & D(n)*C0 + 0*C1 + D(n-1)*C2 + 0*C3 + \\ & D(n-2)*C4 + 0*C5 + D(n-3)*C6 + 0*C7 + \\ & D(n-4)*C8 + 0*C9 + D(n-5)*C10 + 0*C11 + \\ & D(n-6)*C12 + 0*C13 + D(n-7)*C14 + 0*C15 \end{aligned}$$

$$\begin{aligned} \text{Output (n+1)} = & 0*C0 + D(n)*C1 + 0*C2 + D(n-1)*C3 + \\ & 0*C4 + D(n-2)*C5 + 0*C6 + D(n-3)*C7 + \\ & 0*C8 + D(n-4)*C9 + 0*C10 + D(n-5)*C11 + \\ & 0*C12 + D(n-6)*C13 + 0*C14 + D(n-7)*C15 \end{aligned}$$

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XILINX X.D.S.P.



Slide Number 66 9/2/96 20:15 XDSP.PPT

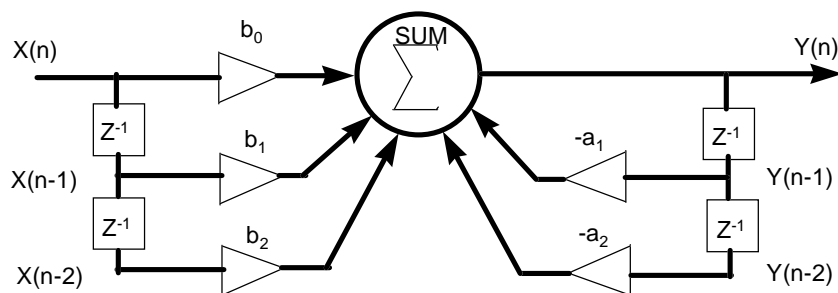
XILINX X.D.S.P.

IIR Filters

Slide Number 67 9/2/96 20:15 XDSP.PPT

XILINX X.D.S.P.

IIR Filter - Biquad (Direct Form)

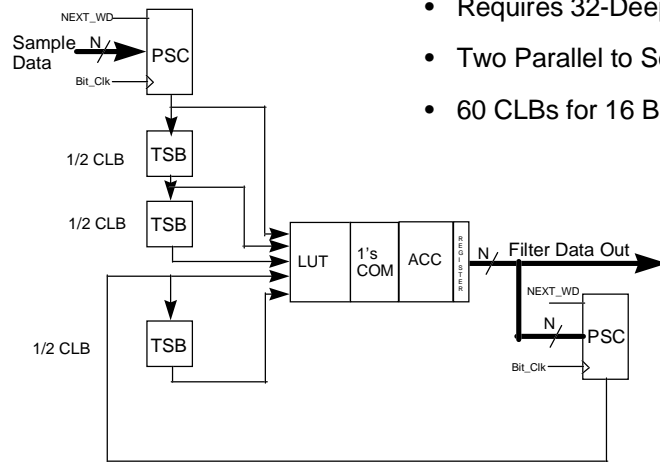


(Lowest Quantization Noise)

Slide Number 68 9/2/96 20:15 XDSP.PPT

XILINX X.D.S.P.

IIR Filter - Biquad Implementation

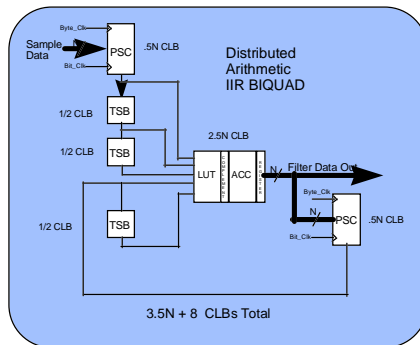


- Requires 32-Deep LUT
- Two Parallel to Serial Converters
- 60 CLBs for 16 Bit Word

Slide Number 69 9/2/96 20:15 XDSP.PPT

XILINX X.D.S.P.

IIR Filter - Biquad Implementation



- $3.5N + 8$ CLBs (Up to 16 Bits)
- Sample rate = $50 / N$ MHZ
- Common Control Logic

Word Size	# CLBs	Word Sample Rate
12 Bits	50 CLBs	4.1 MHZ
14 Bits	55 CLBs	3.6 MHZ
16 Bits	60 CLBs	3.1 MHZ
18 Bits	72 CLBs	2.8 MHZ
20 Bits	77 CLBs	2.5 MHZ
22 Bits	82 CLBs	2.2 MHZ
24 Bits	87 CLBs	2.1 MHZ

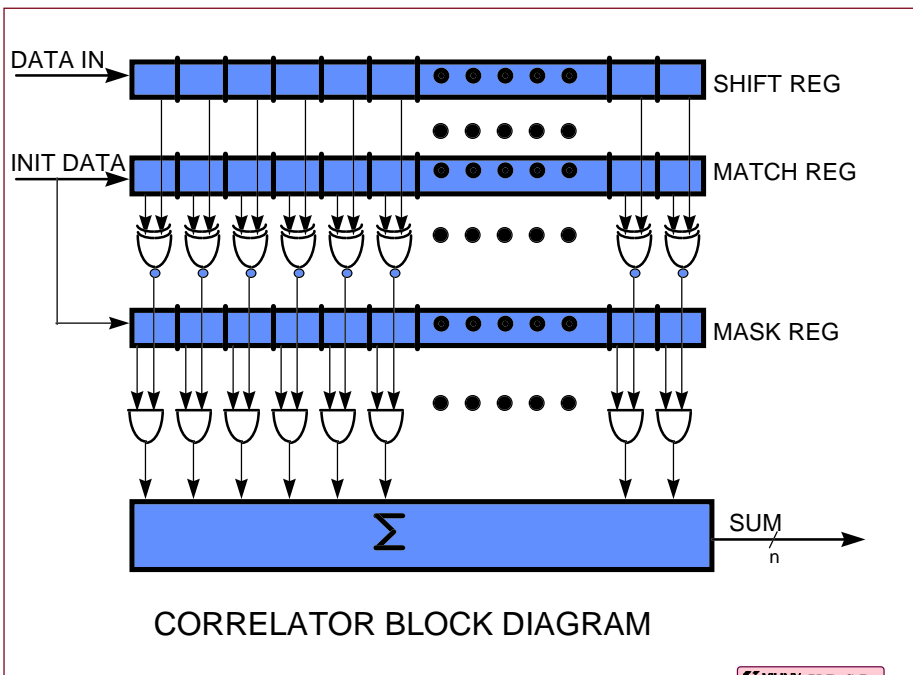
Slide Number 70 9/2/96 20:15 XDSP.PPT

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CORRELATORS

Slide Number 71 9/2/96 20:15 XDSP.PPT

XILINX X.D.S.P.



Slide Number 72 9/2/96 20:15 XDSP.PPT

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USING LUTs FOR CORRELATORS

- Any n-stage correlator can be decomposed into (n/4) 4-stage correlators
- Luts contain all potential outputs for each 4 stage correlation
- Example: correlation pattern = 1011
 Store 4h at address Bh in lut (all 4 bits match)
 Store 3h at addresses 3,F,9,A in LUT (1 bit error)
- Bit rates can exceed 120 MHz (3100A)

Slide Number 73 9/2/96 20:16 XDSP.PPT

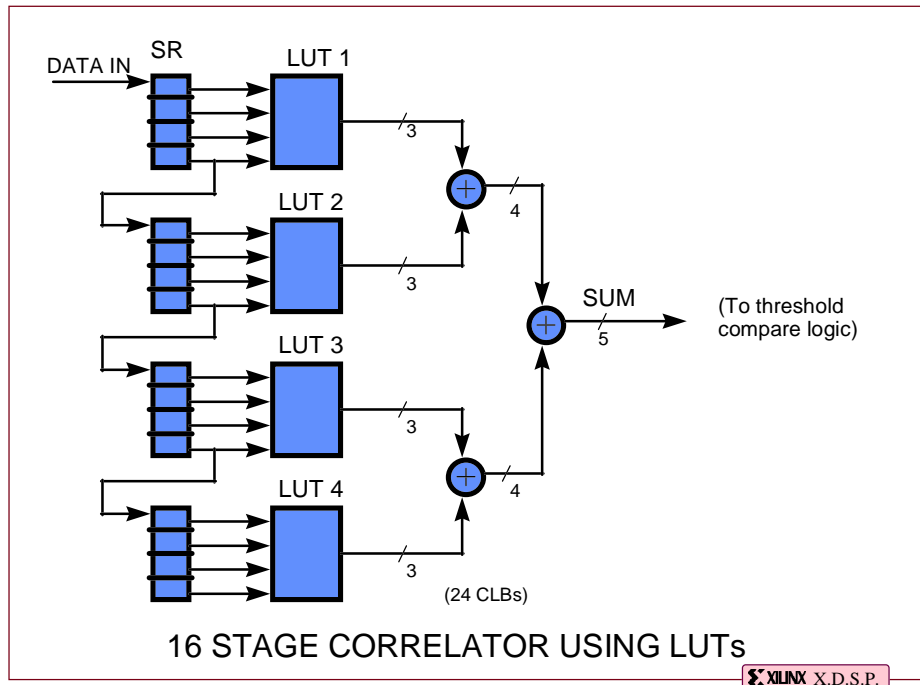
XILINX X.D.S.P.

CORRELATOR LUT EXAMPLE

LUT Contents	
Address	Data
Input search pattern = 1101	0000 001 (1 BIT MATCH)
	0001 010 (2 BIT MATCH)
	0010 000 (0 BIT MATCH)
	0011 001 (1 BIT MATCH)
	0100 010 (2 BIT MATCH)
	0101 011 (3 BIT MATCH)
	0110 001 (1 BIT MATCH)
	0111 010 (2 BIT MATCH)
	1000 010 (2 BIT MATCH)
	1001 011 (3 BIT MATCH)
	1010 001 (1 BIT MATCH)
	1011 010 (2 BIT MATCH)
	1100 011 (3 BIT MATCH)
	1101 100 (4 BIT MATCH)
	1110 010 (2 BIT MATCH)
	1111 011 (3 BIT MATCH)

Slide Number 74 9/2/96 20:16 XDSP.PPT

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XILINX DSP CASE STUDIES

Slide Number 76 9/2/96 20:16 XDSP.PPT

XILINX X.D.S.P.

SATELLITE MODEM CASE STUDY

■ PRODUCT: Satellite modem

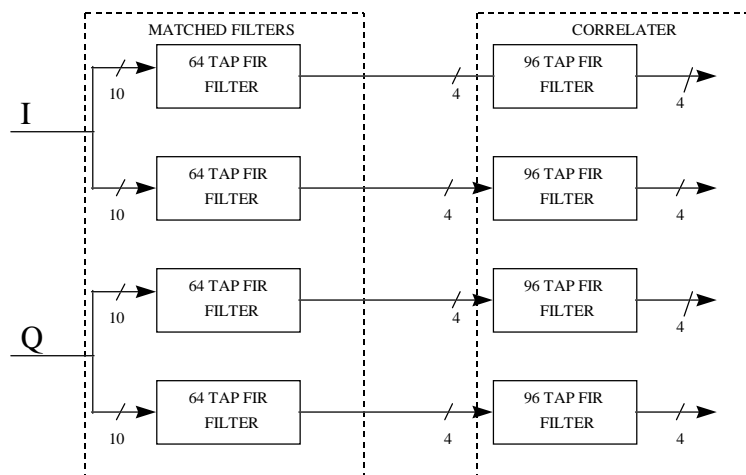
■ REQUIREMENTS:

- (2) decimating 32 TAP FIR filters
- (4) 64 tap FIR filter 10 bit data and coefficient
- (4) 96 tap FIR filter 4 bit data and coefficient
- cost reduction path
- board space reduction

Slide Number 77 9/2/96 20:16 XDSP.PPT

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SATELLITE MODEM BLOCK DIAGRAM



Slide Number 78 9/2/96 20:16 XDSP.PPT

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SATELLITE MODEM CASE STUDY


■ QUESTION: samples per second

- maximum data rate is 64 kbps - four times sampling = 256KSPS
- What potential solutions can we use?
 - » single rate DA FIR
 - » serial sequential
 - » What are the issues with either of these solutions?
 - » performance?
 - » design density?

■ QUESTION: Are the filters symmetrical?

- 64 tap FIR for the matched filters ARE
- 94 tap FIR for the correlators are NOT
 - » What does this do to using the standard XDSP single rate DA FIR?

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 X.D.S.P.

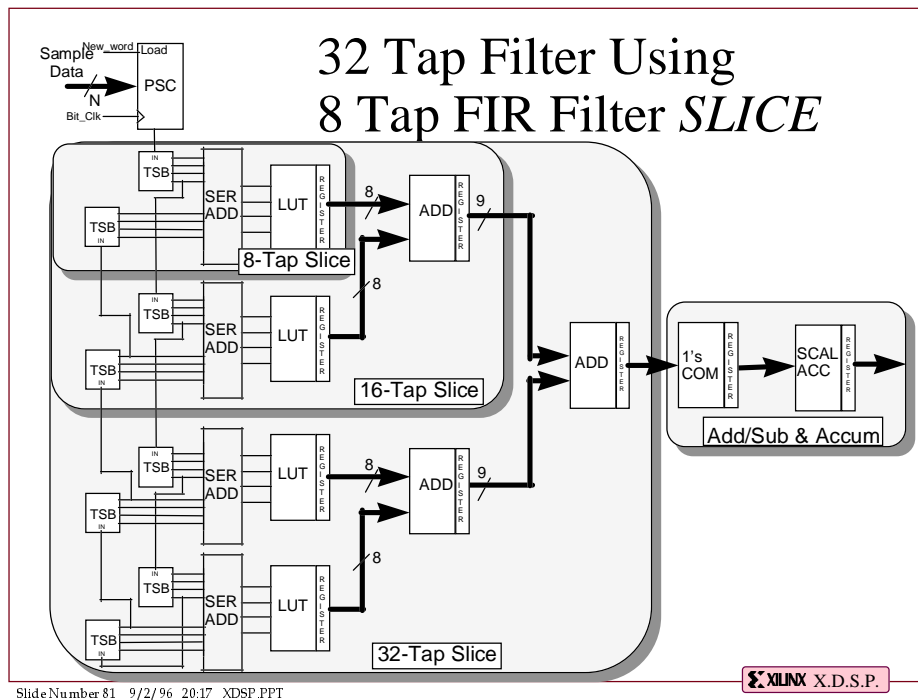
SATELLITE MODEM CASE STUDY

■ QUESTION: What are the data and coefficient sizes and anything 'special' about the coefficients?

- 64 tap FIR 10 bit data, 10 bit coefficients
 - » coefficients are smaller for the outer taps and grow as they move the center tap.
 - » taps 0 to 8 and 56 to 63 have 4 bit coefficients
 - » taps 9 to 16 and 49 to 55 have 5 bit coefficients, etc.
 - » there are four filters BUT the filter PAIRS are identical
- 96 tap FIR 4 bit data and coefficients
 - » the two pairs of filters are identical; two sets of coefficients

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 X.D.S.P.



8 Tap FIR Filter *SLICE*


APPROXIMATE NUMBER OF XC4000 CLBs

8 TAPS	26	30	24	38	42	46	54	58	62	66
16 TAPS	45	51	57	63	69	75	93	99	105	111
32 TAPS	82	92	102	112	122	132	166	176	186	196
48 TAPS		139	154	169	184	199	250	265	280	295
56 TAPS		158	175	192	209	226	285	302	319	336
64 TAPS			190	208	226	244	310	328	346	364
96 TAPS			284	311	338	365	464	491	518	545
128 TAPS			363	397	431	465	595	629	663	697

6 8 10 12 14 16 18 20 22 24

SAMPLE DATA WORD SIZE (N)

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 XILINX X.D.S.P.

8 TAP FIR FILTER *SLICE*

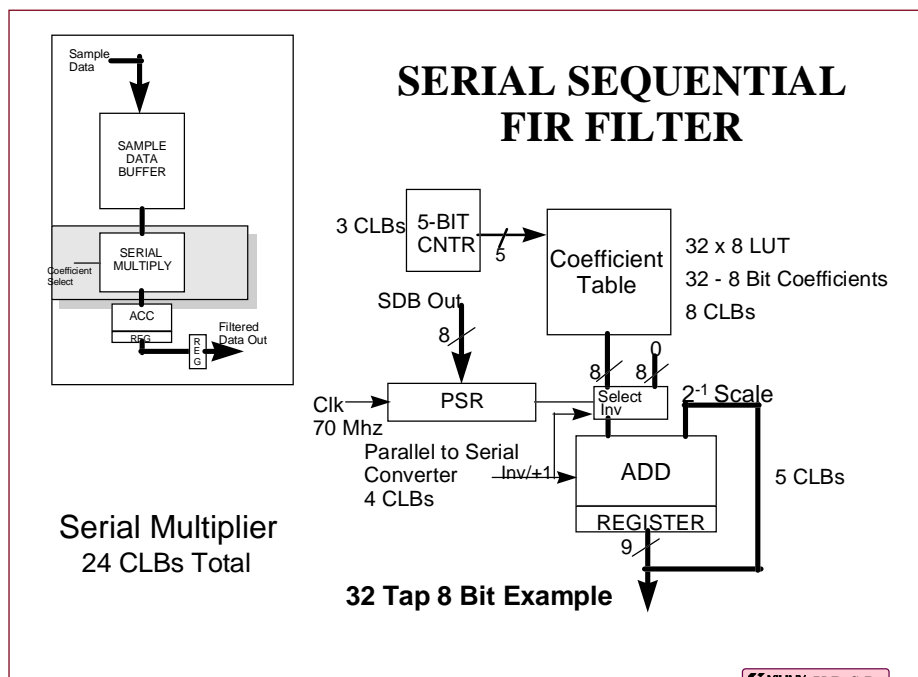
XC4000E-3 PERFORMANCE

SAMPLE DATA WORD SIZE	6	8	10	12	14	16	18	20	22	24
MEGA SAMPLES PER SECOND	10	7.8	6.4	5.4	4.7	4.1	3.7	3.3	3.0	2.8
DOUBLE RATE PERFORMANCE	17.5	14	11.7	10	8.8	7.8	7	6.4	5.8	5.4

SAMPLE RATE IS INDEPENDENT
OF THE NUMBER OF TAPS

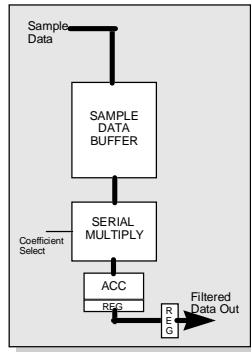
Slide Number 83 9/2/96 20:17 XDSP.PPT

XILINX X.D.S.P.



Slide Number 84 9/2/96 20:17 XDSP.PPT

XILINX X.D.S.P.



SERIAL SEQUENTIAL FIR FILTER

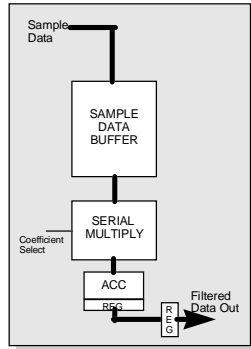
Number CLBs vs. Taps / Word Size

	8 Bit	10 Bit	12 Bit	14 Bit	16 Bit
8 Tap	36	43	50	57	64
16 Tap	36	43	50	57	64
32 Tap	44	53	62	71	80
48 Tap	62	77	92	107	122
64 Tap	70	85	100	115	130
80 Tap	97	115	133	151	169
96 Tap	97	115	133	151	169
128 Tap	112	137	162	187	212

- 4002 = 64 CLBs
- 4005 = 196 CLBs
- 4013 = 576 CLBs
- 4025 = 1024 CLBs

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XILINX X.D.S.P.



SERIAL SEQUENTIAL FIR FILTER

Maximum Sample Rate / Word Size

TAPS	8 Bit	10 Bit	16 Bit
8 Tap	781Khz	625Khz	390Khz
16 Tap	390Khz	312Khz	195Khz
32 Tap	195Khz	156Khz	97Khz
48 Tap	130Khz	104Khz	65Khz
64 Tap	97Khz	78Khz	48Khz
80 Tap	78Khz	62Khz	39Khz
96 Tap	65Khz	52Khz	32Khz
128 Tap	48Khz	39Khz	24Khz

- Serial Mult. Limitations
- Can Use Multiple 16 Tap Building Blocks
- 8X Faster at 128 Taps

Slide Number 86 9/2/96 20:18 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - SATELLITE MODEM

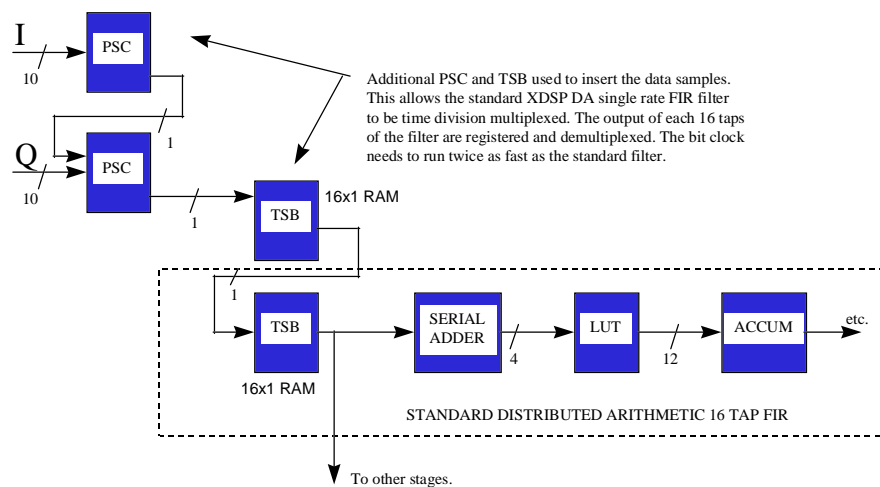
■ SOLUTIONS:

- 64 tap FIR filters have 2 sets of coefficients and two sets of data and are symmetrical
 - Can take advantage of common coefficients and time multiplex the DA FIR filter
 - This effectively reduces the device resources needed by 80% for these filters
- 96 tap FIR filters have 2 sets of coefficients and two sets of data and are NOT symmetrical
 - can take advantage of the coefficients being the same

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XILINX X.D.S.P.

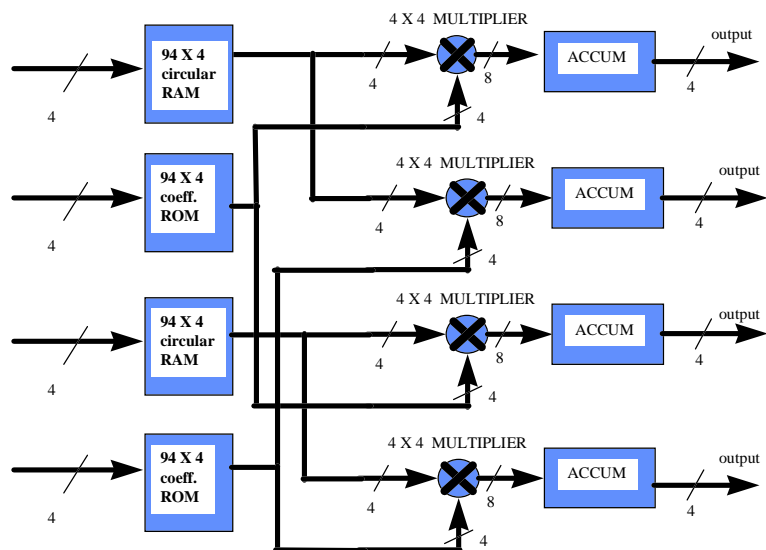
CASE STUDY - SATELLITE MODEM



Slide Number 88 9/2/96 20:18 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - SATELLITE MODEM



Slide Number 89 9/2/96 20:18 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION

■ PRODUCT: video input bar code reader

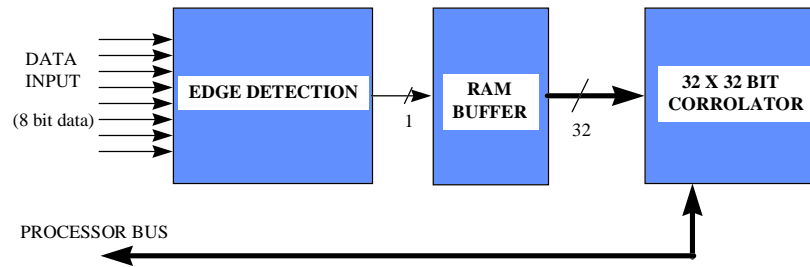
■ REQUIREMENTS:

- real-time video data processing : 50 MSPS, 8 bit data
- 8 X 8 edge detector (very common image processing operation)
- 32 X 32 bit correlator (very common image processing operation)
- cost reduction
- must maintain performance

Slide Number 90 9/2/96 20:18 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION

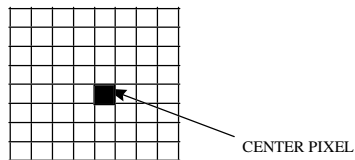


Slide Number 91 9/2/96 20:18 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION

8 x 8 PIXEL IMAGE



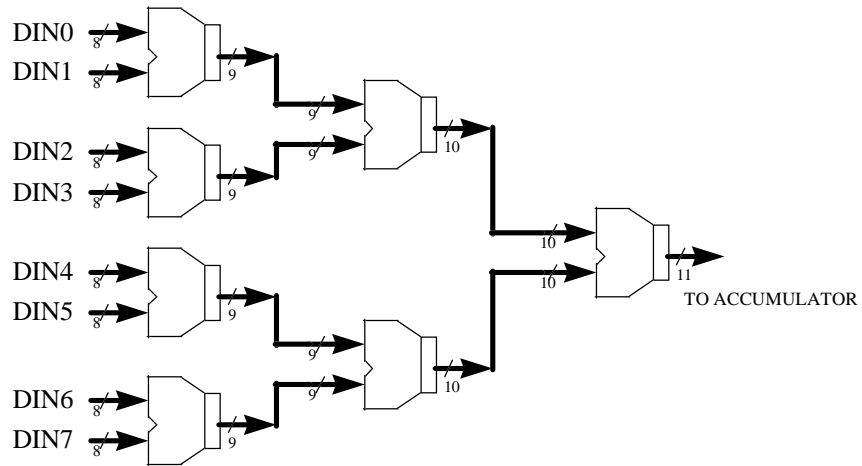
Edge detection is done using a filter operation in two dimensions. All pixel values are added together and then averaged. This value is compared to the center pixel value OR a threshold value and output value is produced. The output can be a saturation value or the original data value.

This design requires 63 adds, divide by 64 and compare each clock cycle; ever 20 nsec. (Piece of cake in a 5206-5).

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XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION

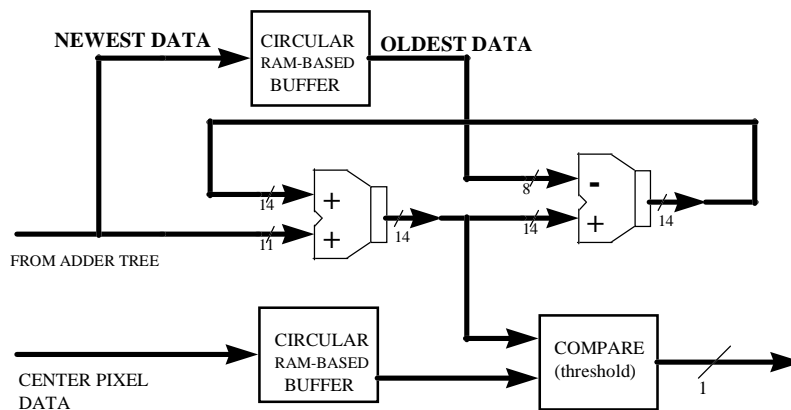


NOTE: DIN4 is the center pixel incoming data.

Slide Number 93 9/2/96 20:19 XDSP.PPT

XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION



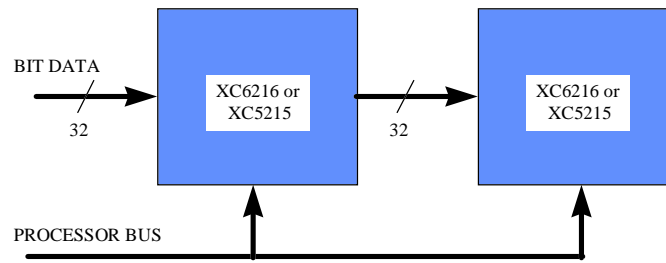
This fits into a XC4005E or XC5206 (using registers) and will run at 50 MSPS!

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XILINX X.D.S.P.

CASE STUDY - EDGE DETECTION

CORRELATOR




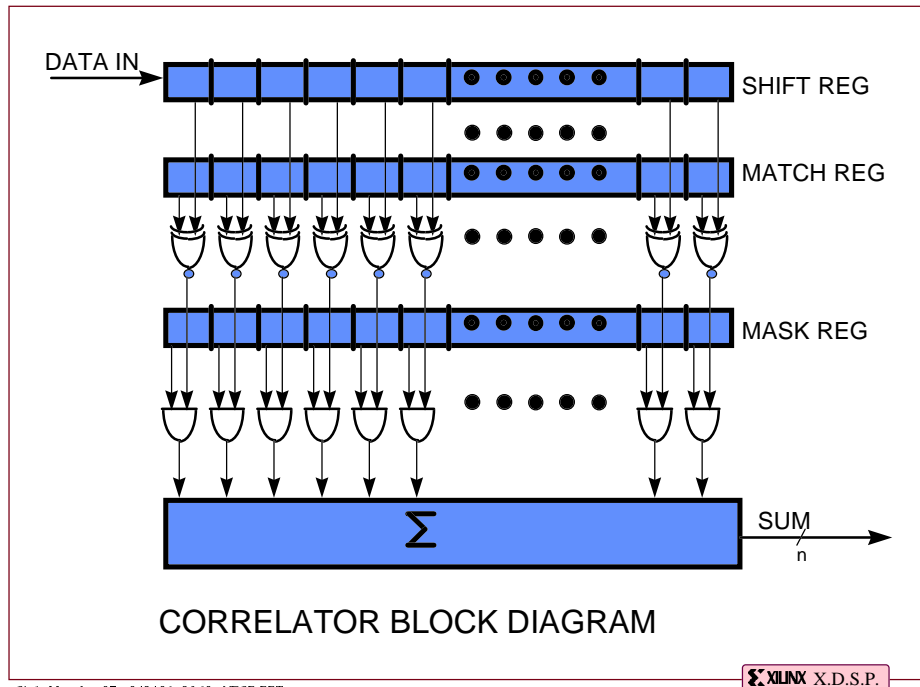
Slide Number 95 9/2/96 20:19 XDSP.PPT

 X.D.S.P.

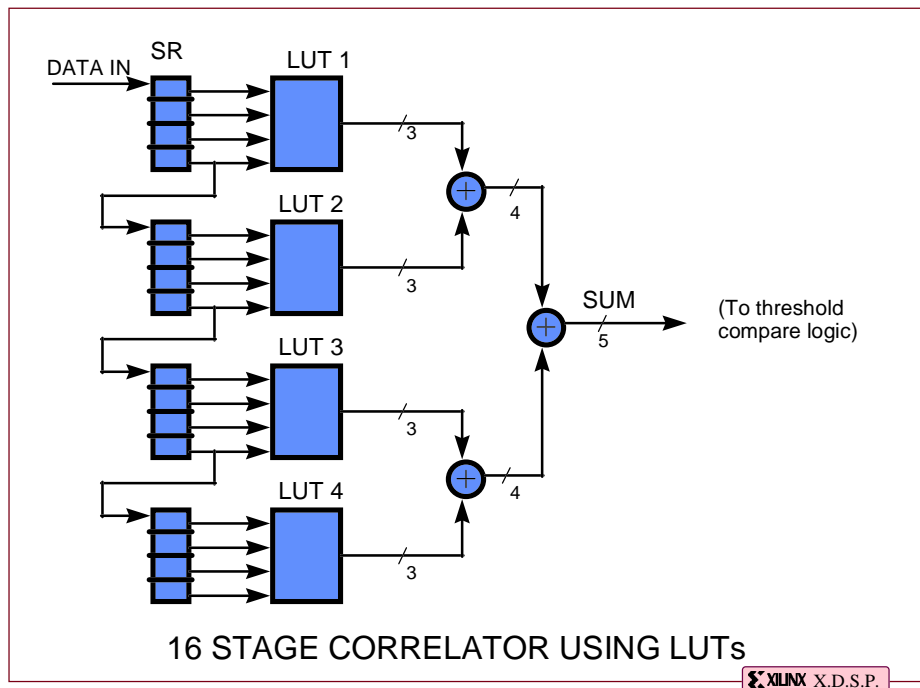
CORRELATORS

Slide Number 96 9/2/96 20:19 XDSP.PPT

 X.D.S.P.



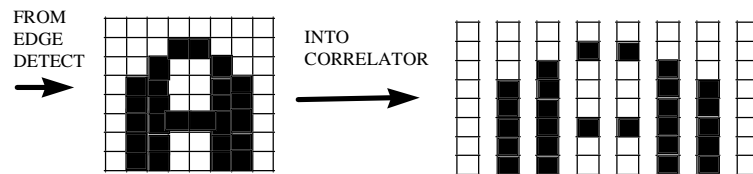
Slide Number 97 9/2/96 20:19 XDSP.PPT



Slide Number 98 9/2/96 20:19 XDSP.PPT

CASE STUDY - 2-D PATTERN MATCHING

EXAMPLE 8 X 8 PIXEL IMAGE



Example bit image post edge detection.

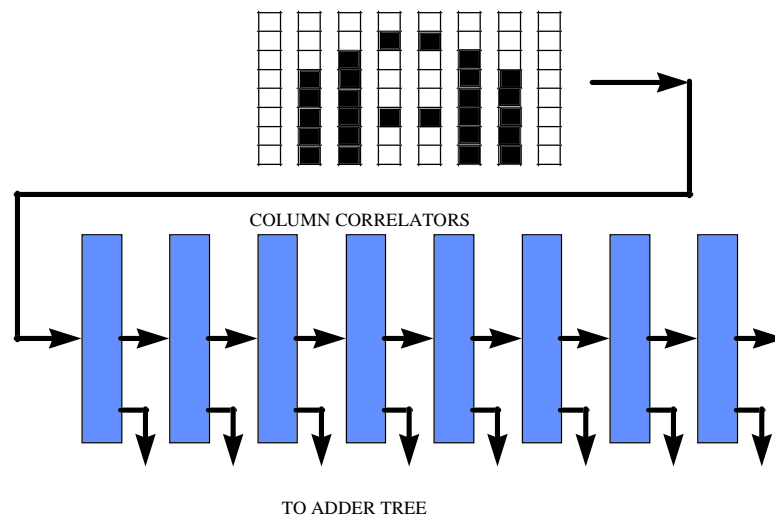
The incoming letter A was captured as a 8 bit grey scale image. The edge detector filters the data and forms a bit mapped image using a high pass filter. In other words, when a sharp transition is detected a 1 is output else a 0. This effectively increases the contrast.

The new image can now be feed into the bit correlator. Each column of the image is examined for how close it matches the match data and a binary value is generated. The column values are added together to form a image correlation value. This is then compared to a reference (threshold) and a hit or no hit signal generated.

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XILINX X.D.S.P.

CASE STUDY - 2D PATTERN MATCHING



NOTE: The data is parallel shifted from one column correlator to the next.

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XILINX X.D.S.P.

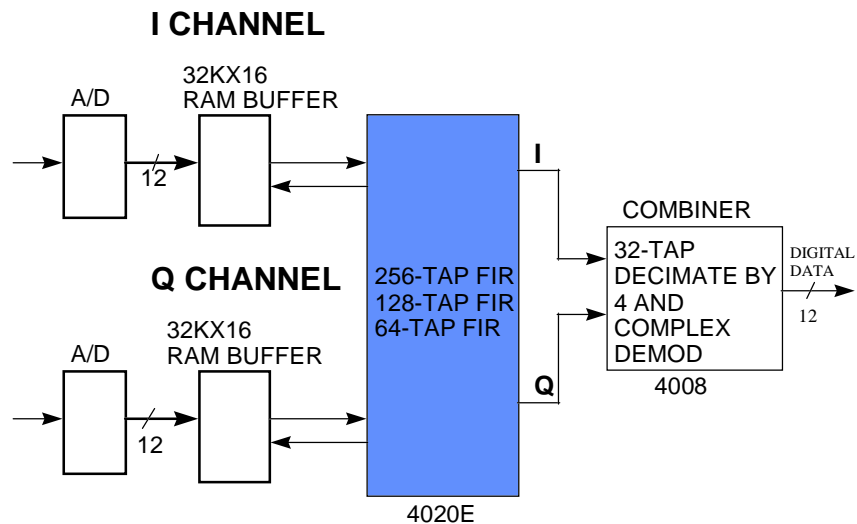
CASE STUDY - DSP CHIP ACCELERATION

- A large communications company primarily involved in the design and production of secure communication products. Also involved with cellular infrastructure design and production.
- Many high-level communications engineers.
- Typical DSP design includes multiple MC56xxx programmable DSPs.
- Some ASICs are used, but typical volumes are less than 10K/yr..
- Major need is **PERFORMANCE**.

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SYSTEM-LEVEL BLOCK DIAGRAM




Slide Number 102 9/2/96 20:20 XDSP.PPT

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CASE STUDY - DSP ACCELERATION

- System is a dual-mode (TDMA/AMPS) cellular phone test set.
- Technology will also be employed in a dual-mode cellular base station.
- Original design used 9 MC56116 programmable DSPs.
 - Approximately 10 sec was required for each test on each phone handset.
 - Program goal was to reduce test time to less than 500 msec per test.
- Final design implementation reduced test time to ~300 msec per test.


Slide Number 103 9/2/96 20:20 XDSP.PPT

 X.D.S.P.

CASE STUDY - DSP ACCELERATION

- System design engineer had three possible scenarios:
 - 1. Keep all 9 DSPs and live with low performance and complex real-time programming. (Medium Risk due to SW)
 - 2. Develop a DSP-based ASIC and meet performance goals. (Highest program Risk due to schedule and cost constraints).
 - 3. Use a FPGA as a DSP accelerator. (Lowest program Risk, meets all performance and cost goals)
- Final design used two XC4013s and one XC4008 per system
- Design uses dynamic in-circuit reconfigurability.
- All filter structures use either the conventional DA or the Decimation DA architecture.
- Systems engineer specified all filter constraints, while the hardware engineer did the actual hardware design.

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 X.D.S.P.

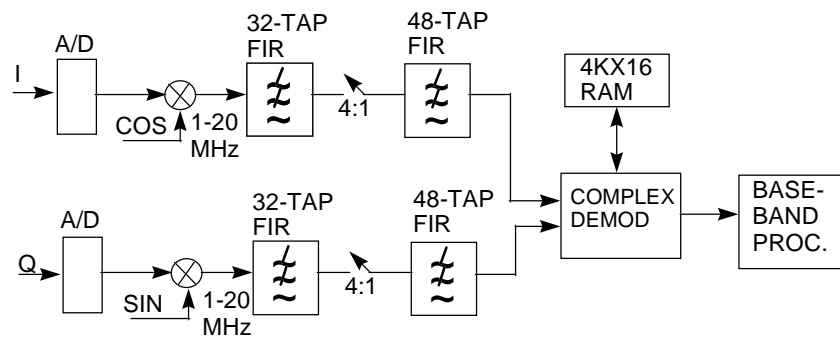
CASE STUDY - SATCOMM RECIEVER

- Designs and produces satellite-based voice and data modems, as well as complete turn-key SAT-COMM systems.
- Requirements:
 - Quadruple data rate over existing products.
 - Need to keep costs in-line with existing products.
 - Expected volumes are 2500 to 10K systems per year.
 - Symbol rate is much too fast for DSP chips, while volume is too low for ASICs.
- Earlier products used AT&T 16C/32C programmable DSPs.
- What is the solution?

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CASE STUDY - SATCOMM RECIEVER



RECEIVER BLOCK DIAGRAM

Slide Number 106 9/2/96 20:20 XDSP.PPT

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Decimate 4:1 FIR Filter (Down-Rate 4:1)

- Example: 32-tap decimate 4:1 FIR
- Discard 3 out of 4 output results
- Equivalent to sliding each Sample by 4 taps/clock
- Filter can be decomposed into 4 eight-tap subfilters
- Architect the filter such that no resources are used to calculate discarded outputs
- **Increases FIR filter input Sample rate by 4X**
- DALUT are composed of every 4th coefficient
- Symmetrical filters OK

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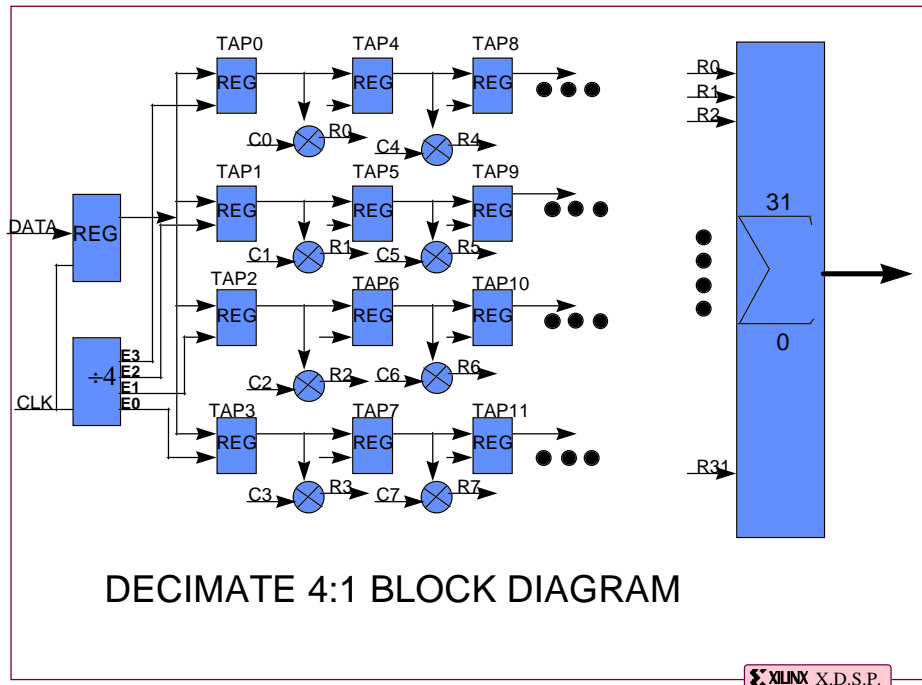
XILINX X.D.S.P.

16-Tap Down-Rate 4:1 Output Sequence

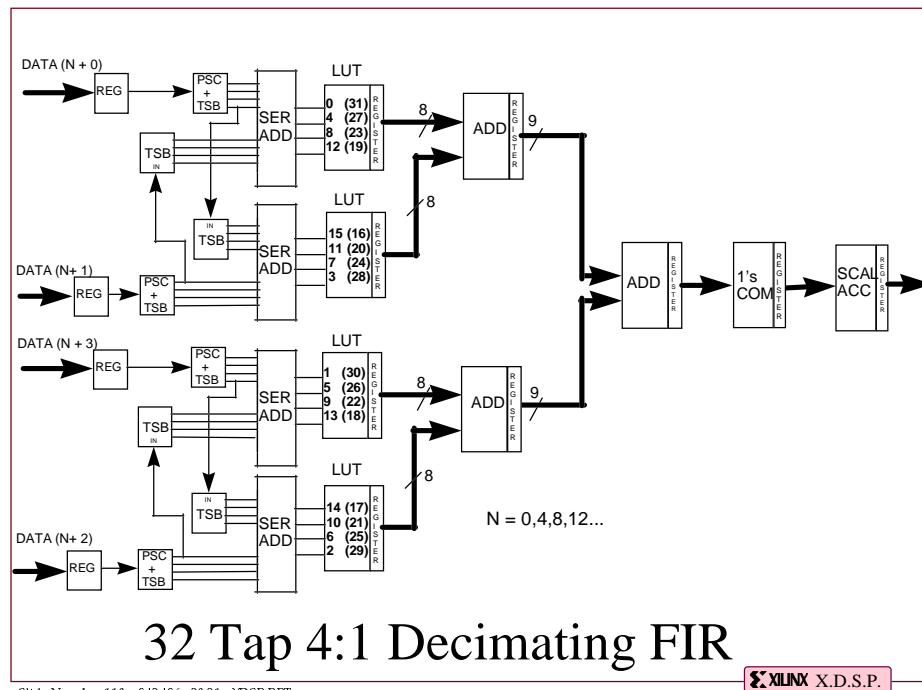
$$\begin{aligned}
 \text{Output (n)} &= D(n)*C0 + D(n-1)*C1 + D(n-2)*C2 + D(n-3)*C3 + \\
 &\quad D(n-4)*C4 + D(n-5)*C5 + D(n-6)*C6 + D(n-7)*C7 + \\
 &\quad D(n-8)*C8 + D(n-9)*C9 + D(n-10)*C10 + D(n-11)*C11 + \\
 &\quad D(n-12)*C12 + D(n-13)*C13 + D(n-14)*C14 + D(n-15)*C15 \\
 \text{Output (n+1)} &= D(n+1)*C0 + D(n)*C1 + D(n-1)*C2 + D(n-2)*C3 + \\
 &\quad D(n-3)*C4 + D(n-4)*C5 + D(n-5)*C6 + D(n-6)*C7 + \\
 &\quad D(n-7)*C8 + D(n-8)*C9 + D(n-9)*C10 + D(n-10)*C11 + \\
 &\quad D(n-11)*C12 + D(n-12)*C13 + D(n-13)*C14 + D(n-14)*C15 \\
 \text{Output (n+2)} &= D(n+2)*C0 + D(n+1)*C1 + D(n)*C2 + D(n-1)*C3 + \\
 &\quad D(n-2)*C4 + D(n-3)*C5 + D(n-4)*C6 + D(n-5)*C7 + \\
 &\quad D(n-6)*C8 + D(n-7)*C9 + D(n-8)*C10 + D(n-9)*C11 + \\
 &\quad D(n-10)*C12 + D(n-11)*C13 + D(n-12)*C14 + D(n-13)*C15 \\
 \text{Output (n+3)} &= D(n+3)*C0 + D(n+2)*C1 + D(n+1)*C2 + D(n)*C3 + \\
 &\quad D(n-1)*C4 + D(n-2)*C5 + D(n-3)*C6 + D(n-4)*C7 + \\
 &\quad D(n-5)*C8 + D(n-6)*C9 + D(n-7)*C10 + D(n-8)*C11 + \\
 &\quad D(n-9)*C12 + D(n-10)*C13 + D(n-11)*C14 + D(n-12)*C15 \\
 \text{Output (n+4)} &= D(n+4)*C0 + D(n+3)*C1 + D(n+2)*C2 + D(n+1)*C3 + \\
 &\quad D(n)*C4 + D(n-1)*C5 + D(n-2)*C6 + D(n-3)*C7 + \\
 &\quad D(n-4)*C8 + D(n-5)*C9 + D(n-6)*C10 + D(n-7)*C11 + \\
 &\quad D(n-8)*C12 + D(n-9)*C13 + D(n-10)*C14 + D(n-11)*C15
 \end{aligned}$$

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Slide Number 109 9/2/96 20:20 XDSP.PPT




Slide Number 110 9/2/96 20:21 XDSP.PPT

CASE STUDY - SATCOMM RECIEVER

- Design requires two 20MHz 32-tap FIR filter with 4:1 down-rate conversion.
 - Uses decimation DA architecture.
- 48-tap FIR filters are conventional DA structures.
- Complex DEMOD uses a 4010E.
- New hardware-based systems are now possible using these technequics.


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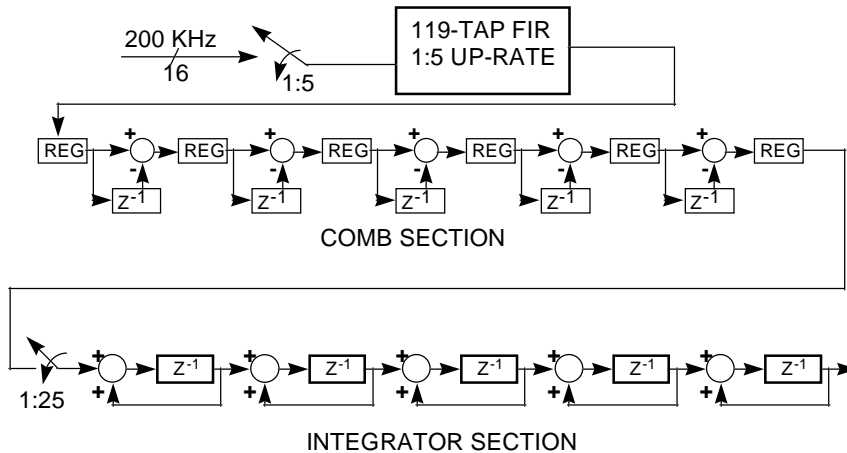
CASE STUDY - HF COMMUNICATIONS

- Needed two 25 MHz Hogenauer Filters.
 - A Hogenauer Filter allows for different data rates between the input rate and the output rate of the filter.
 - A Hogenauer Filter is simply a FIR filter followed by a Comb-Integrator filter.
- A Comb filter is a series of subtractors, while an Integrator is a series of accumulators.
- A Hogenauer Filter design can then be easily constructed from a simple FIR followed by an even simpler Comb-Integrator section.
- Programmable DSP-based solution only allowed for 200KHz data rate.
- IEEE Transactions on Acoustics, Speech, And Signal Processing, Vol. ASSP-29, NO.2, April 1981. By Eugene Hogenauer, Member, IEEE

Slide Number 112 9/2/96 20:21 XDSP.PPT

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HOGENAUER INTERPOLATION FILTER



Slide Number 113 9/2/96 20:21 XDSP.PPT

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Interpolation FIR Filter

- Example: 16-tap up-rate by 2 FIR
- Insert zeros between every other data sample
- Filter data output rate equals 2x input data rate
- Architect filter such that no resources are used to calculate zero * tap coeff
- 16-tap filter can be decomposed into two 8-tap parallel filters
- DALUT are composed of every other coeff

Slide Number 114 9/2/96 20:22 XDSP.PPT

XILINX X.D.S.P.

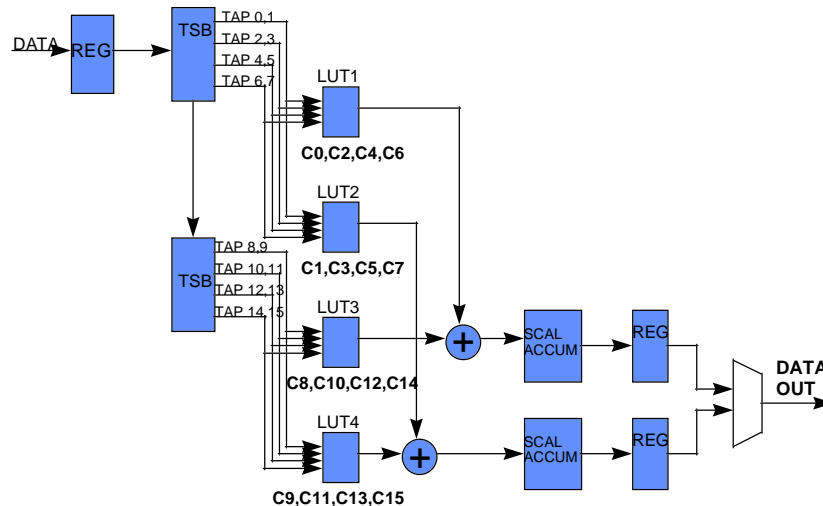
16-Tap 1:2 Interpolation Output Sequence

$$\begin{aligned} \text{Output (n)} = & D(n)*C0 + 0*C1 + D(n-1)*C2 + 0*C3 + \\ & D(n-2)*C4 + 0*C5 + D(n-3)*C6 + 0*C7 + \\ & D(n-4)*C8 + 0*C9 + D(n-5)*C10 + 0*C11 + \\ & D(n-6)*C12 + 0*C13 + D(n-7)*C14 + 0*C15 \end{aligned}$$

$$\begin{aligned} \text{Output (n+1)} = & 0*C0 + D(n)*C1 + 0*C2 + D(n-1)*C3 + \\ & 0*C4 + D(n-2)*C5 + 0*C6 + D(n-3)*C7 + \\ & 0*C8 + D(n-4)*C9 + 0*C10 + D(n-5)*C11 + \\ & 0*C12 + D(n-6)*C13 + 0*C14 + D(n-7)*C15 \end{aligned}$$

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INTERPOLATE 1:2 BLOCK DIAGRAM


Slide Number 116 9/2/96 20:22 XDSP.PPT

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CASE STUDY - HF COMMUNICATIONS


- Interpolation FIR is a 119-TAP FIR with 200KHz input rate, and 1MHz output rate (1:5).
- This is accomplished by inserting 4 zero values after each data sample on the input.
- The 119-TAP FIR uses ~480 CLBs. Need one each for I and Q.
- The Comb-Integrator section takes in data at 1MHz and outputs data at 25 MHz. This accomplished by inserting 24 zeros after each Comb output before the Integrator stage.
- Effective number of MACs = 238 Million MACs/sec for FIR sections.
- Effective number of additions/subtractions = 260 Million Ops/sec.
- Design allowed a maximum rate of 704 M MACs/sec & 1 Billion Ops/sec !!

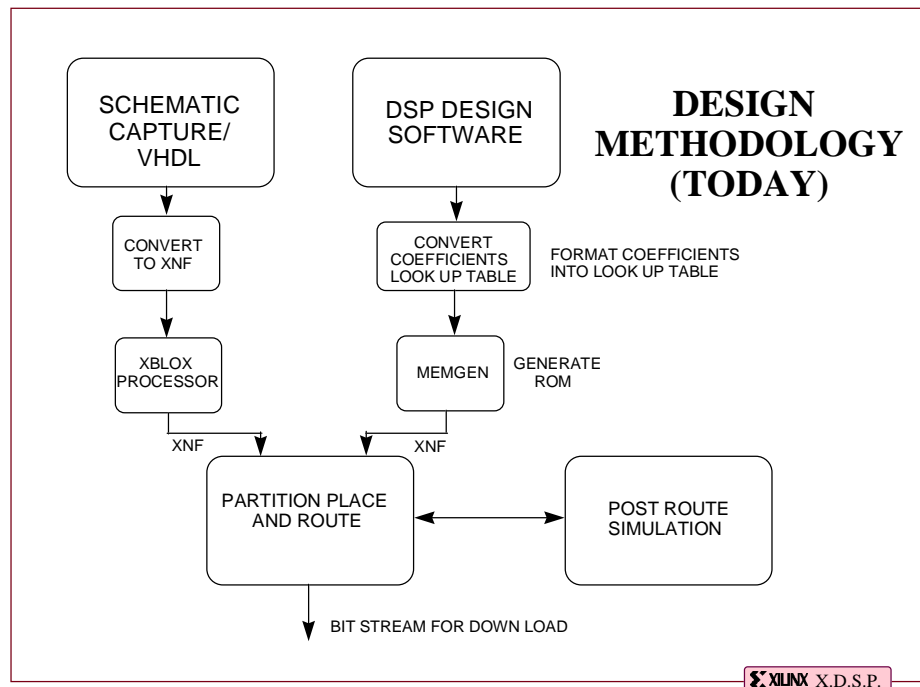
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DESIGN METHODOLOGY

Slide Number 118 9/2/96 20:22 XDSP.PPT

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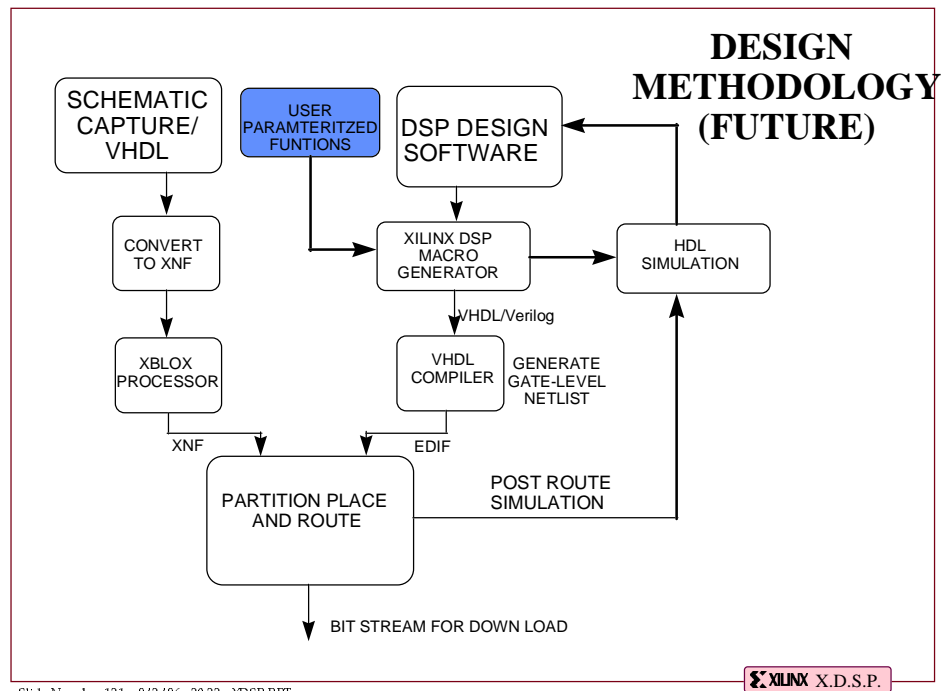


DESIGN METHODOLOGY SCHEMATIC CAPTURE or VHDL

- Filter Blocks can be Embedded in Complete design
- XBLOX Can Synthesize the Data Path Logic
- Filter Design Software used to design Filter Coefficients
- Complete System Level Design in a Single Chip
- Incremental Filter Design Using XACT 6.0/5.2
- Xact Performance used to specify bit rate

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Slide Number 121 9/2/96 20:22 XDSP.PPT

XDSP MACRO GENERATOR


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XDSP MACRO GENERATOR

- **Template Driven**
- **Windows 3.1, NT & 95 support**
- **Unix workstation support**
- **Support for most common DSP functions**
 - **FIR**
 - **IIR**
 - **Correlator**
 - **Multipliers**
- **Common parameterized interface to most DSP design tools**

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XDSP MACRO GENERATOR

(cont)

- **Context sensitive help**
- **Speed vs area optimization**
- **FIR architecture support for:**
 - **Serial Distributed Arithmetic**
 - **Parallel Distributed Arithmetic**
 - **Decimation & Interpolation**
- **Built-in support for Time-specs**

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 **X.D.S.P.**

XDSP MacGen Front Screen

FUNCTION:		▼	FAMILY:		▼
	FIR			3100A	
	IIR			4000E	
	CORRELATOR			5200	
	MULTIPLIER			6200	
	Math Functions			8100	
	ETC				

OK

HELP

CANCEL

Slide Number 125 9/2/96 20:23 XDSP.PPT

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FIR SCREEN

MODULE NAME: *.XSP

INPUT DATA

INPUT DATA SIZE:

NUMBER OF TAPS:

COEFFICIENT SIZE:

USE SYMMETRY ☐

CLK

DECIMATE BY:

INTERPOLATE BY:

COEFFICIENT FILE: *.XCF

OUTPUT DATA

OUTPUT DATA SIZE:

SAMPLE RATE:

SCHEMATIC TOOL:

MAKE SYM ☐

MAKE VHDL ☐

MAKE XNF ☐

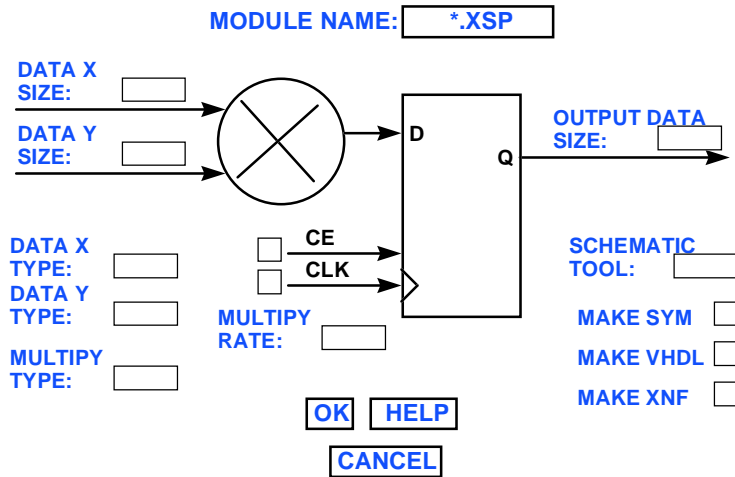
OK HELP

CANCEL

Slide Number 126 9/2/96 20:23 XDSP.PPT

XILINX X.D.S.P.

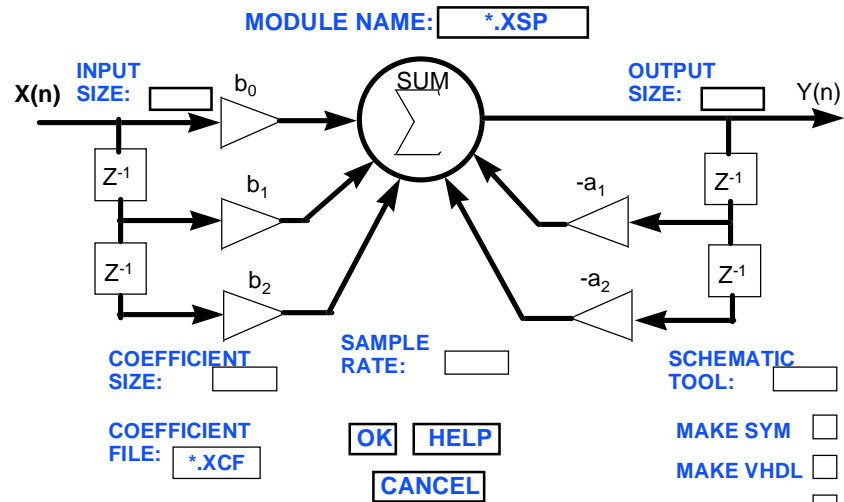
MULTIPLY SCREEN



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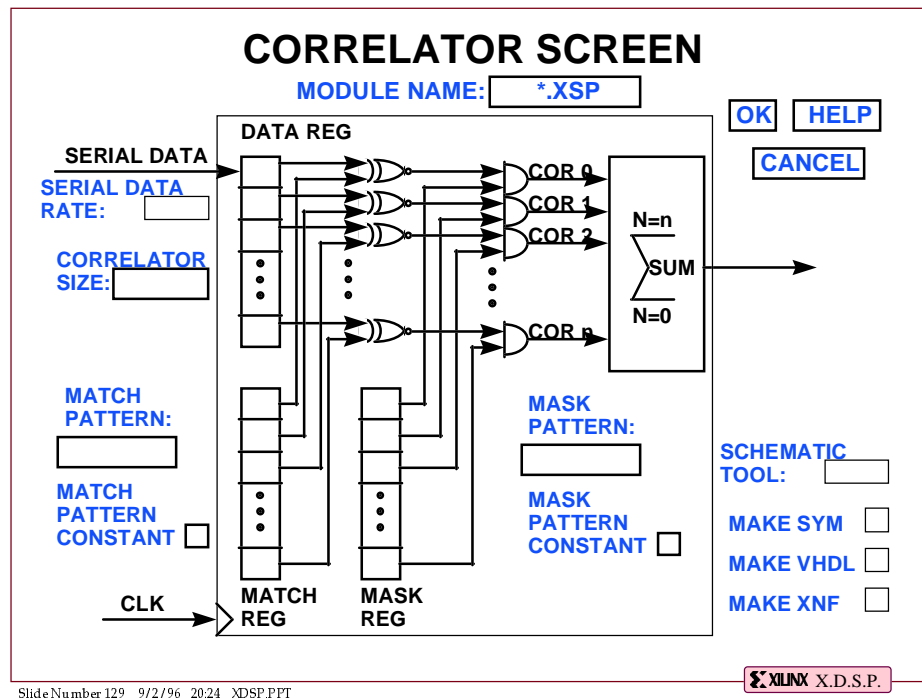
XILINX X.D.S.P.

BIQUAD SCREEN



Slide Number 128 9/2/96 20:23 XDSP.PPT

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Slide Number 129 9/2/96 20:24 XDSP.PPT

SUMMARY

Slide Number 130 9/2/96 20:24 XDSP.PPT

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XILINX VS. D.S.P. CHIP COMPARISON

When Does It Make Sense To Use FPGAs?

- High to Medium Sample Rate Systems
- Small Word Length
- Lots of Taps
- Fast Correlators
- Single Chip Solution Required
- Low Cost Migration Path (HardWire)
- Incremental Cost of DSP Chip
- DSP Application-Specific Chips

“Design Once”

Slide Number 131 9/2/96 20:24 XDSP.PPT


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XDSP

FPGA Applications, [Coming Attractions:](#)

- Signal Synthesis
- Modulation, Demodulation
- FFTs
- Neural Networks
- Video Signal Processing (2D, 3D Filters)

Slide Number 132 9/2/96 20:24 XDSP.PPT

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POSSIBILITIES

 **XILINX X.D.S.P.**

XILINX Hardware Digital Signal Processing

- There is an Alternative to Software DSP Chip Solutions Today
- Existing Xilinx 3100A, 4000E\EX are very efficient at Signal Processing
- System Level Application Specific Solution on a Single Chip
- Standard Product Configurable Solution
- Automatic Migration Path to a Lower Cost High Volume Solution

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 **XILINX X.D.S.P.**