

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.¹

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = -0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	4.75	5.25	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	Industrial	4.5	5.5	V
	Supply voltage relative to GND, $T_C = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per $^{\circ}\text{C}$.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ $I_{OH} = -4.0\text{mA}$, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ $I_{OH} = -1.0\text{mA}$, V_{CC} min	CMOS outputs	$V_{CC}-0.5$		V
V_{OL}	Low-level output voltage @ $I_{OL} = 12.0\text{mA}$, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
		Military		6.0	mA
I_L	Input or output leakage current		-10	+10	μA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}^*	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ (sample tested)		-0.02	-0.25	mA
I_{RLL}^*	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a MakeBits Tie option.

* Characterized Only.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000E Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output (Note 1)	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	Ceramic packages	+150
		Plastic packages	+125

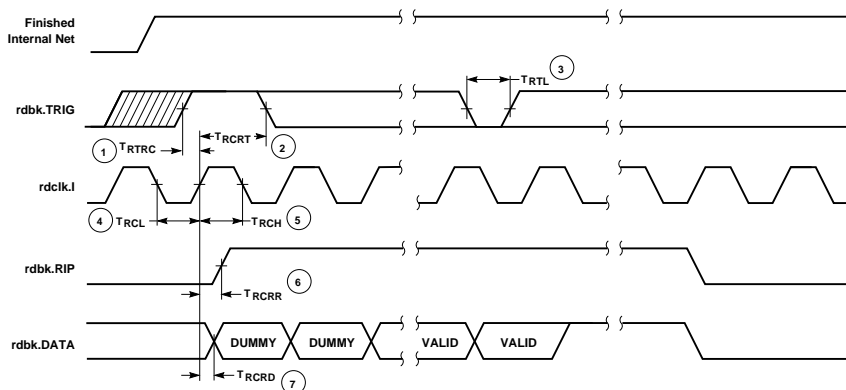
Note 1: Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to $V_{CC} + 2.0$ V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



X1790

	Description	Symbol	Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1 T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2 T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7 T_{RCRD}	-	250	ns
	rdbk.RIP delay	6 T_{RCRR}	-	250	ns
	High time	5 T_{RCH}	250	500	ns
	Low time	4 T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			-4	-3	-2	-1	
Description	Symbol	Device	Max	Max	Max	Max	Units
From pad through Primary buffer, to any clock K	T _{PG}	XC4003E	7.0	4.7	4.0		ns
		XC4005E	7.0	4.7	4.3		ns
		XC4006E	7.5	5.3	5.2		ns
		XC4008E	8.0	6.1	5.2		ns
		XC4010E	11.0	6.3	5.4		ns
		XC4013E	11.5	6.8	5.8		ns
		XC4020E	12.0	7.0	6.4		ns
		XC4025E	12.5	7.2	6.9		ns
From pad through Secondary buffer, to any clock K	T _{SG}	XC4003E	7.5	5.2	4.4		ns
		XC4005E	7.5	5.2	4.7		ns
		XC4006E	8.0	5.8	5.6		ns
		XC4008E	8.5	6.6	5.6		ns
		XC4010E	11.5	6.8	5.8		ns
		XC4013E	12.0	7.3	6.2		ns
		XC4020E	12.5	7.5	6.7		ns
		XC4025E	13.0	7.7	7.2		ns
					Preliminary	Advance	

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
Full length, both pull-ups, inputs from IOB I-pins	T _{WAF}	XC4003E	9.2	5.0	5.0	4.3	ns
		XC4005E	9.5	6.0	6.0	5.1	ns
		XC4006E	12.0	7.0	7.0	6.0	ns
		XC4008E	12.5	8.0	8.0	6.5	ns
		XC4010E	15.0	9.0	9.0	7.5	ns
		XC4013E	16.0	11.0	11.0	8.6	ns
		XC4020E	17.0	13.9	13.9	10.1	ns
		XC4025E	18.0	16.9	16.9		ns
Full length, both pull-ups, inputs from internal logic	T _{WAFL}	XC4003E	12.0	7.0	7.0	5.5	ns
		XC4005E	12.5	8.0	8.0	6.4	ns
		XC4006E	14.0	9.0	9.0	7.0	ns
		XC4008E	16.0	10.0	10.0	7.5	ns
		XC4010E	18.0	11.0	11.0	8.5	ns
		XC4013E	19.0	13.0	13.0	10.0	ns
		XC4020E	20.0	15.5	15.5	11.8	ns
		XC4025E	21.0	18.9	18.9		ns
Half length, one pull-up, inputs from IOB I-pins	T _{WAO}	XC4003E	10.5	6.0	6.0	5.1	ns
		XC4005E	10.5	7.0	7.0	6.0	ns
		XC4006E	13.5	8.0	8.0	6.6	ns
		XC4008E	14.0	9.0	9.0	7.0	ns
		XC4010E	16.0	10.0	10.0	7.5	ns
		XC4013E	17.0	12.0	12.0	10.0	ns
		XC4020E	18.0	15.0	15.0	11.8	ns
		XC4025E	19.0	17.6	17.6		ns
Half length, one pull-up, inputs from internal logic	T _{WAOL}	XC4003E	12.0	8.0	8.0	6.0	ns
		XC4005E	12.5	9.0	9.0	7.0	ns
		XC4006E	14.0	10.0	10.0	7.6	ns
		XC4008E	16.0	11.0	11.0	8.4	ns
		XC4010E	18.0	12.0	12.0	9.2	ns
		XC4013E	19.0	14.0	14.0	10.8	ns
		XC4020E	20.0	16.8	16.8	12.6	ns
		XC4025E	21.0	19.6	19.6		ns
					Preliminary	Advance	

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T _{IO1}	XC4003E	5.0	4.2	3.4	2.9	ns
		XC4005E	5.0	5.0	4.0	3.4	ns
		XC4006E	6.0	5.9	4.7	4.0	ns
		XC4008E	7.0	6.3	5.0	4.3	ns
		XC4010E	8.0	6.4	5.1	4.4	ns
		XC4013E	9.0	7.2	5.7	4.9	ns
		XC4020E	10.0	8.2	7.3	5.6	ns
		XC4025E	11.0	9.1	7.3		ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T _{IO2}	XC4003E	5.0	4.2	3.6	3.1	ns
		XC4005E	6.0	5.3	4.5	3.8	ns
		XC4006E	7.8	6.4	5.4	4.6	ns
		XC4008E	8.1	6.8	5.8	4.9	ns
		XC4010E	10.5	6.9	5.9	5.0	ns
		XC4013E	11.0	7.7	6.5	5.5	ns
		XC4020E	12.0	8.7	8.7	7.4	ns
		XC4025E	12.0	9.6	9.6		ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T _{ON}	XC4003E	5.5	4.6	3.9		ns
		XC4005E	7.0	6.0	5.7		ns
		XC4006E	7.5	6.7	5.7		ns
		XC4008E	8.0	7.1	6.0		ns
		XC4010E	8.5	7.3	6.2		ns
		XC4013E	8.7	7.5	7.0		ns
		XC4020E	11.0	8.4	7.1		ns
		XC4025E	11.0	8.4	7.1		ns
T going High to TBUF going inactive, not driving LL	T _{OFF}	All devices	1.8	1.5	1.3	1.1	ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T _{PUS}	XC4003E	20.0	14.0	14.0	10.1	ns
		XC4005E	23.0	16.0	16.0	11.6	ns
		XC4006E	25.0	18.0	18.0	13.0	ns
		XC4008E	27.0	20.0	20.0	14.5	ns
		XC4010E	29.0	22.0	22.0	15.9	ns
		XC4013E	32.0	26.0	26.0	18.8	ns
		XC4020E	35.0	32.5	32.5	23.5	ns
		XC4025E	42.0	39.1	39.1		ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T _{PUF}	XC4003E	9.0	7.0	6.0	5.4	ns
		XC4005E	10.0	8.0	6.8	5.8	ns
		XC4006E	11.5	9.0	7.7	6.5	ns
		XC4008E	12.5	10.0	8.5	7.5	ns
		XC4010E	13.5	11.0	9.4	8.0	ns
		XC4013E	15.0	13.0	11.7	9.4	ns
		XC4020E	16.0	14.8	14.8	10.5	ns
		XC4025E	18.0	16.5	16.5		ns
					Preliminary	Advance	

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Combinatorial Delays									
F/G inputs to X/Y outputs	T_{ILO}		2.7		2.0		1.6		1.3
F/G inputs via H' to X/Y outputs	T_{IHO}		4.7		4.3		2.7		2.2
C inputs via SR through H' to X/Y outputs	T_{HH0O}		4.1		3.3		2.4		1.9
C inputs via H' to X/Y outputs	T_{HH1O}		3.7		3.6		2.2		1.6
C inputs via DIN through H' to X/Y outputs	T_{HH2O}		4.5		3.6		2.6		1.9
CLB Fast Carry Logic									
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		3.2		2.6		2.1		1.7
Add/Subtract input (F3) to COUT	T_{ASCY}		5.5		4.4		3.7		2.7
Initialization inputs (F1, F3) to COUT	T_{INCY}		1.7		1.7		1.4		1.0
CIN through function generators to X/Y outputs	T_{SUM}		3.8		3.3		2.6		2.0
CIN to COUT, bypass function generators	T_{BYP}		1.0		0.7		0.6		0.5
Sequential Delays									
Clock K to outputs Q	T_{CKO}		3.7		2.8		2.8		1.9
Setup Time before Clock K									
F/G inputs	T_{ICK}	4.0		3.0		2.4		1.8	
F/G inputs via H'	T_{IHCK}	6.1		4.6		3.9		2.8	
C inputs via H0 through H'	T_{HH0CK}	4.5		3.6		3.5		2.4	
C inputs via H1 through H'	T_{HH1CK}	5.0		4.1		3.3		2.1	
C inputs via H2 through H'	T_{HH2CK}	4.8		3.8		3.7		2.5	
C inputs via DIN	T_{DICK}	3.0		2.4		2.0		1.0	
C inputs via EC	T_{ECCK}	4.0		3.0		2.6		2.0	
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		4.0		4.0		1.5	
C_{IN} input via F'/G'	T_{CCK}								
C_{IN} input via F'/G' and H'	T_{CHCK}								
Preliminary								Advance	

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Hold Time after Clock K									
F/G inputs	T_{CKI}	0		0		0		0	
F/G inputs via H'	T_{CKIH}	0		0		0		0	
C inputs via H0 through H'	T_{CKHH0}	0		0		0		0	
C inputs via H1 through H'	T_{CKHH1}	0		0		0		0	
C inputs via H2 through H'	T_{CKHH2}	0		0		0		0	
C inputs via DIN	T_{CKDI}	0		0		0		0	
C inputs via EC	T_{CKEC}	0		0		0		0	
C inputs via SR, going Low (inactive)	T_{CKR}	0		0		0		0	
Clock									
Clock High time	T_{CH}	4.5		4.0		4.0			
Clock Low time	T_{CL}	4.5		4.0		4.0			
Set/Reset Direct									
Width (High)	T_{RPW}	5.5		4.0		4.0		3.0	
Delay from C inputs via S/R, going High to Q	T_{RIO}		6.5		4.0		4.0		3.0
Master Set/Reset (Note 1)									
Width (High or Low)	T_{MRW}	13.0		11.5		11.5			
Delay from Global Set/Reset net to Q	T_{MRQ}		23.0		18.7		17.4		
Global Set/Reset inactive to first active clock K edge	T_{MRK}								
Toggle Frequency ² (MHz) (Note 2)	F_{TOG}		113		142		160		
						Preliminary		Advance	

Note 1: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

Note 2: Export Control Max. flip-flop toggle rate.

XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

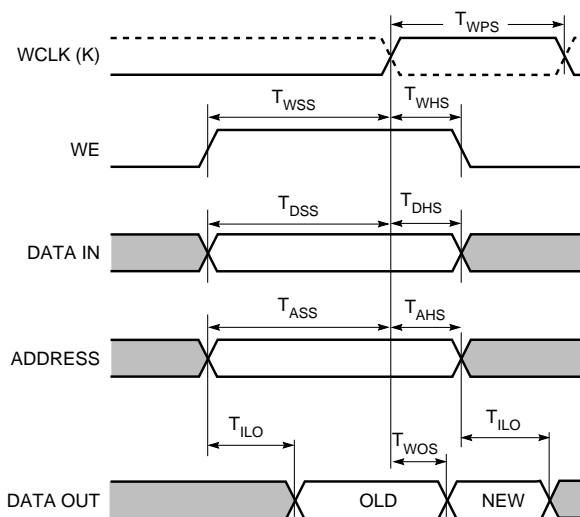
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1	
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation										
Address write cycle time	16x2	T_{WCS}	15.0		14.4		11.6			
(clock K period)	32x1	T_{WCTS}	15.0		14.4		11.6			
Clock K pulse width	16x2	T_{WPS}	7.5	1 ms	7.2	1 ms	5.8	1 ms		
(active edge)	32x1	T_{WPTS}	7.5	1 ms	7.2	1 ms	5.8	1 ms		
Address setup time	16x2	T_{ASS}	2.8		2.4		2.0			
before clock K	32x1	T_{ASTS}	2.8		2.4		2.0			
Address hold time	16x2	T_{AHS}	0		0		0			
after clock K	32x1	T_{AHTS}	0		0		0			
DIN setup time	16x2	T_{DSS}	3.5		3.2		2.7			
before clock K	32x1	T_{DSTS}	2.5		1.9		1.7			
DIN hold time	16x2	T_{DHS}	0		0		0			
after clock K	32x1	T_{DHTS}	0		0		0			
WE setup time	16x2	T_{WSS}	2.2		2.0		1.6			
before clock K	32x1	T_{WSTS}	2.2		2.0		1.6			
WE hold time	16x2	T_{WHS}	0		0		0			
after clock K	32x1	T_{WHTS}	0		0		0			
Data valid	16x2	T_{WOS}		10.3		8.8		7.9		
after clock K	32x1	T_{WOTS}		11.6		10.3		9.3		
								Preliminary	Advance	

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.



X6461

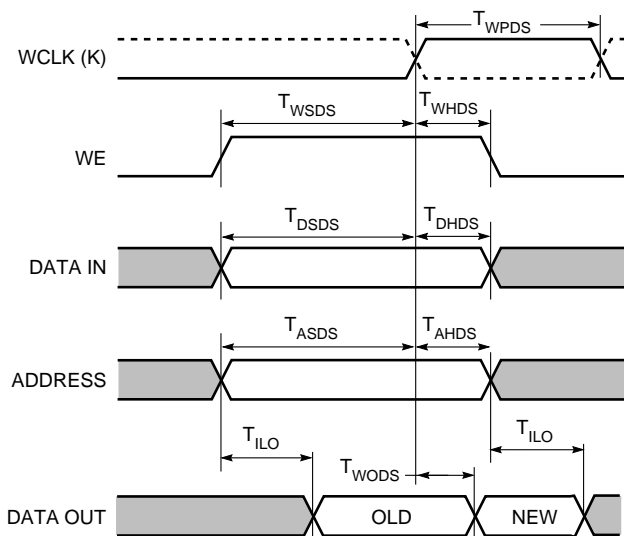
XC4000E CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1	
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation										
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		14.4		11.6			
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.5	1 ms	7.2	1 ms	5.8	1 ms		
Address setup time before clock K	16x1	T_{ASDS}	2.8		2.5		2.1			
Address hold time after clock K	16x1	T_{AHDS}	0		0		0			
DIN setup time before clock K	16x1	T_{DSDS}	2.2		1.9		1.6			
DIN hold time after clock K	16x1	T_{DHDS}	0		0		0			
WE setup time before clock K	16x1	T_{WSDS}	2.2		2.0		1.6			
WE hold time after clock K	16x1	T_{WHDS}	0.3		0		0			
Data valid after clock K	16x1	T_{WODS}		10.0		7.8		7.0		
							Preliminary		Advance	

Note: Applicable Read timing specifications are identical to 16x2 Level-Sensitive Read timing.



X6474

XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

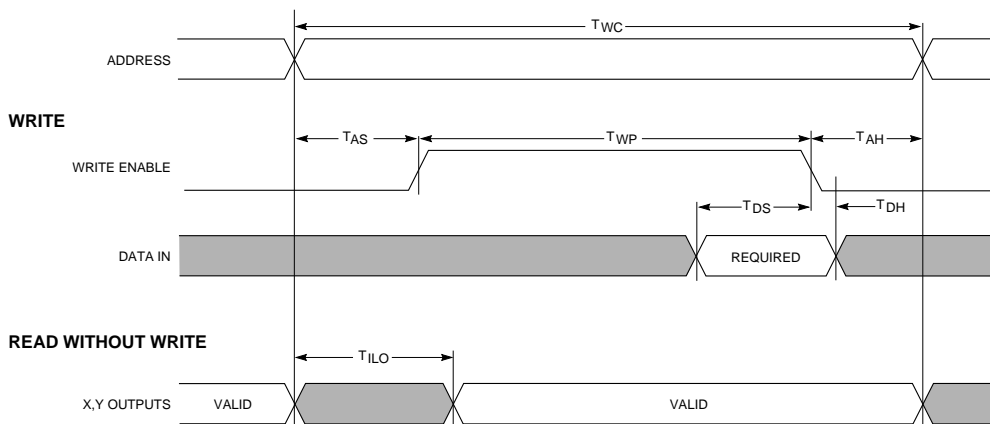
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

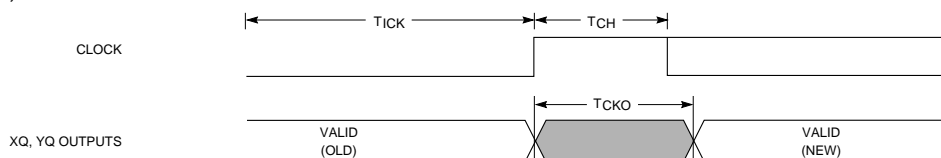
Speed Grade			-4		-3		-2		-1	
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation										
Address write cycle time	16x2	T_{WC}	8.0		8.0		8.0			
	32x1	T_{WCT}	8.0		8.0		8.0			
Write Enable pulse width	16x2	T_{WP}	4.0		4.0		4.0			
(High)	32x1	T_{WPT}	4.0		4.0		4.0			
Address setup time	16x2	T_{AS}	2.0		2.0		2.0			
before WE	32x1	T_{AST}	2.0		2.0		2.0			
Address hold time	16x2	T_{AH}	2.5		2.0		2.0			
after end of WE	32x1	T_{AHT}	2.0		2.0		2.0			
DIN setup time	16x2	T_{DS}	4.0		2.2		0.8			
before end of WE	32x1	T_{DST}	5.0		2.2		0.8			
DIN hold time	16x2	T_{DH}	2.0		2.0		2.0			
after end of WE	32x1	T_{DHT}	2.0		2.0		2.0			
Read Operation										
Address read cycle time	16x2	T_{RC}	4.5		3.1		2.6			
	32x1	T_{RCT}	6.5		5.5		3.8			
Data valid after address	16x2	T_{ILO}		2.7		2.0		1.6		
change (no Write Enable)	32x1	T_{IHO}		4.7		4.3		2.7		
Read Operation, Clocking Data into Flip-Flop										
Address setup time	16x2	T_{ICK}	4.0		3.0		2.4			
before clock K	32x1	T_{IHCK}	6.1		4.6		3.9			
Read During Write										
Data valid after WE goes	16x2	T_{WO}		10.0		6.0		4.9		
active (DIN stable	32x1	T_{WOT}		12.0		7.3		5.6		
before WE)										
Data valid after DIN	16x2	T_{DO}		9.0		6.6		5.8		
(DIN changes during WE)	32x1	T_{DOT}		11.0		7.6		6.2		
Read During Write, Clocking Data into Flip-Flop										
WE setup time	16x2	T_{WCK}	8.0		6.0		5.1			
before clock K	32x1	T_{WCKT}	9.6		6.8		5.8			
Data setup time	16x2	T_{DCK}	7.0		5.2		4.4			
before clock K	32x1	T_{DCKT}	8.0		6.2		5.3			
							Preliminary		Advance	

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

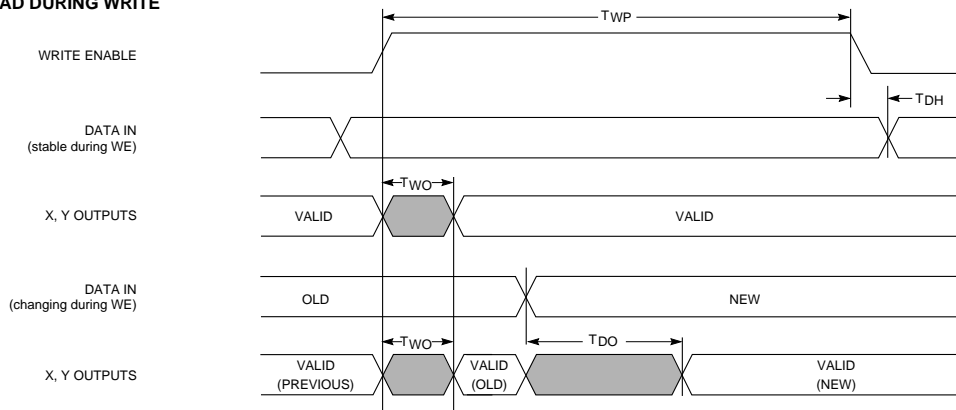
XC4000E CLB Level-Sensitive RAM Timing Characteristics



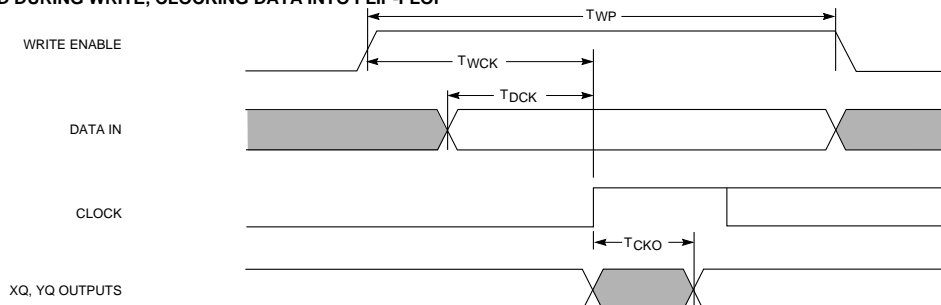
READ, CLOCKING DATA INTO FLIP-FLOP



READ DURING WRITE



READ DURING WRITE, CLOCKING DATA INTO FLIP-FLOP



X2640

XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

Speed Grade			-4	-3	-2	-1
Description	Symbol	Device				
Global Clock to Output (fast) using OFF	T_{ICKOF}	XC4003E	12.5	10.2	8.7	5.8
		XC4005E	14.0	10.7	9.1	6.2
		XC4006E	14.5	10.7	9.1	6.4
		XC4008E	15.0	10.8	9.2	6.6
		XC4010E	16.0	10.9	9.3	6.8
		XC4013E	16.5	11.0	9.4	7.2
		XC4020E	17.0	11.0	10.2	7.4
		XC4025E	17.0	12.6	10.8	
Global Clock to Output (slew-limited) using OFF	T_{ICKO}	XC4003E	16.5	14.0	11.5	7.8
		XC4005E	18.0	14.7	12.0	8.2
		XC4006E	18.5	14.7	12.0	8.4
		XC4008E	19.0	14.8	12.1	8.6
		XC4010E	20.0	14.9	12.2	8.8
		XC4013E	20.5	15.0	12.8	9.2
		XC4020E	21.0	15.1	12.8	9.4
		XC4025E	21.0	15.3	13.0	
Input Setup Time, using IFF (no delay)	T_{PSUF}	XC4003E	2.5	2.3	2.3	1.5
		XC4005E	2.0	1.2	1.2	0.8
		XC4006E	1.9	1.0	1.0	0.6
		XC4008E	1.4	0.6	0.6	0.2
		XC4010E	1.0	0.2	0.2	0
		XC4013E	0.5	0	0	0
		XC4020E	0	0	0	0
		XC4025E	0	0	0	
Input Hold Time, using IFF (no delay)	T_{PHF}	XC4003E	4.0	4.0	4.0	1.5
		XC4005E	4.6	4.5	4.5	2.0
		XC4006E	5.0	4.7	4.7	2.0
		XC4008E	6.0	5.1	5.1	2.5
		XC4010E	6.0	5.5	5.5	2.5
		XC4013E	7.0	6.5	5.5	3.0
		XC4020E	7.5	6.7	5.7	3.5
		XC4025E	8.0	7.0	5.9	
Input Setup Time, using IFF (with delay)	T_{PSU}	XC4003E	8.5	7.0	6.0	5.0
		XC4005E	8.5	7.0	6.0	5.0
		XC4006E	8.5	7.0	6.0	5.0
		XC4008E	8.5	7.0	6.0	5.0
		XC4010E	8.5	7.0	6.0	5.0
		XC4013E	8.5	7.0	6.0	5.0
		XC4020E	9.5	7.0	6.8	5.0
		XC4025E	9.5	7.6	6.8	
Input Hold Time, using IFF (with delay)	T_{PH}	XC4003E	0	0	0	0
		XC4005E	0	0	0	0
		XC4006E	0	0	0	0
		XC4008E	0	0	0	0
		XC4010E	0	0	0	0
		XC4013E	0	0	0	0
		XC4020E	0	0	0	0
		XC4025E	0	0	0	
OFF = Output Flip-Flop			IFF = Input Flip-Flop or Latch			
					Preliminary	Advance

XC4000E IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1	
Description	Symbol	Device	Min	Max	Min	Max	Min	Max	Min	Max
Propagation Delays (TTL Inputs)										
Pad to I1, I2	T_{PID}	All devices		3.0		2.5		2.0		1.4
Pad to I1, I2 via transparent latch, no delay with delay	T_{PLI}	All devices		4.8		3.6		3.6		2.8
	T_{PDLI}	XC4003E		10.4		9.3		6.9		6.4
		XC4005E		10.8		9.6		7.4		6.5
		XC4006E		10.8		10.2		8.1		6.9
		XC4008E		10.8		10.6		8.2		7.0
		XC4010E		11.0		10.8		8.3		7.3
		XC4013E		11.4		11.2		9.8		8.4
		XC4020E		13.8		12.4		11.5		9.0
		XC4025E		13.8		13.7		12.4		
(CMOS Inputs)										
Pad to I1, I2	T_{PIDC}	All devices		5.5		4.1		3.7		1.9
Pad to I1, I2 via transparent latch, no delay with delay	T_{PLIC}	All devices		8.8		6.8		6.2		3.3
	T_{PDLIC}	XC4003E		16.5		12.4		11.0		6.9
		XC4005E		16.5		13.2		11.9		7.0
		XC4006E		16.8		13.4		12.1		7.4
		XC4008E		17.3		13.8		12.4		7.4
		XC4010E		17.5		14.0		12.6		7.8
		XC4013E		18.0		14.4		13.0		9.0
		XC4020E		20.8		15.6		14.0		9.5
		XC4025E		20.8		15.6		14.0		
(TTL or CMOS)										
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		5.6		2.8		2.8		2.7
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		6.2		4.0		3.9		3.2
Hold Times (Note 1)										
Pad to Clock (IK), no delay with delay	T_{IKPI}	All devices	0		0		0		0	
	T_{IKPID}	All devices	0		0		0		0	
Clock Enable (EC) to Clock (IK), no delay with delay	T_{IKEC}	All devices	1.5		1.5		0.9		0	
	T_{IKECD}	All devices	0		0		0		0	
							Preliminary		Advance	

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1	
Description	Symbol	Device	Min	Max	Min	Max	Min	Max	Min	Max
Setup Times (TTL Inputs)										
Pad to Clock (IK), no delay with delay	T _{PICK} T _{PICKD}	All devices	4.0		2.6		2.0		1.5	
		XC4003E	10.9		8.2		6.0		4.8	
		XC4005E	10.9		8.7		6.1		5.1	
		XC4006E	10.9		9.2		6.2		5.8	
		XC4008E	11.1		9.6		6.3		5.8	
		XC4010E	11.3		9.8		6.4		6.0	
		XC4013E	11.8		10.2		7.9		7.3	
		XC4020E	14.0		11.4		9.4		8.2	
		XC4025E	14.0		11.4		10.0			
(CMOS Inputs)										
Pad to Clock (IK), no delay with delay	T _{PICKC} T _{PICKDC}	All devices	6.0		3.3		2.4		2.0	
		XC4003E	12.0		8.8		6.9		5.3	
		XC4005E	12.0		9.7		8.0		5.6	
		XC4006E	12.3		9.9		8.1		6.3	
		XC4008E	12.8		10.3		8.2		6.3	
		XC4010E	13.0		10.5		8.3		6.5	
		XC4013E	13.5		10.9		10.0		7.9	
		XC4020E	16.0		12.1		12.1		8.1	
		XC4025E	16.0		12.1		12.1			
(TTL or CMOS)										
Clock Enable (EC) to Clock (IK), no delay with delay	T _{EICK} T _{EICKD}	All devices	3.5		2.5		2.1			
		XC4003E	10.4		8.1		4.3			
		XC4005E	10.4		8.5		5.6			
		XC4006E	10.4		9.1		6.7			
		XC4008E	10.4		9.5		6.9			
		XC4010E	10.7		9.7		7.1			
		XC4013E	11.1		10.1		9.0			
		XC4020E	14.0		11.3		10.6			
		XC4025E	14.0		11.3		11.0			
Global Set/Reset (Note 3)										
Delay from GSR net through Q to I1, I2	T _{RRI}		12.0		7.8		6.8		6.8	
GSR width	T _{MRW}	13.0		11.5		11.5				
GSR inactive to first active Clock (IK) edge	T _{MRI}									
							Preliminary		Advance	

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Propagation Delays (TTL Output Levels)									
Clock (OK) to Pad, fast	T _{OKPOF}		7.5		6.5		4.5		3.0
slew-rate limited	T _{OKPOS}		11.5		9.5		7.0		5.0
Output (O) to Pad, fast	T _{OPF}		8.0		5.5		4.8		3.5
slew-rate limited	T _{OPS}		12.0		8.5		7.3		5.5
3-state to Pad hi-Z (slew-rate independent)	T _{TSHZ}		5.0		4.2		3.8		
3-state to Pad active and valid, fast	T _{TSONF}		9.7		8.1		7.3		
slew-rate limited	T _{TSONS}		13.7		11.1		9.8		
Propagation Delays (CMOS Output Levels)									
Clock (OK) to Pad, fast	T _{OKPOFC}		9.5		7.8		7.0		4.0
slew-rate limited	T _{OKPOSC}		13.5		11.6		10.4		7.0
Output (O) to Pad, fast	T _{OPFC}		10.0		9.7		8.7		4.0
slew-rate limited	T _{OPSC}		14.0		13.4		12.1		6.0
3-state to Pad hi-Z (slew-rate independent)	T _{TSHZC}		5.2		4.3		3.9		
3-state to Pad active and valid, fast	T _{TSONFC}		9.1		7.6		6.8		
slew-rate limited	T _{TSONSC}		13.1		11.4		10.2		
						Preliminary		Advance	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Setup and Hold									
Output (O) to clock (OK) setup time	T_{OOK}	5.0		4.6		3.8		2.3	
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		0	
Clock Enable (EC) to clock (OK) setup	T_{ECOK}	4.8		3.5		2.7		2.5	
Clock Enable (EC) to clock (OK) hold	T_{OKEC}	1.2		1.2		0.5		0	
Clock									
Clock High	T_{CH}	4.5		4.0		4.0			
Clock Low	T_{CL}	4.5		4.0		4.0			
Global Set/Reset (Note 3)									
Delay from GSR net to Pad	T_{RPO}		15.0		11.8		8.7		7.0
GSR width	T_{MRW}	13.0		11.5		11.5			
GSR inactive to first active clock (OK) edge	T_{MRO}								
						Preliminary		Advance	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Setup and Hold									
Input (TDI) to clock (TCK) setup time	T _{TDITCK}	30		30		30		20	
Input (TDI) to clock (TCK) hold time	T _{TCKTDI}	0		0		0		0	
Input (TMS) to clock (TCK) setup time	T _{TMSTCK}	15		15		15		10	
Input (TMS) to clock (TCK) hold time	T _{TCKTMS}	0		0		0		0	
Propagation Delay									
Clock (TCK) to Pad (TDO)	T _{TCKPO}		30		30		30		20
Clock									
Clock (TCK) High	T _{TCKH}	5		5		5		4	
Clock (TCK) Low	T _{TCKL}	5		5		5		4	
F _{MAX} (MHz)									
	F _{MAX}		15		15		15		25
						Preliminary		Advance	

- Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
- Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.
- Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.