

XC4000L Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.¹

XC4000L Operating Conditions

| Symbol | Description | Min | Max | Units |
|----------|--|------|----------------|-------|
| V_{CC} | Supply voltage relative to GND, $T_J = -0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ Commercial | 3.0 | 3.6 | V |
| V_{IH} | High-level input voltage | 2.0 | $V_{CC} + 0.3$ | V |
| V_{IL} | Low-level input voltage | -0.3 | 0.8 | V |
| T_{IN} | Input signal transition time (Note 2) | | 250 | ns |

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per $^{\circ}\text{C}$.

Note 2: Typical value only. Not tested or characterized.

XC4000L DC Characteristics Over Operating Conditions

| Symbol | Description | Min | Max | Units |
|-----------|---|------------------------|------|---------------|
| V_{OH} | High-level output voltage @ $I_{OH} = -4.0\text{mA}$, V_{CC} min | 2.4 | | V |
| | High-level output voltage @ $I_{OH} = -0.1\text{mA}$, V_{CC} min | $V_{CC}-0.2$ | | V |
| V_{OL} | Low-level output voltage @ $I_{OL} = +4.0\text{mA}$, V_{CC} min | | 0.4 | V |
| | Low-level output voltage @ $I_{OL} = +0.1\text{mA}$, V_{CC} min | | 0.2 | V |
| I_{CCO} | Quiescent FPGA supply current (Note 1) | | 100 | μA |
| I_L | Input or output leakage current | -10 | +10 | μA |
| C_{IN} | Input capacitance (sample tested) | PQFP and MQFP packages | 10 | pF |
| | | Other packages | 16 | pF |
| I_{RIN} | Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ (sample tested) | 0.02 | 0.25 | mA |
| I_{RLI} | Horizontal Longline pull-up (when selected) @ logic Low | 0.2 | 2.5 | mA |

Note 1: With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option in the bitstream generation software.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

XC4000L Absolute Maximum Ratings

| Symbol | Description | | Units |
|-----------|--|------------------------|-------|
| V_{CC} | Supply voltage relative to GND | -0.5 to +7.0 | V |
| V_{IN} | Input voltage relative to GND (Note 1) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{TS} | Voltage applied to 3-state output (Note 1) | -0.5 to $V_{CC} + 0.5$ | V |
| T_{STG} | Storage temperature (ambient) | -65 to +150 | °C |
| T_{SOL} | Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm) | +260 | °C |
| T_J | Junction temperature | Ceramic packages | +150 |
| | | Plastic packages | +125 |

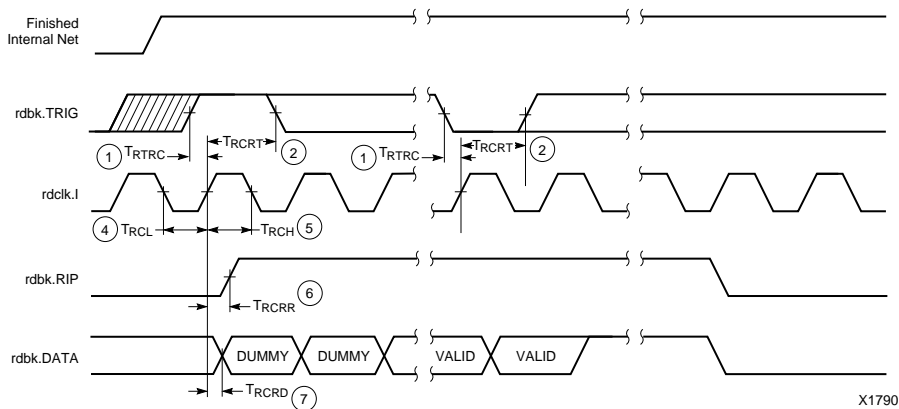
Note 1: Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to $V_{CC} + 2.0$ V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000L Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



| | Description | Symbol | Min | Max | Units |
|-----------|--|--------------|-----|-----|-------|
| rdbk.TRIG | rdbk.TRIG setup to initiate and abort Readback | 1 T_{RTRC} | 200 | - | ns |
| | rdbk.TRIG hold to initiate and abort Readback | 2 T_{RCRT} | 50 | - | ns |
| rdclk.1 | rdbk.DATA delay | 7 T_{RCRD} | - | 250 | ns |
| | rdbk.RIP delay | 6 T_{RCRR} | - | 250 | ns |
| | High time | 5 T_{RCH} | 1 | 5 | ns |
| | Low time | 4 T_{RCL} | 1 | 5 | ns |

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

XC4000L Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

| Speed Grade | | | -5 | -4 | | Units |
|---|-----------------|---------|-------------|-----|--|-------|
| Description | Symbol | Device | Max | Max | | |
| From pad through Primary buffer, to any clock K | T _{PG} | XC4005L | 7.9 | | | ns |
| | | XC4010L | 9.9 | | | ns |
| | | XC4013L | 11.9 | | | ns |
| From pad through Secondary buffer, to any clock K | T _{SG} | XC4005L | 9.4 | | | ns |
| | | XC4010L | 11.4 | | | ns |
| | | XC4013L | 13.4 | | | ns |
| | | | Preliminary | | | |

XC4000L Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

| Speed Grade | | | -5 | -4 | | Units |
|---|-------------------|---------|-------------|-----|--|-------|
| Description | Symbol | Device | Max | Max | | |
| Full length, both pull-ups, inputs from IOB I-pins | T _{WAF} | XC4005L | 12.4 | | | ns |
| | | XC4010L | 16.8 | | | ns |
| | | XC4013L | 20.0 | | | ns |
| Full length, both pull-ups, inputs from internal logic | T _{WAFL} | XC4005L | 15.9 | | | ns |
| | | XC4010L | 20.7 | | | ns |
| | | XC4013L | 25.0 | | | ns |
| Half length, one pull-up, inputs from IOB I-pins | T _{WAO} | XC4005L | 12.4 | | | ns |
| | | XC4010L | 16.8 | | | ns |
| | | XC4013L | 20.0 | | | ns |
| Half length, one pull-up, inputs from internal logic | T _{WAOL} | XC4005L | 15.9 | | | ns |
| | | XC4010L | 20.7 | | | ns |
| | | XC4013L | 25.0 | | | ns |
| | | | Preliminary | | | |

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000L Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

| Speed Grade | | | -5 | -4 | | Units |
|--|------------------|-------------|-------------|-----|--|-------|
| Description | Symbol | Device | Max | Max | | |
| TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1) | T _{IO1} | XC4005L | 8.1 | | | ns |
| | | XC4010L | 10.0 | | | ns |
| | | XC4013L | 12.0 | | | ns |
| I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1) | T _{IO2} | XC4005L | 7.5 | | | ns |
| | | XC4010L | 9.4 | | | ns |
| | | XC4013L | 11.2 | | | ns |
| T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1) | T _{ON} | XC4005L | 9.6 | | | ns |
| | | XC4010L | 10.9 | | | ns |
| | | XC4013L | 13.0 | | | ns |
| T going High to TBUF going inactive, not driving LL | T _{OFF} | All devices | 2.2 | | | ns |
| T going High to LL going from Low to High, pulled up by a single resistor. (Note 2) | T _{PUS} | XC4005L | 24.1 | | | ns |
| | | XC4010L | 30.1 | | | ns |
| | | XC4013L | 36.0 | | | ns |
| T going High to LL going from Low to High, pulled up by two resistors. (Note1) | T _{PUF} | XC4005L | 13.1 | | | ns |
| | | XC4010L | 17.2 | | | ns |
| | | XC4013L | 20.0 | | | ns |
| | | | Preliminary | | | |

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000L CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | -5 | | -4 | | | |
|--|--------------------|------|------|-----|-----|--|--|
| Description | Symbol | Min | Max | Min | Max | | |
| Combinatorial Delays: | | | | | | | |
| F/G inputs to X/Y outputs | T _{ILO} | | 3.1 | | | | |
| F/G inputs via H' to X/Y outputs | T _{IHO} | | 5.8 | | | | |
| C inputs via SR through H' to X/Y outputs | T _{HH00} | | 5.3 | | | | |
| C inputs via H' to X/Y outputs | T _{HH10} | | 4.8 | | | | |
| C inputs via DIN through H' to X/Y outputs | T _{HH20} | | 5.8 | | | | |
| CLB Fast Carry Logic: | | | | | | | |
| Operand inputs (F1, F2, G1, G4) to COUT | T _{OPCY} | | 4.5 | | | | |
| Add/Subtract input (F3) to COUT | T _{ASCY} | | 7.4 | | | | |
| Initialization inputs (F1, F3) to COUT | T _{INCY} | | 2.4 | | | | |
| CIN through function generators to X/Y outputs | T _{SUM} | | 5.5 | | | | |
| CIN to COUT, bypass function generators | T _{BYP} | | 1.2 | | | | |
| Sequential Delays: | | | | | | | |
| Clock K to outputs Q | T _{CKO} | | 4.6 | | | | |
| Setup Time before Clock K: | | | | | | | |
| F/G inputs | T _{ICK} | 4.2 | | | | | |
| F/G inputs via H' | T _{IHCK} | 6.9 | | | | | |
| C inputs via H0 through H' | T _{HH0CK} | 6.4 | | | | | |
| C inputs via H1 through H' | T _{HH1CK} | 5.9 | | | | | |
| C inputs via H2 through H' | T _{HH2CK} | 6.9 | | | | | |
| C inputs via DIN | T _{DICK} | 3.0 | | | | | |
| C inputs via EC | T _{ECCK} | 5.8 | | | | | |
| C inputs via S/R, going Low (inactive) | T _{RCK} | 5.9 | | | | | |
| CIN input via F'/G' | T _{CCK} | | | | | | |
| CIN input via F'/G' and H' | T _{CHCK} | | | | | | |
| Hold Time after Clock K: | | | | | | | |
| F/G inputs | T _{CKI} | 0 | | | | | |
| F/G inputs via H' | T _{CKIH} | 0 | | | | | |
| C inputs via H0 through H' | T _{CKHH0} | 0 | | | | | |
| C inputs via H1 through H' | T _{CKHH1} | 0 | | | | | |
| C inputs via H2 through H' | T _{CKHH2} | 0 | | | | | |
| C inputs via DIN | T _{CKDI} | 0 | | | | | |
| C inputs via EC | T _{CKEC} | 0 | | | | | |
| C inputs via S/R, going Low (inactive) | T _{CKR} | 0 | | | | | |
| Clock: | | | | | | | |
| Clock High time | T _{CH} | 5.0 | | | | | |
| Clock Low time | T _{CL} | 5.0 | | | | | |
| Set/Reset Direct: | | | | | | | |
| Width (High) | T _{RPW} | 7.4 | | | | | |
| Delay from C inputs via S/R, going High to Q | T _{RIO} | | 7.4 | | | | |
| Master Set/Reset (Note 1): | | | | | | | |
| Width (High or Low) | T _{MRW} | 18.0 | | | | | |
| Delay from Global Set/Reset net to Q | T _{MRQ} | | 23.8 | | | | |
| Global Set/Reset inactive to first active clock K edge | T _{MRK} | | | | | | |
| Toggle Frequency ² (MHz) | F _{TOG} | | 100 | | | | |
| Preliminary | | | | | | | |

Note: 1. Timing is based on the XC4005L. For other devices see the XACT timing calculator.
2. Export Control Max. flip-flop toggle rate.

XC4000L CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

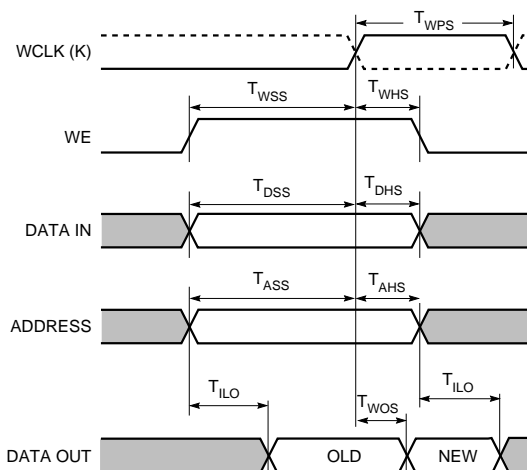
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | | -5 | | -4 | | | |
|--------------------------|------|------------|------|------|-----|-----|--|--|
| Description | Size | Symbol | Min | Max | Min | Max | | |
| Write Operation | | | | | | | | |
| Address write cycle time | 16x2 | T_{WCS} | 20.0 | | | | | |
| (clock K period) | 32x1 | T_{WCTS} | 20.0 | | | | | |
| Clock K pulse width | 16x2 | T_{WPS} | 10.0 | | | | | |
| (active edge) | 32x1 | T_{WPTS} | 10.0 | | | | | |
| Address setup time | 16x2 | T_{ASS} | 5.5 | | | | | |
| before clock K | 32x1 | T_{ASTS} | 5.5 | | | | | |
| Address hold time | 16x2 | T_{AHS} | 0 | | | | | |
| after clock K | 32x1 | T_{AHTS} | 0 | | | | | |
| DIN setup time | 16x2 | T_{DSS} | 5.5 | | | | | |
| before clock K | 32x1 | T_{DSTS} | 5.5 | | | | | |
| DIN hold time | 16x2 | T_{DHS} | 0 | | | | | |
| after clock K | 32x1 | T_{DHTS} | 0 | | | | | |
| WE setup time | 16x2 | T_{WSS} | 4.4 | | | | | |
| before clock K | 32x1 | T_{WSTS} | 4.4 | | | | | |
| WE hold time | 16x2 | T_{WHS} | 0 | | | | | |
| after clock K | 32x1 | T_{WHTS} | 0 | | | | | |
| Data valid | 16x2 | T_{WOS} | | 12.1 | | | | |
| after clock K | 32x1 | T_{WOTS} | | 14.2 | | | | |
| Preliminary | | | | | | | | |

Note 1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

Note 2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.



X6461

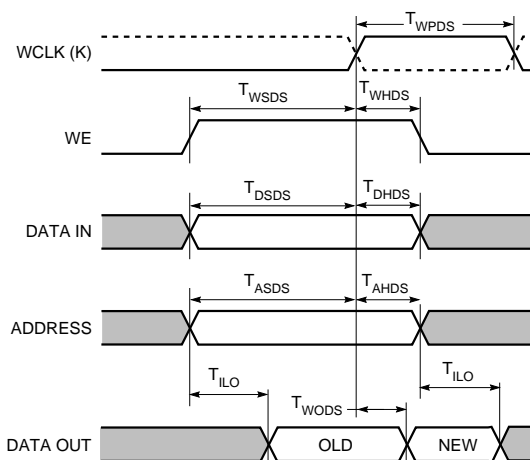
XC4000L CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | | -5 | | -4 | | | |
|--|------|------------|------|------|-----|-----|--|--|
| Description | Size | Symbol | Min | Max | Min | Max | | |
| Write Operation | | | | | | | | |
| Address write cycle time (clock K period) | 16x1 | T_{WCDS} | 20.0 | | | | | |
| Clock K pulse width (active edge) | 16x1 | T_{WPDS} | 10.0 | | | | | |
| Address setup time before clock K | 16x1 | T_{ASDS} | 5.5 | | | | | |
| Address hold time after clock K | 16x1 | T_{AHDS} | 5.5 | | | | | |
| DIN setup time before clock K | 16x1 | T_{DSDS} | 5.5 | | | | | |
| DIN hold time after clock K | 16x1 | T_{DHDS} | 0 | | | | | |
| WE setup time before clock K | 16x1 | T_{WSDS} | 4.4 | | | | | |
| WE hold time after clock K | 16x1 | T_{WHDS} | 0 | | | | | |
| Data valid after clock K | 16x1 | T_{WODS} | | 12.3 | | | | |
| Preliminary | | | | | | | | |

Note: Applicable Read timing specifications are identical to 16x2 Level-Sensitive Read timing.



X6474

XC4000L CLB Level-Sensitive RAM Switching Characteristic Guidelines

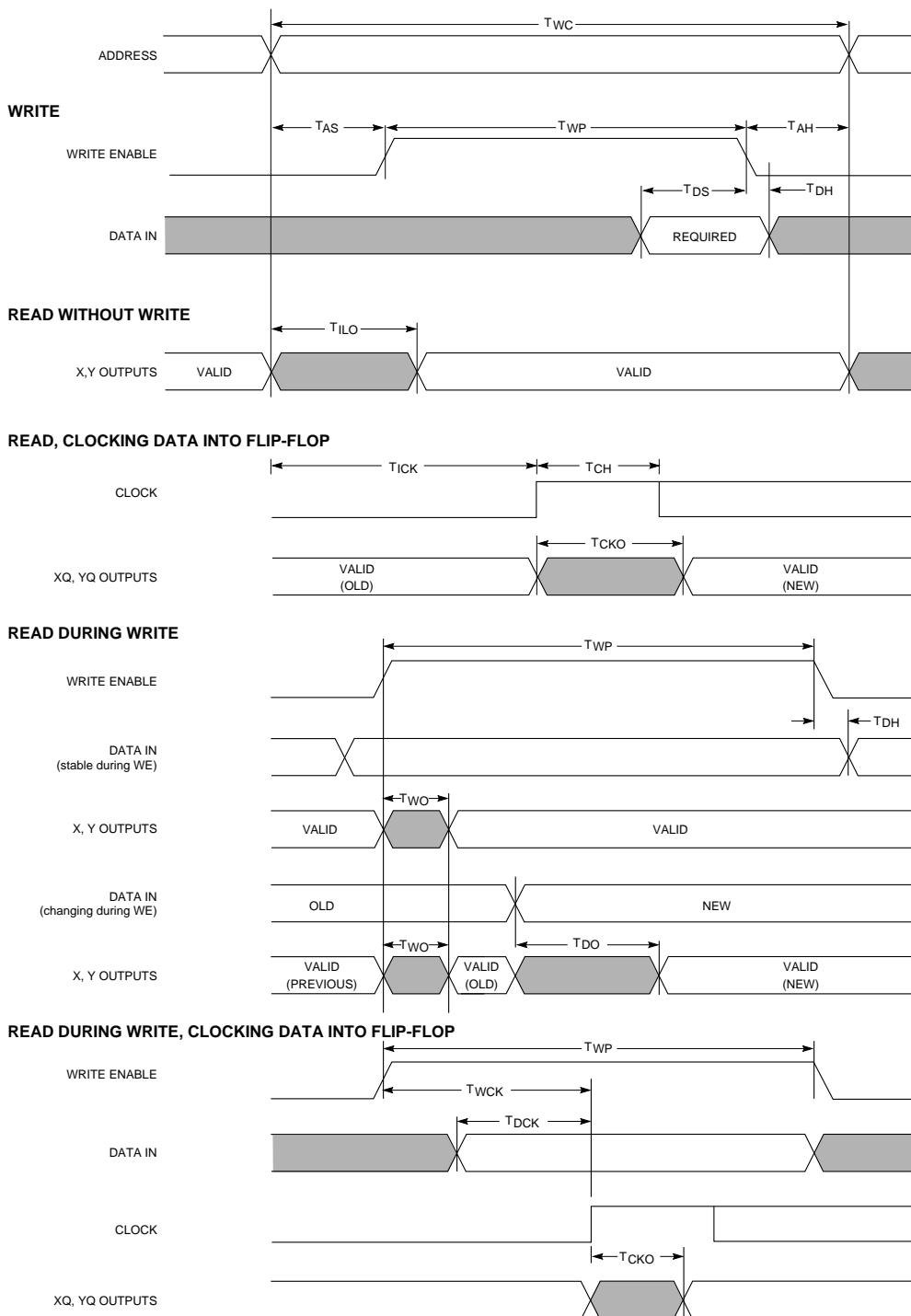
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | | -5 | | -4 | | | |
|--|------|------------|------|------|-----|-----|--|--|
| Description | Size | Symbol | Min | Max | Min | Max | | |
| Write Operation | | | | | | | | |
| Address write cycle time | 16x2 | T_{WC} | 12.0 | | | | | |
| | 32x1 | T_{WCT} | 12.0 | | | | | |
| Write Enable pulse width (High) | 16x2 | T_{WP} | 8.0 | | | | | |
| | 32x1 | T_{WPT} | 8.0 | | | | | |
| Address setup time before WE | 16x2 | T_{AS} | 2.0 | | | | | |
| | 32x1 | T_{AST} | 2.0 | | | | | |
| Address hold time after end of WE | 16x2 | T_{AH} | 2.0 | | | | | |
| | 32x1 | T_{AHT} | 2.0 | | | | | |
| DIN setup time before end of WE | 16x2 | T_{DS} | 4.0 | | | | | |
| | 32x1 | T_{DST} | 5.0 | | | | | |
| DIN hold time after end of WE | 16x2 | T_{DH} | 2.0 | | | | | |
| | 32x1 | T_{DHT} | 2.0 | | | | | |
| Read Operation | | | | | | | | |
| Address read cycle time | 16x2 | T_{RC} | 3.1 | | | | | |
| | 32x1 | T_{RCT} | 5.8 | | | | | |
| Data valid after address change (no Write Enable) | 16x2 | T_{ILO} | | 3.1 | | | | |
| | 32x1 | T_{IHO} | | 5.8 | | | | |
| Read Operation, Clocking Data into Flip-Flop | | | | | | | | |
| Address setup time before clock K | 16x2 | T_{ICK} | 4.2 | | | | | |
| | 32x1 | T_{IHCK} | 6.9 | | | | | |
| Read During Write | | | | | | | | |
| Data valid after WE goes active (DIN stable before WE) | 16x2 | T_{WO} | | 11.7 | | | | |
| | 32x1 | T_{WOT} | | 14.3 | | | | |
| Data valid after DIN (DIN changes during WE) | 16x2 | T_{DO} | | 10.1 | | | | |
| | 32x1 | T_{DOT} | | 12.7 | | | | |
| Read During Write, Clocking Data into Flip-Flop | | | | | | | | |
| WE setup time before clock K | 16x2 | T_{WCK} | 12.2 | | | | | |
| | 32x1 | T_{WCKT} | 14.8 | | | | | |
| Data setup time before clock K | 16x2 | T_{DCK} | 9.3 | | | | | |
| | 32x1 | T_{DCKT} | 11.9 | | | | | |
| Preliminary | | | | | | | | |

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

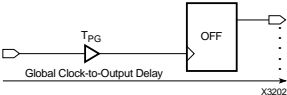
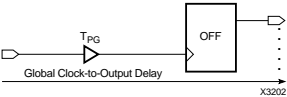
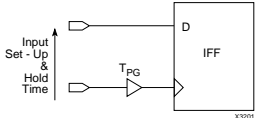
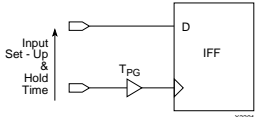
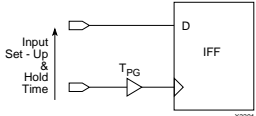
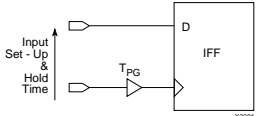
XC4000L CLB Level-Sensitive RAM Timing Characteristics



X2640

XC4000L Guaranteed Input and Output Parameters (Pin-to-Pin, CMOS Inputs)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored.

| Description | Speed Grade | | -5 | -4 | Units |
|---|----------------------|-------------------------------|----------------------|----|----------------|
| | Symbol | Device | | | |
| Global Clock to Output (fast) using OFF | T_{ICKOF} (Max) | XC4005L XC4010L XC4013L | 15.7 17.1 20.0 | | ns ns ns |
|  | | | | | |
| Global Clock to Output (slew-limited) using OFF | T_{ICKO} (Max) | XC4005L XC4010L XC4013L | 19.5 21.3 25.0 | | ns ns ns |
|  | | | | | |
| Input Setup Time, using IFF (no delay) | T_{PSUF} (Min) | XC4005L XC4010L XC4013L | 0 0 0 | | ns ns ns |
|  | | | | | |
| Input Hold Time, using IFF (no delay) | T_{PHF} (Min) | XC4005L XC4010L XC4013L | 2.7 3.7 4.5 | | ns ns ns |
|  | | | | | |
| Input Setup Time, using IFF (with delay) | T_{PSU} (Min) | XC4005L XC4010L XC4013L | 6.9 7.6 9.0 | | ns ns ns |
|  | | | | | |
| Input Hold Time, using IFF (with delay) | T_{PH} (Min) | XC4005L XC4010L XC4013L | 0 0 0 | | ns ns ns |
|  | | | | | |

OFF = Output Flip-Flop

IFF = Input Flip-Flop or Latch

Preliminary

XC4000L IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | | -5 | | -4 | | | |
|--|--------------|-------------|-------------|------|-----|-----|--|--|
| Description | Symbol | Device | Min | Max | Min | Max | | |
| Propagation Delays (CMOS Inputs) | | | | | | | | |
| Pad to I1, I2 | T_{PIDC} | All devices | | 3.7 | | | | |
| Pad to I1, I2 via transparent latch, no delay | T_{PLIC} | All devices | | 7.7 | | | | |
| with delay | T_{PDLIC} | XC4005L | | 15.1 | | | | |
| | | XC4010L | | 16.4 | | | | |
| | | XC4013L | | 20.0 | | | | |
| Propagation Delays (CMOS Inputs) | | | | | | | | |
| Clock (IK) to I1, I2 (flip-flop) | T_{IKRI} | All devices | | 7.0 | | | | |
| Clock (IK) to I1, I2 (latch enable, active Low) | T_{IKLI} | All devices | | 7.3 | | | | |
| Hold Times (Note 1) | | | | | | | | |
| Pad to Clock (IK), no delay | T_{IKPI} | All devices | 0 | | | | | |
| Pad to Clock (IK), with delay | T_{IKPID} | All devices | 0 | | | | | |
| Clock Enable (EC) to Clock (IK), no delay | T_{IKEC} | All devices | 0 | | | | | |
| with delay | T_{IKECD} | All devices | 0 | | | | | |
| Setup Times (CMOS Inputs) | | | | | | | | |
| Pad to Clock (IK), no delay | T_{PICKC} | All devices | 3.7 | | | | | |
| with delay | T_{PICKDC} | XC4005L | 11.1 | | | | | |
| | | XC4010L | 12.4 | | | | | |
| | | XC4013L | 16.0 | | | | | |
| Setup Times (CMOS Inputs) | | | | | | | | |
| Clock Enable (EC) to Clock (IK), no delay | T_{ECIK} | All devices | 5.5 | | | | | |
| with delay | T_{ECIKD} | XC4005L | 12.8 | | | | | |
| | | XC4010L | 14.1 | | | | | |
| | | XC4013L | 18.0 | | | | | |
| Global Set/Reset (Note 3) | | | | | | | | |
| Delay from GSR net through Q to I1, I2 | T_{RRI} | | | 12.2 | | | | |
| GSR width | T_{MRW} | | 18.2 | | | | | |
| GSR inactive to first active Clock (IK) edge | T_{MRI} | | | | | | | |
| | | | Preliminary | | | | | |

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005L. For other devices see the XACT timing calculator.

XC4000L IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | -5 | | -4 | | | |
|--|--------------|-------------|------|-----|-----|--|--|
| Description | Symbol | Min | Max | Min | Max | | |
| Propagation Delays (CMOS Output Levels) | | | | | | | |
| Clock (OK) to Pad, fast | T_{OKPOFC} | | 8.9 | | | | |
| slew-rate limited | T_{OKPOSC} | | 13.5 | | | | |
| Output (O) to Pad, fast | T_{OPFC} | | 8.7 | | | | |
| slew-rate limited | T_{OPSC} | | 13.4 | | | | |
| 3-state to Pad hi-Z (slew-rate independent) | T_{TSHZC} | | 9.5 | | | | |
| 3-state to Pad active and valid, fast | T_{TSOFC} | | 11.1 | | | | |
| slew-rate limited | T_{TSOFC} | | 15.7 | | | | |
| Setup and Hold | | | | | | | |
| Output (O) to clock (OK) setup time | T_{OOK} | 8.1 | | | | | |
| Output (O) to clock (OK) hold time | T_{OKO} | 0 | | | | | |
| Clock Enable (EC) to clock (OK) setup time | T_{ECOK} | 7.6 | | | | | |
| Clock Enable (EC) to clock (OK) hold time | T_{OKEC} | 0 | | | | | |
| Clock | | | | | | | |
| Clock High | T_{CH} | 5.0 | | | | | |
| Clock Low | T_{CL} | 5.0 | | | | | |
| Global Set/Reset (Note 3) | | | | | | | |
| Delay from GSR net to Pad | T_{RPO} | | 15.5 | | | | |
| GSR width | T_{MRW} | 18.0 | | | | | |
| GSR inactive to first active clock (OK) edge | T_{MRO} | | | | | | |
| | | Preliminary | | | | | |

- Note 1: Timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.
- Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
- Note 3: Timing is based on the XC4005L. For other devices see the XACT timing calculator.

XC4000L Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

| Speed Grade | | -5 | | -4 | | | |
|--|--------------|-------------|-----|-----|-----|--|--|
| Description | Symbol | Min | Max | Min | Max | | |
| Setup and Hold | | | | | | | |
| Input (TDI) to clock (TCK) setup time | T_{TDITCK} | | | | | | |
| Input (TDI) to clock (TCK) hold time | T_{TCKTDI} | | | | | | |
| Input (TMS) to clock (TCK) setup time | T_{TMSTCK} | | | | | | |
| Input (TMS) to clock (TCK) hold time | T_{TCKTMS} | | | | | | |
| Propagation Delay | | | | | | | |
| Clock (TCK) to Pad (TDO) | T_{TCKPO} | | | | | | |
| Clock | | | | | | | |
| Clock (TCK) High | T_{TCKH} | | | | | | |
| Clock (TCK) Low | T_{TCKL} | | | | | | |
| Power-On Reset | | | | | | | |
| JTAG operation after valid Vcc | T_{RJTAG} | | | | | | |
| | | Preliminary | | | | | |

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.