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Features

- Mask-programmed versions of Xilinx programmable devices
 - Specifically designed for easy conversions
 - Significant cost reduction for high-volume applications
 - Same specifications and architecture as the programmable devices
 - On-chip scan path test registers
 - High-performance CMOS process
- Easy conversion with guaranteed results
 - "Design Once Methodology" requires no customer engineering resources for conversion
 - Fully pin-for-pin compatible with the programmable device
 - Support for most popular package types
 - PLD database file used to generate production-ready prototypes
 - Automatic test vector generation with >95% fault coverage
 - Prototypes built on production line

The following is an overview of the Xilinx HardWire device product line. Product specifications for the HardWire devices and additional information are available in a separate publication - The HardWire Data Book.

HardWire Arrays are mask-programmed versions of the popular XC2000, XC3000, XC4000, and XC5000 series FPGAs, as well as the XC9500 CPLDs. The HardWire devices provide a transparent migration path from a programmable logic device to a cost-reduced device without the engineering burden associated with conventional gate-array re-design.

In standard programmable logic, the functions and interconnections are determined by configuration data stored in memory cells. In the HardWire components, the memory cells and the logic they control are replaced by metal connections. All other circuitry in the HardWire devices is identical to the corresponding programmable logic's internal circuitry. Thus, a HardWire device is a semicustom device manufactured to provide a specific functionality, yet is completely compatible with the programmable device it replaces.

Advantages of Using Xilinx HardWire Arrays

Xilinx offers an easy, seamless process for achieving the shortest Time-to-Volume solution possible. Simply stated, our unique Design Once methodology allows engineers to develop their design in a programmable device, then switch to a lower cost mask-programmed product without utilizing additional internal resources.

Production is often started using the same programmable logic in which the application was designed. This flexibility allows the product to be introduced to the market quickly. Later in the production process, the PLD can be replaced with a HardWire Array without expending additional engineering time and effort to redesign either the FPGA's circuit or the printed circuit board. Other conversion methodologies introduce risk at each project milestone of the conversion process. Only the Xilinx Design Once Methodology can offer this no risk, 100% pin-for-pin compatible path to dramatic cost reductions.

Whenever a system incorporating Xilinx PLDs ramps to high production volumes, the HardWire mask-programmed solution should be the first consideration for cost reduction. Because the HardWire implementation dramatically reduces the die size by removing programmable elements, the resulting device is much smaller than the equivalent PLD. This smaller die provides a no-risk path to achieve dramatic cost reductions.

HardWire versus Full ASIC Gate Array Implementation

Converting a device from programmable logic to a HardWire Array has many advantages over generic gate array redesign. The most important is that the Xilinx HardWire methodology requires no additional customer engineering to convert the programmable logic design into a fully tested, completely verified mask-programmed design.

This ease of conversion is available only through Xilinx because the PLD database file is the actual physical data base previously created and verified in the process of developing the PLD design. Xilinx has the only methodology that preserves all attributes of the original physical data base file. If the design is mapped to a third party library for conversion at the schematic level to another technology, the design must be verified and prototyped. Third party implementation will change the placement and routing, thereby changing the design's performance characteristics.

Thus, the revised device needs to be re-verified and re-tested in the system to be certain both the functionality and the performance still meet the application's requirements.

A comparison of the activities required to convert a HardWire Array versus a standard array is shown in **Figure 1**.

Reverifying the Design

In conventional gate array conversion (redesign), the design must be re-verified after the schematic is translated or recaptured. The process of reverifying a design is rigorous and time-consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. A suitable test methodology must be considered and implemented.

In contrast, no additional effort is required when converting to Xilinx HardWire Arrays. The HardWire design is self-verifying because the actual PLD database file is used for the conversion.

Fault Coverage and Test Vectors

All designs need to be testable. In a traditional mask-programmed gate array, the designer is required to build in testability and generate test vectors that verify chip performance by exercising as much of the device's circuitry as possible. Most designers strive for greater than 95% fault

coverage. However, they often settle for significantly less because the iterative process is extremely time consuming and increases exponentially as fault coverage is increased.

Any third-party conversion from a Xilinx FPGA or CPLD to a gate array or other similar technology will require test vector generation. Typically, the original designers create the test vectors, since they are most familiar with the design implementation. This method ties up valuable design resources and reverses the value of the original decision to use programmable logic for their ease of design and time-to-market advantages. Another alternative is to contract with the conversion or gate array vendor to create the test vectors. This method can be both time-consuming and expensive, since vendors usually charge by the vector. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts all the liability of determining whether the resulting device is production worthy. In today's competitive market, many projects can not afford the risk of possible respins if the design doesn't work.

Converting from a Xilinx programmable to a HardWire device requires no test vector generation. Xilinx guarantees greater than 95% fault coverage through a proprietary Automatic Test Vector Generation methodology. All HardWire Arrays are 100% fully guaranteed to work in the user's application exactly like the programmable logic.

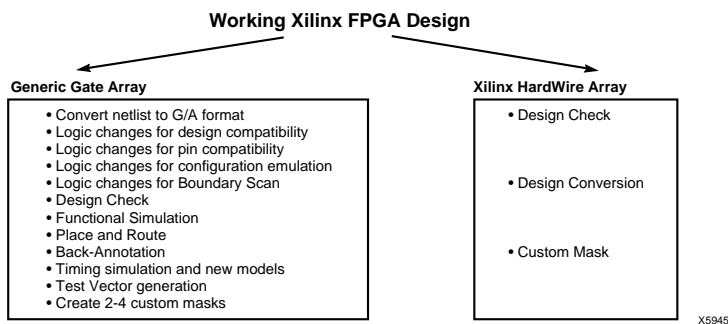


Figure 1: Steps Involved in Converting a PLD Design to a Gate Array as Compared to a Hard Wire Array

Packaging and Silicon Considerations

All of the physical attributes of the HardWire Arrays are virtually identical to the programmable logic devices. Xilinx uses the same qualified fabrication facilities for both the PLD and HardWire devices. The same IC process, as well as packaging, assembly, and test facilities, are used. This allows users to circumvent costly and time-consuming requalification efforts.

Converting from a Xilinx programmable logic device to anything but a Xilinx HardWire Array means a change to silicon, packaging, assembly and test. Each of these changes adds an element of risk into the qualification process.

Support for the Entire Product Life Cycle

Figure 2 shows the typical life cycle of a high-volume product, and illustrates the optimal way for using the programmable and HardWire devices.

During the development, prototype, and initial production stages, the programmable device is the best choice. Later in the life-cycle, when the design is stable and in high volume production, the HardWire Array can be used in place of the original programmable device.

Since the circuit board was designed initially for a programmable device, production can be switched back from the HardWire Array to the programmable device if the situation warrants. For example, if demand for the product increases dramatically, production can be increased in days or weeks

by using programmable devices. In addition, a change can be quickly made to the product, since there is no manufacturing lead-time for an off-the-shelf programmable device. Production can be switched to programmable devices as the product nears the end of the life cycle, avoiding end-of-life buys and the risk of obsolescence.

Furthermore, designs implemented with multiple static RAM-based FPGAs can be cost reduced incrementally, converting one or more of the programmable devices while leaving the others for future conversion. As each PLD is converted to a Xilinx HardWire Array, the user enjoys a lower cost for that unit, while maintaining the ease-of-use of off-the-shelf programmable logic in the other sockets. When all of the devices are converted, the storage element can then be removed, giving even further cost reductions. This flexibility is unique to Xilinx, and allows OEMs to achieve cost reductions quickly with minimal effort.

The HardWire Product Series

As listed in **Table 1**, the HardWire product chart, there is a range of products available for Xilinx FPGAs and XC9500 CPLDs. For designs developed using the Xilinx XC4000 family, there are two HardWire options. The XC4400 family is based on Xilinx advanced technology. It is most beneficial for higher volume applications, as well as XC4000E designs utilizing Xilinx's Select-RAM™ features, and low power 3.3 volt designs. For an application with low annual volumes (as low as 1500 units) and where a low NRE is required, the XC4300 family provides the best fit. Xilinx also supports the low-power 3.3 volt XC2000L and XC3000L.

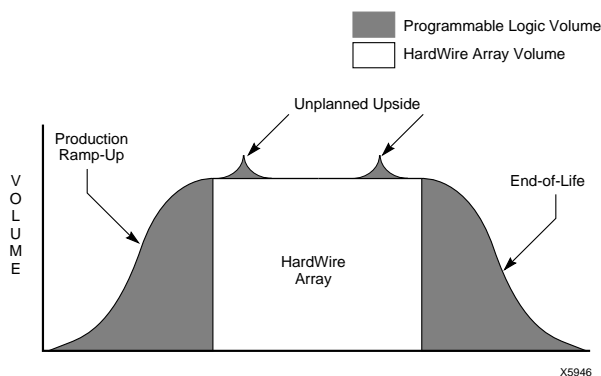


Figure 2: Typical High Volume Product Life Cycle

Table 1: HardWire Product Chart¹

PLD Family	H/W Equivalent	Minimum Order Quantity (KU)	Minimum Shipment (KU)	Production Availability
XC2000	XC2300	7	2	Now
XC3000/A	XC3330	10	2	
XC3100A	XC3342	6	1	
	XC3390	4	0.5	
XC3195	XC4495T	10	2	
XC4000/E ²	XC4303	6	2	
	XC4305	4	1	
	XC4310	1.5	0.4	
	XC4313	1.5	0.4	
	XC4403/H	10	2	
	XC4405/H	10	2	
	XC4406	5	1	
	XC4408	5	1	
	XC4410	5	1	
	XC4413	3.5	0.5	
	XC4425	2.5	0.5	
XC4000EX	XH4028EX	2.5	0.5	Q4/96
	XH4036EX	2.5	0.5	Q4/96
	XH4044EX	2.5	0.5	Q1/97
	XH4052EX	2.5	0.5	Q1/97
	XH4062EX	2.5	0.5	Q1/97
XC5200	XC5402	10	2	Now
	XC5404	10	2	
	XC5406	5	1	
	XC5410	5	1	
	XC5415	3.5	0.5	
XC9500	XC95144	10	10	Q2/97
	XC95180	10	10	
	XC95216	10	10	
	XC95288	10	10	

Notes: 1. Industrial temperature grades are available for all products.

2. The XC4300 supports the XC4000 design features. The XC4400 supports both the XC4000 and XC4000E design features.