

About this Book

This Data Book provides a “snapshot in time” in its listing of IC devices and development system software available from Xilinx as of early 1996. New devices, speed grades, package types and development system products are continually being added to the Xilinx product portfolio. Users are encouraged to contact their local Xilinx sales representative and consult the WebLINX World Wide Web site (<http://www.xilinx.com>) and the quarterly XCELL newsletter for the latest information regarding new product availability.

The product specifications for several older Xilinx FPGA families are not included in this Data Book. This does not imply that these products are no longer available. However, for new designs, users are encouraged to use the newer products described in this book, which offer better performance at lower cost than the older technologies. Product specifications for the older products are available at WebLINX, the Xilinx site on the World Wide Web, or through your local Xilinx sales representative. These products include the following FPGA families: the XC2000, XC3000, XC3100, XC4000, XC4000A, XC4000D, and XC4000H families.

Data Sheet Categories

In order to provide the most up-to-date information, some component products included in this book may not have been fully characterized at the time of publication. In these cases, the AC and DC characteristics included in the data sheets will be marked as *Advance* or *Preliminary* information. (Not withstanding the definitions of such terms, all specifications are subject to change without notice.) These designations have the following meaning:

- **Advance** — Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, but not for final production.
- **Preliminary** — Based on preliminary characterization. Changes are possible, but not expected.
- **Final (unmarked)** — Specifications not identified as either Advance or Preliminary are to be considered final.

Data Book Contents

Chapter 1 is a general overview of the Xilinx product line, and is recommended reading for designers who are new to the field of high-density programmable logic.

Chapter 2 contains a discussion of the overall design methodology when using Xilinx programmable logic and descriptions of Xilinx development system products. This chapter is placed at the beginning of the book since these development tools are needed to design with any of the Xilinx programmable logic devices.

Chapter 3 contains the product descriptions for the Xilinx Complex Programmable Logic Device (CPLD) products, including the XC7000 and XC9000 series.

Chapter 4 includes the product descriptions for the Xilinx static-memory-based Field Programmable Gate Array (FPGA) products, including the XC3000, XC4000, XC5000, and XC6000 series.

Chapter 5 holds the product descriptions for the XC1700 family of Serial PROM devices. These Serial PROMs provide a convenient, low-cost means of storing configuration programs for the SRAM-based FPGAs described in Chapter 4.

Chapter 6 is an overview of Xilinx components appropriate for 3.3 V and mixed-voltage systems. This chapter will refer you back to the appropriate product descriptions in the earlier chapters.

Chapter 7 contains a brief overview of the HardWire product line. Detailed product specifications are available in separate Xilinx data sheets.

Chapter 8 is an overview of Xilinx High-Reliability/Military products. Detailed product specifications are available in separate Xilinx data sheets.

Chapter 9 describes the HW130 device programmer for the XC1700 series of Serial PROMs and the XC7000 and XC9000 series of CPLDs.

Chapter 10 contains a description of all the physical packages for the various IC products, including information about the thermal characteristics of those packages.

Chapter 11 discusses the testing, quality, and reliability of Xilinx component products.

Chapter 12 includes a listing of all the technical support facilities provided by Xilinx.

Chapter 13 contains additional information about Xilinx components that is not provided in the product specifications of the earlier chapters. This includes some additional electrical parameters that are not in the product specifications because they are not part of the manufacturing test program for the particular device, but may be of interest to the user. Also included in this chapter is a discussion of the

JTAG boundary test scan logic found in several Xilinx component families.

The final two sections contain an index to the topics included in this Data Book and a listing of Xilinx sales offices, sales representatives, and distributors.

About the Company

Xilinx, Inc., offers the industry's broadest selection of programmable logic devices. With 1995 revenues of over \$500 million, Xilinx is the world's largest supplier of programmable logic, and the market leader in Field Programmable Gate Arrays (FPGAs).

Xilinx was founded in 1984, based on the revolutionary idea of combining the logic density and versatility of gate arrays with the time-to-market advantages and convenience of user-programmable standard parts. One year later, Xilinx introduced the world's first Field Programmable Gate Array. Since then, through a combination of architectural and manufacturing process improvements, the company has continually increased device performance, in terms of capacity, speed, and ease-of-use, while lowering costs.

In 1992, Xilinx expanded its product line to include advanced Complex Programmable Logic Devices (CPLDs, also known as EPLDs). For the user, CPLDs are an attractive complement to FPGAs, offering simpler design software and more predictable timing.

As the market leader in one of the fastest growing segments of the semiconductor industry, Xilinx strategy is to focus its resources on creating new ICs and development system software, providing world-class technical support, developing markets, and building a diverse customer base across a broad range of geographic and end-use application segments. The company has avoided the large capital commitment and overhead burden associated with sole ownership and operation of a wafer fabrication facility. Instead, Xilinx has established alliances with several high-volume, state-of-the-art CMOS IC manufacturers. Using standard, high-volume processes assures low manufacturing costs, produces programmable logic devices with well-established reliability, and provides for early access to advances in CMOS processing technology.

Xilinx headquarters are located in San Jose, California. The company markets its products worldwide through a network of direct sales offices, manufacturers' representatives, and distributors (as listed in the back of this book). The company has representatives and distributors in over 38 countries.

Product Line Overview

Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) can be used in virtually any digital logic system. Over 35 million Xilinx components have been used in a wide variety of end-equipment applications, ranging from supercomputers to hand-held



instruments, from central office switches to centrifuges, and from missile guidance systems to guitar synthesizers.

Xilinx achieved its leading position through a continuing commitment to provide a complete product solution. This encompasses a focus on all three critical areas of the high-density programmable solution “triangle”: components (silicon), software, and service (**Figure 1**).

Programmable Logic vs. Gate Arrays

Xilinx programmable logic devices provide the benefits of high integration levels without the risks or expenses of semi-custom and custom IC development. Some of the benefits of programmable logic as versus mask-programmed gate arrays are briefly discussed below.

Faster Design and Verification

Xilinx FPGAs and CPLDs can be designed and verified quickly while the same process requires several weeks with gate arrays. There are no non-recurring engineering (NRE) costs, no test vectors to generate, and no delay while waiting for prototypes to be manufactured.

Design Changes without Penalty

Because the devices are software-configured and user-programmed, modifications are much less risky and can be made anytime - in a manner of minutes or hours, as opposed to the weeks it would take with a gate array. This results in significant cost savings in design and production.

Shortest Time-to-Market

When designing with Xilinx programmable logic, time-to-market is measured in days or a few weeks, not the months often required when using gate arrays. A study by market research firm McKinsey & Co. concluded that a six-month delay in getting to market can cost a product one-third of its

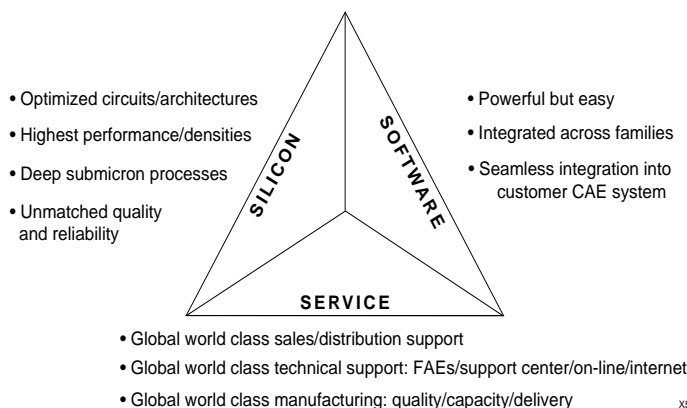
lifetime potential profit. With mask-programmed gate arrays, design iterations can easily add that much time, and more, to a product schedule.

Once the decision has been made to use Xilinx programmable logic, a choice must be made from a number of product families, device options, and product types. The information in the product selection matrices that follow can help guide that selection; detailed product specifications are available in subsequent chapters of this book. Since many component products are available in common packages with common footprints, designs often can be migrated to higher or lower density devices, or even across some product families, without any printed circuit board changes. Design ideas, represented in text or schematic format, are converted into a configuration data file for an FPGA or CPLD device using the Xilinx XACT^{step} development software running on a PC or workstation.

Component Products

Xilinx offers the broadest line of programmable logic devices available today, with hundreds of products featuring various combinations of architectures, logic densities, package types, and speed grades in commercial, industrial, and military grades. This breadth of product offerings allows the selection of the programmable logic device that is best suited for the target application.

Xilinx programmable logic offerings include several families of reprogrammable FPGAs, one-time-programmable FPGAs, EPROM-based CPLDs, and FLASH-memory-based CPLDs (**Figure 2**). HardWire devices are mask-programmed versions of the reprogrammable FPGAs, and provide a transparent, no-risk migration path to lower-cost devices for high-volume, stable designs. Additionally, a family of Serial PROM devices is available to store configuration programs for the reprogrammable FPGA devices.



X5955

Figure 1: The Xilinx Programmable Solution Triangle

Many devices are available in military temperature range and/or MIL-STD-883B versions, for high-reliability and military applications.

Field Programmable Gate Arrays (FPGAs)

FPGA devices feature a gate-array-like architecture, with a matrix of logic cells surrounded by a periphery of I/O cells, as diagrammed in **Figure 3**. Segments of metal interconnect can be linked in an arbitrary manner by programmable switches to form the desired signal nets between the cells.

FPGAs combine an abundance of logic gates, registers, and I/Os with fast system speed. Xilinx offers several families of reprogrammable, static-memory-based (SRAM-based) FPGAs, including the XC2000, XC3000, XC4000, XC5000, and XC6000 series.

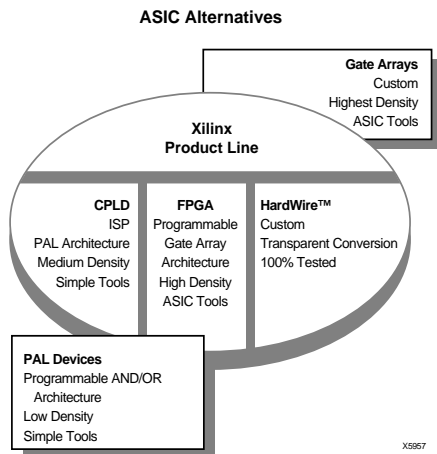


Figure 2: Application-Specific IC Products

Complex Programmable Logic Devices (CPLDs)

Designers more comfortable with the speed, design simplicity, and predictability of PALs may prefer CPLD devices. Conceptually, CPLDs consist of multiple PAL-like function blocks that can be interconnected through a switch matrix (**Figure 4**). The Xilinx XC7000 CPLD series is based on EPROM technology. The new XC9000 CPLD series features 5V in-system programmable FLASH technology, and, like most of the FPGA families, includes built-in JTAG boundary scan test logic.

HardWire devices

HardWire devices are masked-programmed versions of the SRAM-based FPGAs. The HardWire products provide an easy, transparent migration path to a cost-reduced device without the engineering burden associated with conventional gate array re-design. The HardWire gate array is architecturally identical to its FPGA counterpart, but the programmable elements in the FPGA are replaced with fixed metal connections. The resulting die is considerably smaller, with a correspondingly lower cost. Using proprietary automatic test vector generation software and patented test logic, Xilinx guarantees over 95% fault coverage, while eliminating the need for user-generated test vectors. The mask and test programs are generated automatically by Xilinx from the user's existing FPGA design file.

Serial PROMs

The XC1700 family features one-time programmable serial PROMs ranging in density from about 18,000 bits to over 260,000 bits. These serial PROMs are an easy-to-use, cost-effective method for storing configuration data for the SRAM-based FPGAs.

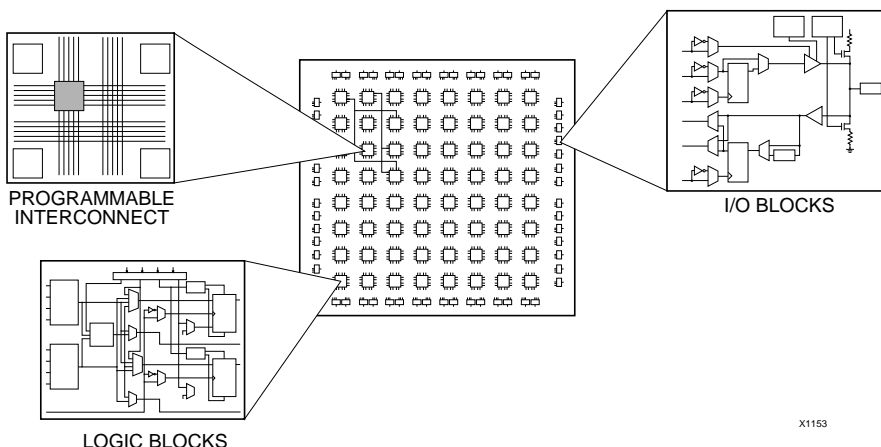


Figure 3: FPGA Architecture

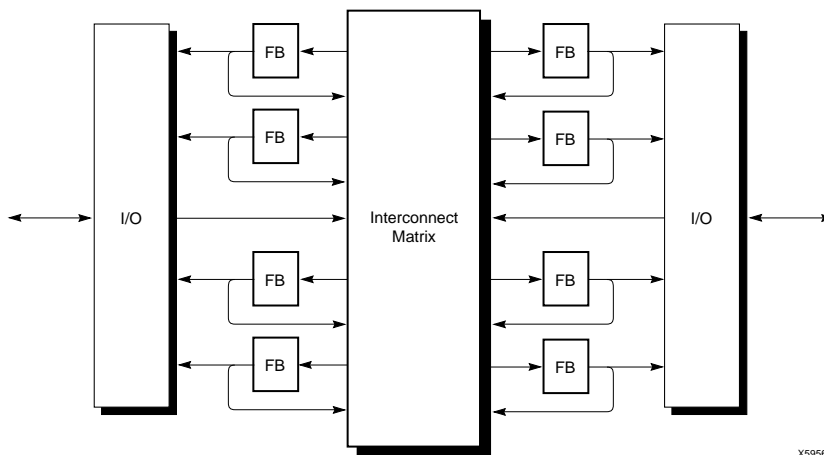


Figure 4: CPLD Architecture

High-Reliability Devices

Xilinx was the first company to offer high-reliability FPGAs by introducing MIL-STD-883B qualified XC2000 and XC3000 series devices in 1989. MIL-STD-883B members of the XC4000 FPGA series also are available, and qualified versions of additional Xilinx families are in development. The product line also includes Standard Microcircuit Drawing (SMD) versions of several families. Some Xilinx devices are available in tested die form through arrangements with manufacturing partners.

Development System Products

Xilinx offers a complete software environment for the implementation of logic designs in Xilinx programmable logic devices. This environment, called *XACTstep*, combines powerful technology with a flexible, easy-to-use graphical interface to help users achieve the best possible designs, regardless of experience level. The user has a wide range of choices between a fully-automatic implementation and detailed involvement in the layout process. The *XACTstep* system provides all the implementation tools required to design with Xilinx logic devices, including the following:

- libraries and interfaces for popular schematic editors, logic synthesis tools, and simulators
- design manager/flow engine
- module generator
- map, place, and route compilation software
- graphical floorplanner
- static timing analyzer
- hardware debugger

Xilinx is committed to an “open system” approach to front-end design creation, synthesis, and verification. Xilinx devices are supported by the broadest number of EDA vendors and synthesis vendors in the industry. Supported platforms include the ubiquitous PC and several popular workstations.

Service

Providing global, world-class manufacturing, technical support, and sales/distribution support is an essential foundation of the Xilinx product strategy. Xilinx manufacturing facilities have earned ISO9002 certification, and Xilinx quality and reliability achievements are among the world's best - not just for programmable logic suppliers, but among all semiconductor companies. Comprehensive technical support facilities include training courses, extensive product documentation and application notes, a quarterly technical newsletter, automated document servers, a technical bulletin board, the WebLINX World Wide Web site, technical support hotlines, and a cadre of Field Application Engineers. Sales support is provided by a worldwide network of representatives and distributors.

FPGA Product Selection Matrix

DEVICES	XC3000 Series	XC3020A/L	XC3030A/L	XC3042A/L	XC3064A/L	XC3090A/L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC3142L	XC3190L
KEY FEATURES		Low Cost/ Low Power					Highest Performance						Low Voltage (3.3 V) Highest Performance	
DENSITY	Max Logic Gates (K)	1.5	2	3	5	6	1.5	2	3	5	6	8	3	6
	Max RAM Bits	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Typical Gate Range (K)	1-1.5	1.5-2	2-3	4-5	5-6	1-1.5	1-2	2-3	4-5	5-6	7-8	2-3	5-6
	CLBs	64	100	144	224	320	64	100	144	224	320	484	144	320
	Flip-Flops	256	360	480	688	928	256	360	480	688	928	1320	480	928
FEATURES	Output Drive (mA)	4	4	4	4	4	8	8	8	8	8	8	4	4
	JTAG (IEEE 1149.1)	N	N	N	N	N	N	N	N	N	N	N	N	N
	Dedicated Arithmetic	N	N	N	N	N	N	N	N	N	N	N	N	N
	Quiescent Current (mA)	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	0.5/ 0.02	8	8	8	8	8	8	1.5	1.5
PERFORMANCE	Fastest Speed Grade	-6/-8	-6/-8	-6/-8	-6/-8	-6/-8	-09	-09	-09	-09	-09	-09	-2	-2
	Shift Register (MHz)	124/69	124/69	124/69	124/69	124/69	312	312	312	312	312	312	256	256
	Small State Machine (MHz)	42/23	42/23	42/23	42/23	42/23	112	112	112	112	112	112	68	68
	Large State Machine (MHz)	21/14	21/14	21/14	21/14	21/14	55	55	55	55	55	55	33	33
	4-Bit Multiply-Accumulator (MHz)	20/12	20/12	20/12	20/12	20/12	51	51	51	51	51	51	33	33
	16-Bit Accumulator (MHz)	25/15	25/15	25/15	25/15	25/15	58	58	58	58	58	58	41	41
	Address Map Decoder (MHz)	52/27	52/27	52/27	52/27	52/27	127	127	127	127	127	127	84	84
	Data Path (MHz)	147/86	147/86	147/86	147/86	147/86	335	335	335	335	335	335	84	84
	Counter Timer (MHz)	37/23	37/23	37/23	37/23	37/23	81	81	81	81	81	81	56	56
	16-Bit Non Loadable Counter (MHz)	135/81	135/81	135/81	135/81	135/81	370	370	370	370	370	370	323	323
	16-Bit Loadable Binary Up Counter (MHz)	39/25	39/25	39/25	39/25	39/25	91	91	91	91	91	91	63	63
	16-Bit Loadable Prescaled Counter (MHz)	100/59	100/59	100/59	100/59	100/59	228	228	228	228	228	228	154	154
	RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	Pad to Setup (ns)	14/12	14/12	14/12	14/12	14/12	2.5	2.5	2.5	2.5	2.5	2.5	4	4
	Clock to Pad (ns)	7/18	7/18	7/18	7/18	7/18	4	4	4	4	4	4	5	5
	Combinatorial Pad to Pad (ns)	14/25	14/25	14/25	14/25	14/25	6	6	6	6	6	6	8	8

FPGA Product Selection Matrix (continued)

DEVICES	XC4000 Series															XC4003E*	XC4005E*	XC4006E*	XC4008E*	XC4010E*	XC4013E*	XC4020E*	XC4025E*	XC4028EX	XC4036EX	XC4044EX	XC4052XL	XC4062XL	XC4003H	XC4005H	XC4005L	XC4010L	XC4013L
KEY FEATURES	High Density High Performance Select-RAM™ Memory															High I/O		Low Voltage (3 V)															
DENSITY	Max Logic Gates, (no RAM) (K)	3	5	6	8	10	13	20	25	28	36	44	52	62	3	5	5	10	13														
	Max RAM Bits (no Logic)	3200	6272	8192	10368	12800	18342	25088	32768	32768	41472	51200	61952	73728	3200	6272	6272	12800	18432														
	Typical Gate Range (Logic and RAM) (K)	2-5	3-9	4-12	6-15	7-20	10-30	13-40	15-45	18-50	22-65	27-80	33-100	40-130	2-5	3-9	3-9	7-20	10-30														
	CLBs	100	196	256	324	400	576	784	1024	1024	1296	1600	1936	2304	100	196	196	400	576														
	Flip-Flops	360	616	768	936	1120	1536	2016	2560	2560	3168	3840	4576	5376	200	392	616	1120	1536														
FEATURES	Output Drive (mA)	12	12	12	12	12	12	12	12	12	12	12	12	12	24	24	4	4	4														
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y														
	Dedicated Arithmetic	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y														
	Quiescent Current (mA)	10	10	10	10	10	10	10	10	10	10	10	10	10	10	10	0.05	0.05	0.05														
PERFORMANCE	Fastest Speed Grade	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-5	-5	CONTACT FACTORY																
	Shift Register (MHz)	190	190	190	190	190	190	190	190	190	190	190	190	190	105	105																	
	Small State Machine (MHz)	69	69	69	69	69	69	69	69	69	69	69	69	69	48	48																	
	Large State Machine (MHz)	43	43	43	43	43	43	43	43	43	43	43	43	43	37	37																	
	4-Bit Multiply-Accumulator (MHz)	39	39	39	39	39	39	39	39	39	39	39	39	39	20	20																	
	16-Bit Accumulator (MHz)	65	65	65	65	65	65	65	65	65	65	65	65	65	36	36																	
	Address Map Decoder (MHz)	71	71	71	71	71	71	71	71	71	71	71	71	71	43	43																	
	Data Path (MHz)	156	156	156	156	156	156	156	156	156	156	156	156	156	105	105																	
	Counter Timer (MHz)	117	117	117	117	117	117	117	117	117	117	117	117	117	58	58																	
	16-Bit Non Loadable Counter (MHz)	180	180	180	180	180	180	180	180	180	180	180	180	180	95	95																	
	16-Bit Loadable Binary Up Counter (MHz)	87	87	87	87	87	87	87	87	87	87	87	87	87	42	42																	
	16-Bit Loadable Prescaled Counter (MHz)	115	115	115	115	115	115	115	115	115	115	115	115	115	63	63																	
	RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	50		50															
	Pad to Setup (ns)	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	7	7																	
	Clock to Pad (ns)	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	6.5	10	10																	
Combinatorial Pad to Pad (ns)	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	10.5	5	5																		

*Usable gates assume 20% of CLBs used as RAM

DEVICES	XC5000, XC6000 Series										XC5202	XC5204	XC5206	XC5210	XC5215	XC6209	XC6216	XC6236	XC6264
KEY FEATURES	High Density Low Cost										µP Interface Fast Configuration								
DENSITY	Max Logic Gates (K)	3	6	10	16	23	13	24	55	100									
FEATURES	Max RAM Bits	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A									
	Typical Gate Range (K)	2-3	4-6	6-10	10-16	15-23	9-13	16-24	36-55	64-100									
PERFORMANCE	CLBs/Logic Cells	64	120	196	324	484	2304	4096	9216	16384									
	Flip-Flops	256	480	784	1296	1936	2304	4096	9216	16384									
PERFORMANCE	Output Drive (mA)	8	8	8	8	8	8	8	8	8									
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	N	N	N	N									
PERFORMANCE	Dedicated Arithmetic	Y	Y	Y	Y	Y	N	N	N	N									
	Quiescent Current (mA)	15	15	15	15	15	-	-	-	-									
PERFORMANCE	Fastest Speed Grade	-4	-4	-4	-4	-4													
	Shift Register (MHz)	83	83	83	83	83													
PERFORMANCE	Small State Machine (MHz)	50	50	50	50	50													
	Large State Machine (MHz)	35	35	35	35	35													
PERFORMANCE	4-Bit Multiply-Accumulator (MHz)	24	24	24	24	24													
	16-Bit Accumulator (MHz)	60	60	60	60	60													
PERFORMANCE	Address Map Decoder (MHz)	69	69	69	69	69													
	Data Path (MHz)	83	83	83	83	83													
PERFORMANCE	Counter Timer (MHz)	59	59	59	59	59													
	16-Bit Non Loadable Counter (MHz)	N/A	N/A	N/A	N/A	N/A													
PERFORMANCE	16-Bit Loadable Binary Up Counter (MHz)	58	58	58	58	58													
	16-Bit Loadable Prescaled Counter (MHz)	83	83	83	83	83													
PERFORMANCE	RAM Read Modify Write (MHz)	N/A	N/A	N/A	N/A	N/A													
	Pad to Setup (ns)	6.6	6.6	6.6	6.6	6.6													
PERFORMANCE	Clock to Pad (ns)	14.2	14.2	14.2	14.2	14.2													
	Combinatorial Pad to Pad (ns)	15	15	15	15	15													

*Usable gates assume 20% of CLBs used as RAM

CPLD Product Selection Matrix

DEVICES	CPLD Families	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC9572	XC95108	XC95144	XC95180	XC95216	XC95288	XC95432	XC95576
KEY FEATURES		100% Routable 100% Utilization 5 ns T _{PD}							JTAG 5 V ISP 3 V or 5 V I/O								
DENSITY	Gates (K)	0.4	0.8	0.8	1.5	1.9	3.0	3.8	0.8	1.6	2.4	3.2	4.0	4.8	6.4	9.6	12.8
	Macrocells	18	36	36	54	72	108	144	36	72	108	144	180	216	288	432	576
	Flip-Flops	18	36	36	108	126	198	234	36	72	108	144	180	216	288	432	576
FEATURES	Output Drive (mA)	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24	24
	JTAG (IEEE 1149.1)	N	N	N	N	N	N	N	Y	Y	Y	Y	Y	Y	Y	Y	Y
	Dedicated Arithmetic	N	N	N	Y	Y	Y	Y	N	N	N	N	N	N	N	N	N
	Quiescent Current (mA)	90	126	50	140	187	227	250	–	–	140	–	–	–	–	–	–
	Fastest Speed Grade	-5	-5	-10	-7	-7	-7	-7	-5	-7	-7	-7	-10	-10	-10	–	–
PERFORMANCE	Shift Register (MHz)	125	125		95	95	95	95	CONTACT FACTORY								
	Small State Machine (MHz)	108	108		95	95	95	95									
	Large State Machine (MHz)	102	102		95	95	95	95									
	4-Bit Multiply-Accumulator (MHz)	46	46		52	52	52	52									
	16-Bit Accumulator (MHz)	40	40		63	63	63	63									
	Address Map Decoder (MHz)	108	108		95	95	95	95									
	Data Path (MHz)	125	125		95	95	95	95									
	Counter Timer (MHz)	94	94		47	47	47	47									
	16-Bit Non Loadable Counter (MHz)	125	125		95	95	95	95									
	16-Bit Loadable Binary Up Counter (MHz)	125	125		95	95	95	95									
	16-Bit Loadable Prescaled Counter (MHz)	125	125		95	95	95	95									
	RAM Read Modify Write (MHz)	N/A	N/A		N/A	N/A	N/A	N/A									
	Pad to Setup (ns)	3.5	3.5		4	4	4	4									
	Clock to Pad (ns)	4.5	4.5		7	7	7	7									
	Combinatorial Pad to Pad (ns)	5	5		7	7	7	7									

		Number of Pins																	
PACKAGE OPTIONS AND USER I/O Package (Code)	MAX I/O		38	38	38	58	84	120	156	34	72	108	133	168	168	192	232	232	
	PLCC (PC)	44	38	38	38	38				34									
	PQFP (PQ)	44	38	38	38	38				34									
	CLCC (WC)	44		38	38	38													
	VQFP (VQ)	44			38														
	PLCC (PC)	68				58	57												
	CLCC (WC)	68				58	57												
	PLCC (PC)	84					72	72			69	69							
	CLCC (WC)	84					72	72											
	PGC (PG)	84																	
	PQFP (PQ)	100					84	84			72	81	81						
	TQFP (TQ)	100									72	81							
	PGA (PG)	144						120											
	PQFP (PQ)	160						120	136			108	133	133	133				
	HQFP (HQ)	208												168	168	168			
	BGA (BG)	225						120	156								192	232	232
	HQFP (HQ)	304																	