

August 6, 1996 (Version 1.2)

## Number of Available I/O Pins

	Max I/O	44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	225	228	240	299	304	352	411	432	499
XC7236A	36	36																									
XC7272A	72			56	72																						
XC7318	38	38																									
XC7336	38	38																									
XC7336Q	38	38																									
XC7354	58	38		58																							
XC7372	84			57	72	84																					
XC73108	120				72	84			120		120								120								
XC73144	156										136								156								
XC9536	34	34																									
XC9572	72				69	72																					
XC95108	108				69	81					108																
XC95144	133					81					133																
XC95180	168																168										
XC95216	168										133						168										
XC95288	192																168							192			
XC95432	240																						240				
XC95576	240																						240				
XC3020/A/L & XC3120A	64			58	64	64																					
XC3030/A/L & XC3130A	80	34	54	58	74	80																					
XC3042/A/L & XC3142A/L	96				74	82			96	96																	
XC3064/A/L & XC3164A	120				70				110	110		120															
XC3090/A/L & XC3190A/L	144				70				120		138	144	144	144			144										
XC3195A	176				70						138		144				176	176									
XC4003E	80				61	77	80																				
XC4005E	112				61	77			112	112	112	112					112										
XC4005L	112				61												112										
XC4006E	128				61				113	125	128						128										
XC4008E	144				61						129				144		144										
XC4010E	160				61						129				160	160	160		160								
XC4010L	160				61									153			160										
XC4013E	192										129						160	192	192	192	192						
XC4013L	192																160		192		192						
XC4020E	224																160	192			193						
XC4025E	256																	192			193	256	256				
XC4028EX	256																160				193	256	256	256			
XC4028XL	256																160				193	256	256	256			
XC4036EX	288																						256		288	288	
XC4036XL	288																						256		288	288	

## Number of Available I/O Pins (Continued)

	Max I/O	44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	225	228	240	299	304	352	411	432	499
XC4044EX	320																								320	320	
XC4044XL	320																								320	320	
XC4052XL	352																								352	352	
XC4062XL	384																										384
XC5202	84				65	81			84	84																	
XC5204	124				65	81			117	124	124																
XC5206	148				65	81			117		133			148	148		148										
XC5210	196				65				117		133			149			164	196	196		196						
XC5215	244										133						164		196		197	244	244	244			
XC6209	180																				180	180					
XC6216	242																				199	242					
XC6236	384																										
XC6264	512																										

## Package Options

	Surface Mount							Through-hole
	PLCC	PQFP	HQFP	TQFP	VQFP	CQFP	BGA	PGA
Standard	JEDEC	EIAJ	EIAJ	EIAJ	EIAJ	JEDEC	JEDEC	JEDEC
Lead Pitch	50 mil	0.65/0.5 mm	0.65/0.5 mm	0.5 mm	0.5 mm	25 mil	1.5 mm	100 mil
Body	Plastic	Plastic	Plastic/Metal	Plastic	Plastic	Ceramic	FR4	Ceramic/ Plastic
Temperature Options	C, I	C, I	C, I	C, I	C, I	M, B	C	C, I, M, B
Ordering Code	PC	PQ	HQ	TQ/HT	VQ	CB	BG	PG, PP
XC7236A	44							
XC7272A	68, 84							84
XC7318	44	44						
XC7336	44	44						
XC7336Q	44	44			44			
XC7354	44, 68							
XC7372	68, 84	100						
XC73108	84	100, 160					225	144
XC73144		160					225	184
XC9536	44				44			
XC9572	84	100		100				
XC95108	84	100, 160	100	100				
XC95144		100, 160						
XC95180		160	208					
XC95216		160	208					
XC95288			208, 304					
XC95432			304					
XC95576			304					
XC3020/A/L & XC3120A	68, 84	100				100		84
XC3030/A/L & XC3130A	44, 68, 84	100	100	100	64			84
XC3042/A/L & XC3142A/L	68, 84	100	100, 144	100, 144		100		84, 132
XC3064/A/L & XC3164A	84	160	144	144				132
XC3090/A/L & XC3190A/L	84	160, 208		144, 176		164		175
XC3195A	84	160, 208						175, 223
XC4003E	84	100			100			120
XC4005E	84	100, 160, 208		144		164		156
XC4005L	84	208						
XC4006E	84	160, 208		144				156
XC4008E	84	160, 208						191
XC4010E	84	160, 208				196	255	191
XC4010L	84	208		176				
XC4013E		160, 208, 240	208, 240			228	225	223
XC4013L		208, 240					225	
XC4020E			208, 240					223

## Package Options (Continued)

	Surface Mount							Through-hole
	PLCC	PQFP	HQFP	TQFP	VQFP	CQFP	BGA	PGA
Standard	JEDEC	EIAJ	EIAJ	EIAJ	EIAJ	JEDEC	JEDEC	JEDEC
Lead Pitch	50 mil	0.65/0.5 mm	0.65/0.5 mm	0.5 mm	0.5 mm	25 mil	1.5 mm	100 mil
Body	Plastic	Plastic	Plastic/Metal	Plastic	Plastic	Ceramic	FR4	Ceramic/Plastic
Temperature Options	C, I	C, I	C, I	C, I	C, I	M, B	C	C, I, M, B
Ordering Code	PC	PQ	HQ	TQ/HT	VQ	CB	BG	PG, PP
XC4025E			240, 304			228		223, 299
XC4028EX			208, 240, 304				352	299
XC4028XL			208, 240, 304				352	299
XC4036EX			304				432	411
XC4036XL			304				432	411
XC4044EX							432	411
XC4044XL							432	411
XC4052XL							432	411
XC4062XL								499
XC5202	84	100		144	100			156
XC5204	84	100, 160		144	100			156
XC5206	84	100, 160, 208		144, 176	100			191
XC5210	84	160, 208, 240		144, 176			225	223
XC5215		160	208, 240, 304				225, 352	299
XC6209	84		240					299
XC6216	84	240						299
XC6236								
XC6264								

### Inches vs. Millimeters

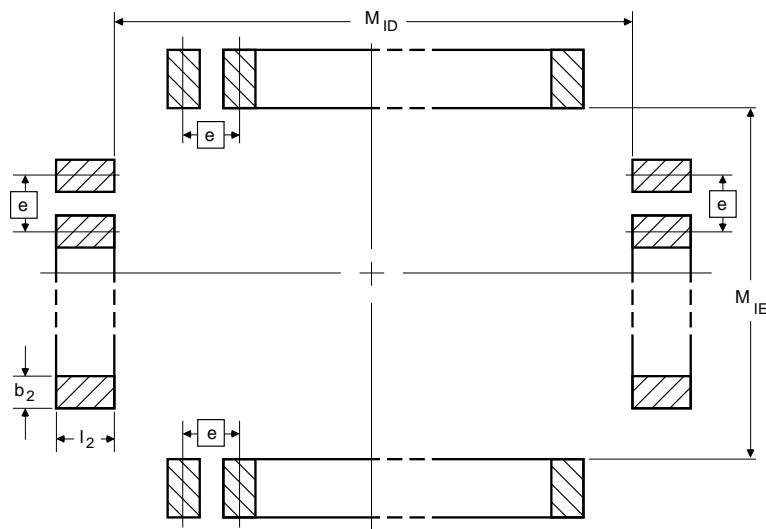
The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The EIAJ standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These

packages have a lead spacing of 0.5 mm, except for the 100- and 160-pin PQFP packages, which have a lead spacing of 0.65 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters.

## EIA Standard Board Layout of Soldered Pads for QFP Devices



**Table 1: Dimensions for Xilinx Quad Flat Packs<sup>1</sup>**

Dim.	PQ44	VQ64	PQ100	PQ160	HQ/MQ/PQ208	VQ/TQ100	TQ144	TQ176	HQ/MQ/PQ240	HQ304
$M_{ID}$	10.40	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
$M_{IE}$	10.40	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
$e$	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
$b_2$	0.4 - 0.6	0.3 - 0.4	0.3 - 0.5	0.3 - 0.5	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4
$l_2$	1.80	1.60	1.80 <sup>2</sup>	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes: 1. Dimensions in millimeters  
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

### Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled “Cavity Down”, with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

### Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100- and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

## Thermal Management

Modern high speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages are chosen to handle 'typical' designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

## Package Thermal Characterization Methods & Conditions

### Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power ( $P_d$ ) is applied. Power ( $P_d$ ) is applied to the device through diffused resistors on the same thermal die. The resulting rise

in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the set-up is within 6%.

### Definition of Terms

- $T_J$  Junction Temperature — the maximum temperature on the die, expressed in °C (degree Celsius)
- $T_A$  Ambient Temperature — expressed in °C.
- $T_C$  The temperature of the package body taken at a defined location on the body. This is taken at the primary heat flow path on the package and represents the hottest part on the package — expressed in °C.
- $T_I$  The isothermal fluid temperature when junction to case temperature is taken — expressed in °C.
- $P_d$  The total device power dissipation — expressed in watts.

### Junction-to-Reference General Setup

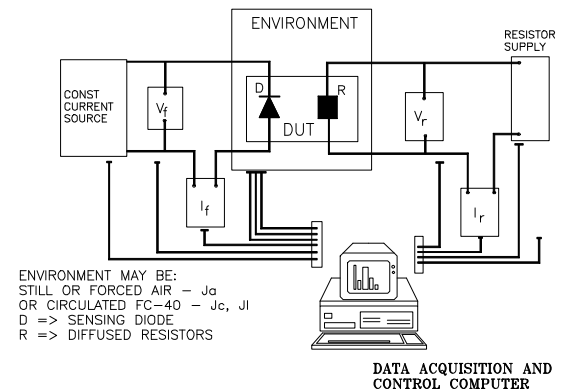


Figure 1: Thermal Measurement Set-Up (Schematic for Junction to Reference)

### Junction-to-Case Measurement — $\Theta_{JC}$

$\Theta_{JC}$  is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded.  $P_d$  is then applied. Case temperature ( $T_C$ ) is measured at the primary heat-flow path of the particular package. Junction temperature ( $T_J$ ) is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/P_d$$

The junction-to-isothermal-fluid measurement ( $\Theta_{JL}$ ) is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_I)/P_d$$

The latter data is considered as the ideal  $\Theta_{JA}$  data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heat-sinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the  $\Theta_{JA}$  data is not published. The thermal lab keeps such data for package comparisons.

## Junction-to-Ambient Measurement — $\Theta_{JA}$

$\Theta_{JA}$  is measured on FR4 based PC boards measuring 4.5" x 6.0" x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with 2 signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has 2 internal copper planes (one power, one ground) and 2 signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as  $\Theta_{JC}$  measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The

junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/P_d$$

The setup described herein lends itself to the application of various airflow velocities from 0 - 800 Linear Feet per Minute (LFM), i.e., 0 - 4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

## Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration,  $\Theta_{JA}$ ,  $\Theta_{JC}$ , fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 1 shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

**Table 2: Summary of Thermal Resistance for Packages**

PKG-CODE	$\Theta_{JA}$ at 0° (Max)	$\Theta_{JA}$ at 0° (Typ)	$\Theta_{JA}$ at 0° (Min)	$\Theta_{JA}$ at 250° (Typ)	$\Theta_{JA}$ at 500° (Typ)	$\Theta_{JA}$ at 750° (Typ)	$\Theta_{JC}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BG225	37	30	24	19	17	16	3.3	Various
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
CQ100	46	45	44	37	30	25	7.1	Socketed
DD8	114	109	97	90	73	60	8.2	Socketed
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
MQ208	18	18	17	14	13	12	1.2	2L/0P-SMT
MQ240	17	17	16	12	11	10	1.2	2L/0P-SMT
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT
PD48	43	43	43	33	29	27	11.6	Socketed
PD8	82	79	73	60	54	50	22.2	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG144	26	25	23	17	14	13	3.7	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Estimated
PG68	39	37	34	26	20	17	7.8	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PP132	35	34	33	23	18	17	6.0	Socketed
PP175	29	29	28	19	15	13	2.5	Socketed
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
PQ44	52	51	51	40	36	35	12.4	4L/2P-SMT
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT



**Table 2: Summary of Thermal Resistance for Packages (Continued)**

PKG-CODE	$\Theta_{JA}$ at 0 <sup>7</sup> (Max)	$\Theta_{JA}$ at 0 <sup>7</sup> (Typ)	$\Theta_{JA}$ at 0 <sup>7</sup> (Min)	$\Theta_{JA}$ at 250 <sup>6</sup> (Typ)	$\Theta_{JA}$ at 500 <sup>6</sup> (Typ)	$\Theta_{JA}$ at 750 <sup>6</sup> (Typ)	$\Theta_{JC}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
WB144	28	28	28	—	—	—	6.0	2L/0P-SMT
WB225	28	28	28	—	—	—	6.0	2L/0P-SMT
WC44	47	46	45	38	31	25	9.1	Socketed
WC68	46	43	40	31	26	23	7.0	Socketed
WC84	43	41	38	29	24	21	3.9	Socketed

- Notes:
1. Maximum, typical and minimum numbers are based on numbers for all the devices in the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
  2. Package configurations and drawings are in the package section of the data book.
  3. 2L/0P - SMT: the data is from a surface mount type I board -- no internal planes on the board.
  4. 4L/2P - SMT: the data is from a 4 layer SMT board incorporating 2 internal planes. Socketed data is taken in socket.
  5. Thermal data is in degree Celsius/watt.
  6. Airflow is reported in Linear Feet per minute (LFM).
  7. Columns 1, 2 and 3 are for  $\Theta_{JA}$  in still air.

## Application of Thermal Resistance Data

Thermal resistance data gauges the IC package thermal performance.  $\Theta_{JC}$  measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior.  $\Theta_{JC}$  strongly depends on the package's heat conductivity, architecture and geometrical considerations.

$\Theta_{JA}$  measures the total package thermal resistance including  $\Theta_{JC}$ .  $\Theta_{JA}$  depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a  $\Theta_{JA}$  value 20% higher than the same package mounted on a 4 layer board with power and ground planes.

By specifying a few constraints, devices are ensured to operate within the intended temperature range. This also ensures device reliability and functionality. The system ambient temperature needs to be specified. A maximum  $T_J$

also needs to be established for the system. The following inequality will hold.

$$T_J(\text{max}) > \Theta_{JA} * P_d + T_A$$

The following two examples illustrates the use of this inequality.

### Example 1:

The manufacturer's goal is  $T_J(\text{max}) < 100^\circ\text{C}$

A module is designed for a  $T_A = 45^\circ\text{C}$  max.

A XC3042 in a PLCC 84 has a  $\Theta_{JA} = 32^\circ\text{C/watt}$ .

Given a XC3042 with a logic design with a rated power  $P_d$  of 0.75watt.

With this information, the maximum die temperature can be calculated as:

$$T_J = 45 + (32 \times .75) ==> 69^\circ\text{C}.$$

The system manufacturer's goal of  $T_J < 100^\circ\text{C}$  is met.

**Example 2:**

A module has a  $T_A = 55^\circ\text{C}$  max.

The Xilinx XC4013E is in a PQ240 package (HQ240 is also considered).

A XC4013E, in an example logic design, has a rated

power of 2.50 watts. The module manufacturers goal is  $T_J(\text{max.}) < 100^\circ\text{C}$ .

**Table 3** shows the package and thermal enhancement combinations required to meet the goal of  $T_J < 100^\circ\text{C}$ .

**Table 3: Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

Dev Name	Package	$\Theta_{JA}$ still air	$\Theta_{JA}$ (250 LFM)	$\Theta_{JA}$ (500 LFM)	$\Theta_{JA}$ (750 LFM)	$\Theta_{JC}$	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4 Layer Board data

Possible Solutions to meet the module requirements of  $100^\circ\text{C}$ :

1a. Using the standard PQ240;

1b. Using standard PQ240 with 250LFM forced air

2a. Using standard HQ240

2b. Using HQ240 with 250 LFM forced air

$$T_J = 55 + (23.7 \times 2.50) \Rightarrow 114.25^\circ\text{C}.$$

$$T_J = 55 + (17.5 \times 2.50) \Rightarrow 98.75^\circ\text{C}$$

$$T_J = 55 + (12.5 \times 2.50) \Rightarrow 86.25^\circ\text{C}$$

$$T_J = 55 + (8.6 \times 2.50) \Rightarrow 76.5^\circ\text{C}$$

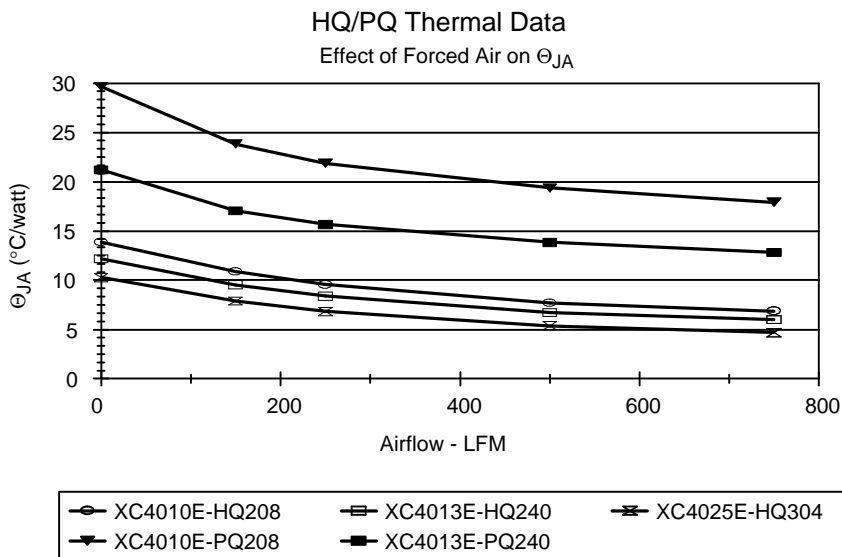
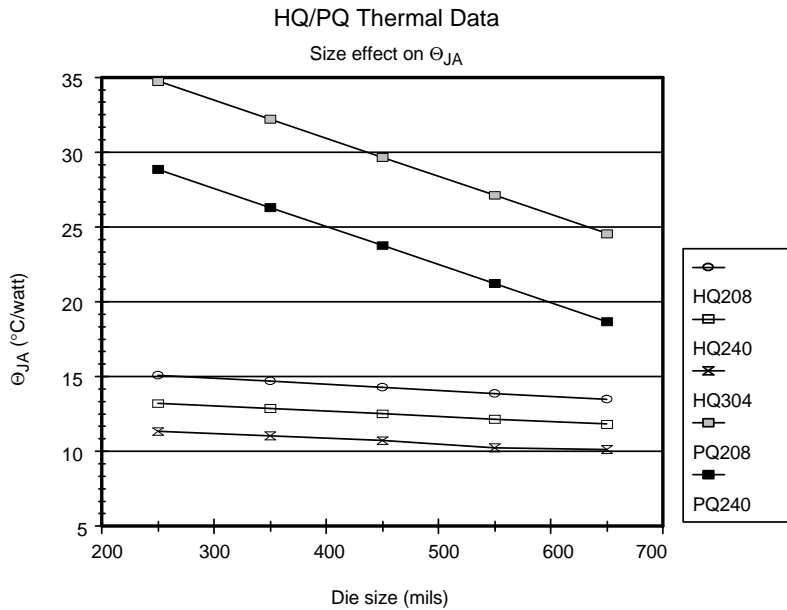
For all solutions, the junction temperature is calculated as:

$$T_J = \text{Power} \times \Theta_{JA} + T_A$$

All solutions meet the module requirement of less than  $100^\circ\text{C}$ , with the exception of the PQ240 package in still air.

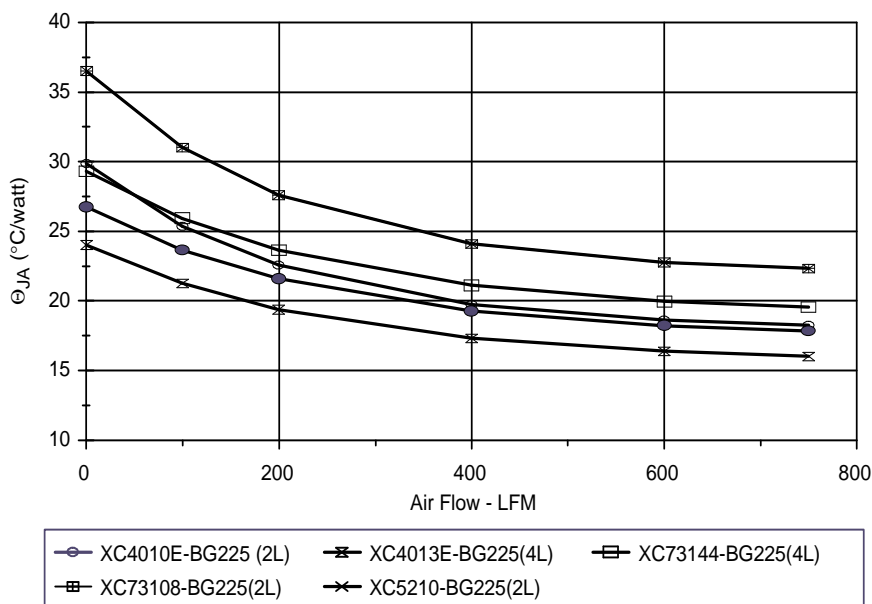
In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements -- such as forced air cooling, heat sinking, etc. may be necessary to meet the  $T_J(\text{max})$  conditions set.

## PQ/HQ Thermal Data Comparison



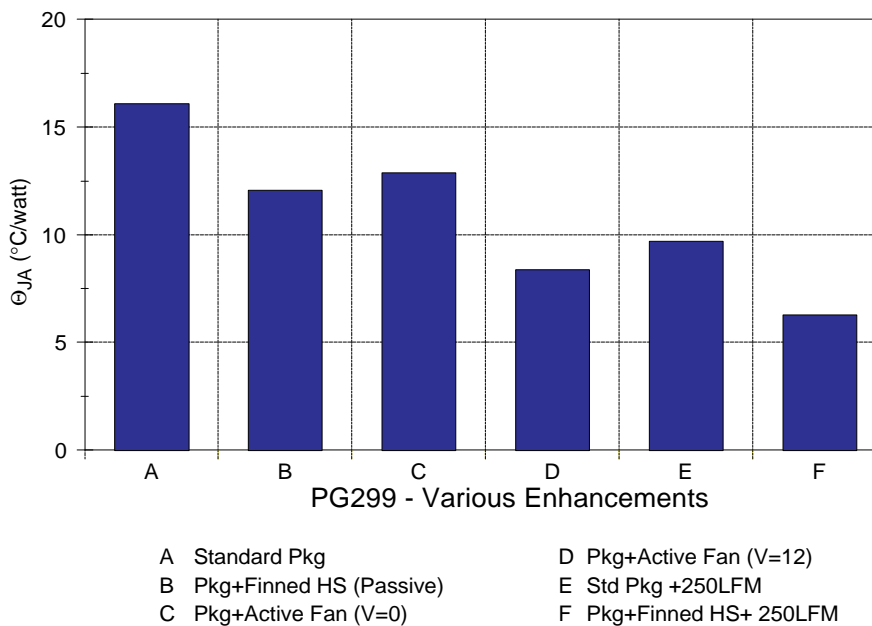
## BGA Thermal Resistance

Effect of Air Flow on  $\Theta_{JA}$



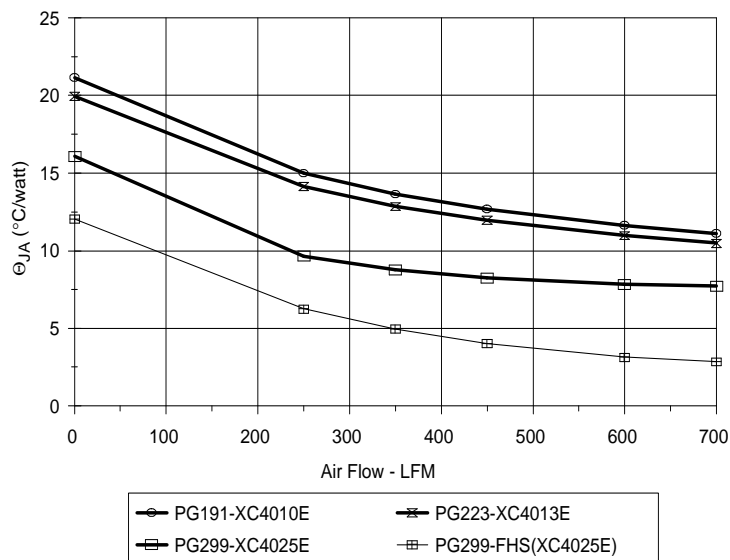
## PG299 Thermal Resistance

Effects of Active & Passive Heat sinks



# PGA 299 Thermal Resistance

Effect of Air Flow on  $\Theta_{JA}$



## Some Power Management Options

FPGA devices are usually not the dominating power consumers in a system, and do not have a big impact on power supply designs. There are obvious exceptions. When the actual or estimated power dissipation appears to be more than the specification of the chosen package, some options can be considered. Details on the engineering designs and analysis of some of these suggested considerations may be obtained from the references listed at the end of the section. The options include:

- A Xilinx low power (L) version of the circuit in the same package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated. For more information, contact the Xilinx Hotline group.
- Explore thermally enhanced package options available for the same device. As illustrated above, the HQ240 package has a thermal impedance of about 50% of the equivalent PQ240. Besides, the 240 lead, the 208 lead and the 304 lead Quad packages have equivalent heatsink enhanced versions. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink enhanced packages. Most of the high gate count devices above the XC4013 level come either exclusively in heat enhanced packages or have these packages as options. If the use of a standard PQ appears to be a handicap in this respect, a move to the equivalent HQ package if available may resolve the issue. The heat enhanced packages are pin to pin compatible and they use the same board layout.
- The use of forced air is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200 -- 300 LFM) can reduce junction to ambient thermal resistance by 30%.
- If space will allow, the use of finned external heatsinks can be effective. If implemented with forced air as well, the benefit can be a 40% to 50% reduction. The HQ304, all cavity down PGAs, and the BG352 with exposed heatsink lend themselves to the application of external heatsinks for further heat removal efficiency.
- Outside the package itself, the board on which the package sits can have a significant impact. Board designs may be implemented to take advantage of this.

Heat flows to the outside of a board mounted package and is sunk into the board to radiate. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package. Some of the heatsink packages with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal.

## References

### Forced Air Cooling Application Engineering

COMAIR ROTRON  
2675 Custom House Court  
San Ysidro, CA 92173  
1-619-661-6688

### Heatsink Application Engineering

The following facilities provide heatsink solutions for industry standard packages.

#### AAVID Thermal Technologies

1 Kool Path  
Box 400  
Laconia, NH 03247-0400  
1-603-528-3400

#### Thermalloy, Inc.

2021 W. Valley View Lane  
Box 810839  
Dallas, TX 75381-0839  
1-214-243-4321

#### Wakefield Engineering, Inc.

60 Audubon Road  
Wakefield MA 01880-1255  
1-617-245-5900

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

## Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BG225	MOLDED BGA 27mm- ANAM	MO-151-CAL	OBG0001	2.2
BG352	SUPERBGA - 35X35MM AMKOR	MO-151-BAR	OBG0008	7.1
BG432	SUPERBGA - 40X40MM AMKOR	MO-151-BAU	OBG0009	9.1
CB100	NCTB TOP BRAZE 3K VER	MO-113	OCQ0008	10.8
CB100	NCTB TOP BRAZE 4K VER	MO-113	OCQ0006	10.8
CB164	NCTB TOP BRAZE 3K VER	MO-113-AA	OCQ0003	11.5
CB164	NCTB TOP BRAZE 4K VER	MO-113-AA	OCQ0007	11.5
CB196	NCTB TOP BRAZE 4K VER	MO-113-AB	OCQ0005	15.3
CB228	NCTB TOP BRAZE 4K VER	MO-113	OCQ0012	17.6
CC20	CERAMIC LEADED CHIP CARRIER	N/A	OCQ0011	8.4
DD8	.300 Cerdip PACKAGE	MO-036-AA	OPD0005	1.1
HQ208	METRIC 28 X 28 - H/S DIE UP	MO-143-FA1	OPQ0020	10.8
HQ240	METRIC QFP 32 32 - H/S DIE UP	MO-143-GA	OPQ0019	15.0
HQ304	METRIC QFP 40 40-H/S DIE DOWN	MO-143-JA	OPQ0014	26.2
MQ208	METAL QUAD EIAJ	N/A	OPQ0006	6.1
MQ240	METAL QUAD	N/A	OPQ0011	8.0
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC28	PLCC JEDEC MO-047	MO-047-AB	OPC0001	1.1
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD48	DIP .600	N/A	OPD0001	7.9
PD8	DIP .300 STANDARD	MO-001-AA	OPD0002	0.5
PG120	CERAMIC PGA 13 X 13 MATRIX	MO-067-AE	OPG0012	11.5
PG132	CERAMIC PGA 14 X 14 MATRIX	MO-067-AF	OPG0004	11.8
PG144	CERAMIC PGA 15 X15 CAVITY UP	MO-067-AG	OPG0017	16.9
PG156	CERAMIC PGA 16 X 16 MATRIX	MO-067-AH	OPG0007	17.1
PG175	CERAMIC PGA 16X16 STD VER.	MO-067-AH	OPG0009	17.7
PG184	CERAMIC PGA 15 X15 CAVITY UP	MO-067-AG	OPG0019	17.5
PG191	CERAMIC PGA 18 X 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	CERAMIC PGA 18 X 18 TYPE	MO-067-AK	OPG0016	26.0
PG299	CERAMIC PGA 20 X 20 HEATSINK	MO-067-AK	OPG0022	37.5
PG299	CERAMIC PGA 20 X 20 TYPE	MO-067-AM	OPG0015	29.8
PG411	CERAMIC PGA 39 X 39 STAGGER	MO-128-AM	OPG0019	36.7
PG68	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0002	7.0
PG84	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0003	7.2
PP132	PLASTIC PGA 14 X 14 MATRIX	MO-83-AF	OPG0001	8.1
PP175	PLASTIC PGA 16X16 BURRIED	MO-83-AH	OPG0006	11.1
PQ100	EIAJ 14X20 QFP - 1.60	MO-108-CC1	OPQ0013	1.6
PQ160	EIAJ 28X28 .65MM 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28X28 .5MM 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 X 32 .5MM	MO-143-GA	OPQ0010	7.1
PQ44	EIAJ 10 X 10 X 2.0	MO-108-AA2	OPQ0015	0.5
SO8	VERSION 1 - .150/55MIL	MO-150	OPD0006	0.1
TQ100	THIN QFP 1.4mm thick	MS-026-BDE	OPQ0004	0.7

## Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
TQ144	THIN QFP 1.4mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	THIN QFP 1.4mm thick	MS-026-BGA	OPQ0008	0.9
VO8	THIN SOIC-II	N/A	OPD0007	0.1
VQ100	THIN QFP 1.0 thick	MS-026-AED	OPQ0012	0.6
VQ44	EIAJ 10 X 10 X 1.0	MS-026-ACB	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
WC44	JEDEC WINDOWED CQUAD	MO-087	OCQ0004	2.9
WC68	WINDOWED CERQUAD	MO-087	OCQ0009	7.3
WC84	WINDOWED CERQUAD	MO-087	OCQ0010	11.0

Notes: 1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.  
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.



# Xilinx Thermally Enhanced Packaging

## The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ208	28x28	3.37	10.0	DOWN	MO-143-FA	OPQ0020

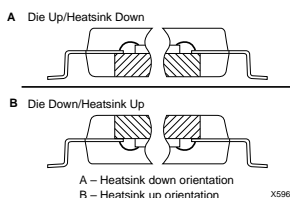
## Overview

Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

## Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240 pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.
- At the 304 pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.



## Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

	PQ (gm)	MQ (gm)	HQ (gm)
208 Pin	5.3	6.1	10.0
240 Pin	7.1	8.0	15.0
304 Pin	N/A	N/A	26.2

## Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Still Air Data Comparison			
	HQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )	MQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )	PQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )
208 Pin	10-14	17-19	25-32
240 Pin	11-14	15-17	18-28
304 Pin	10-12	N/A	N/A

Note:  $\Theta_{JC}$  is typically between 1 and 2  $^{\circ}\text{C}/\text{Watt}$  for HQ and MQ Packages. For PQ's, it is between 2 and 7  $^{\circ}\text{C}/\text{Watt}$ .

Data Comparison at Airflow - 250 LFM			
	HQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )	MQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )	PQ $\Theta_{JA}$ ( $^{\circ}\text{C}/\text{Watt}$ )
208 Pin	9-10	14-15	19-25
240 Pin	8-9	11-13	14-20
304 Pin	6.5-8	N/A	N/A

## Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated  $\rightarrow$  Heatsink metal is Grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material - Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd. Same as PQ - EME7304LC
- Packed in the same JEDEC trays

## Moisture Sensitivity of PSMCs

### Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details -- materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures

have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112. Test Method A112 "Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices".

Available through Global Engineering Documents  
Phone: USA and Canada 800-854-7179, International 1-303-792-2181

- IPC Standard IPC-SM-786A "Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs".

Available through IPC  
Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established 6 levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in [Table 4](#). Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In [Table 4](#), the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

**Table 4: Package Moisture Sensitivity Levels per JEDEC A112**

Level	Factory Floor Life		Soak Requirements (Preconditioning)			
	Conditions	Time	Time			Conditions
1	≤30°C / 90% RH	Unlimited	168 hours			85°C / 85% RH
2	≤30°C / 60% RH	1 year	168 hours			85°C / 60% RH
			Time (hours)			
			X +	Y =	Z	
3	≤30°C / 60% RH	168 hours	24	168	192	≤30°C / 60% RH
4	≤30°C / 60% RH	72 hours	12	72	84	≤30°C / 60% RH
5	≤30°C / 60% RH	24 hours	6	24	30	≤30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	≤30°C / 60% RH

Notes: X = Default value of semiconductor manufacturer's time between bake and bag. If the semiconductor manufacturer's actual time between bake and bag is different from the default value, use the actual time.  
Y = Floor life of package after it is removed from dry pack bag.  
Z = Total soak time for evaluation.

## Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in [Table 4](#). If factory floor conditions are outside the stated environmental conditions (85°C/85% RH for level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

## Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C., in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches

are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

## Handling Parts in Sealed Bags

### Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

### Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in part appearance can verify moisture levels.

### **Expiration Date**

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

### **Other Conditions**

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, **if the factory floor life has not been exceeded**. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

## Tape and Reel

Xilinx offers a tape & reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive Polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape & reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

### Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape & reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Anti-static reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape & reel shipments include desiccant pouches and humidity indicators to insure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481.

## Material and Construction

### Carrier Tape

- The pocketed carrier Tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded 'live bug' or leads down, into a device pocket.

- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into an automated board assembly equipment.

### Cover Tape

- An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.
- Surface resistivity on both sides is less than 1011 ohms per square inch.

### Reel

- The reel is made of anti-static Polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.
- A protective strip made of conductive Polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.
- Surface resistivity is less than 1011 ohms per square inch.
- Device loading orientation is in compliance with EIA Standard 481.

### Bar Code Label

- The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.
- Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.
- The label is an alphanumeric, medium density Code 39 labels.
- This machine-readable label enhances inventory management and data input accuracy.

### Shipping Box

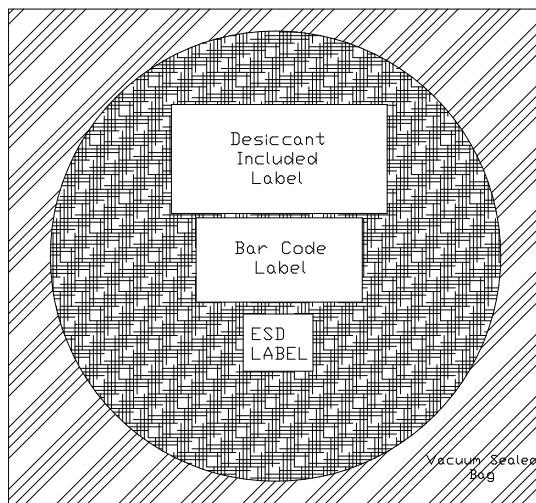
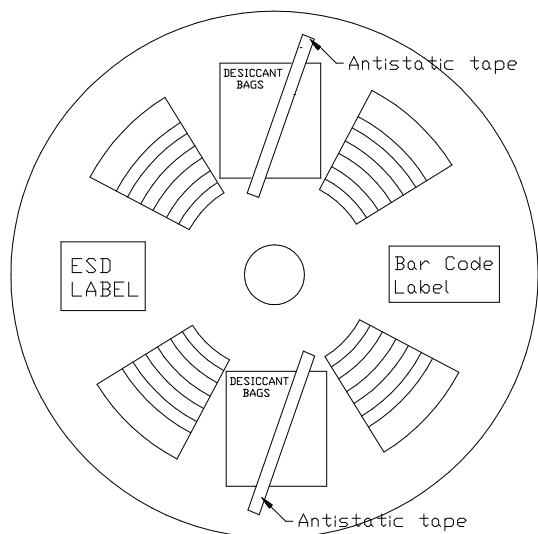
- The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, # 3 white 'pizza' box, rated to 200 lb test.

**Table 5: Tape & Reel Packaging**

Package Type	Pin Count	Carrier Width	Cover Width	Pitch	Reel Size	Qty per Reel
PLCC (Plastic Leaded Chip Carrier)	20	16 mm	13.3 mm	12 mm	7 inch	250
	20	16 mm	13.3 mm	12 mm	13 inch	750
	44	32 mm	25.5 mm	24 mm	13 inch	500
	68	44 mm	37.5 mm	32 mm	13 inch	250
	84	44 mm	37.5 mm	36 mm	13 inch	250
SO (Plastic Small Outline)	8	12 mm	9.2 mm	8 mm	7 inch	750
QFP (Plastic Quad Flat Pack)	100	44 mm	37.5 mm	32 mm	13 inch	250
	160	44 mm	37.5 mm	40 mm	13 inch	200
BGA (Plastic Ball Grid Array)	225	44 mm	37.5 mm	32 mm	13 inch	500

- Notes:
- 1.A minimum of 230mm of empty pockets are provided at the beginning (leader) of each reel.
  - 2.A minimum of 160mm of empty pockets are provided at the end (trailer) of each reel.
  - 3.Tape Leader/Trailer requirements are in compliance to EIA Standards 481.
  - 4.Peel Strength between 20 and 120 grams ensures consistency during de-reeling operations and is compliant to EIA Standard 481.
  - 5.Each reel is subject to peel back strength tests.
  - 6.For packages not listed above, please contact your Xilinx sales representative for updated information.

## Standard Bar Code Label Locations



## Reflow Soldering Process Guidelines

In order to implement and control the production of surface mount assemblies, the dynamics of the solder reflow process, and how each element of the process is related to the end result, must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in [Figure 2](#).

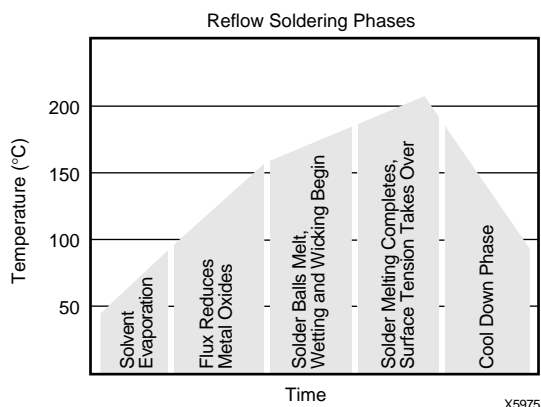


Figure 2:

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in [Figure 3](#).

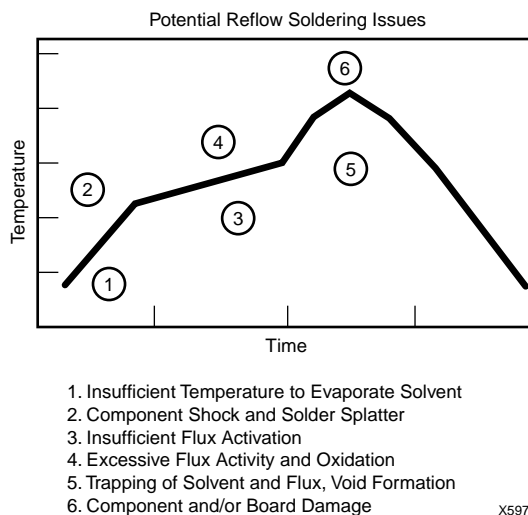
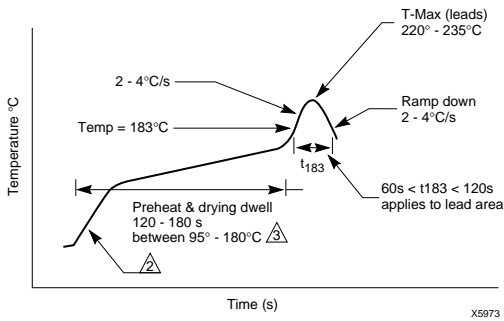


Figure 3:

Figure 4 and Figure 5 show typical conditions for solder reflow processing using Vapor Phase or IR Reflow. The moisture sensitivity of Plastic Surface Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

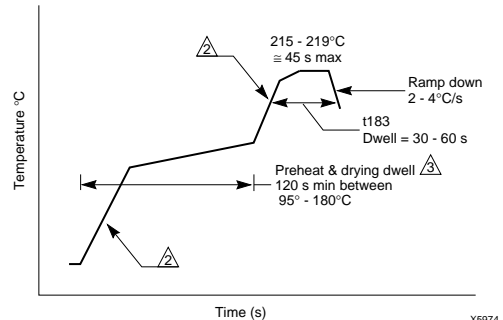


**Figure 4:** Typical conditions for IR reflow soldering

Notes:

1. Max temperature range = 220°C-235°C (leads)  
Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.



**Figure 5:** Typical conditions for vapor phase reflow soldering

Notes:

1. Solvent - FC5312 or equivalent - ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.



## Sockets

**Table 6** lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorse-

ment by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

**Table 6: Socket Manufacturers**

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	