

Summary

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application.

Xilinx Families

XC2000, XC3000, XC4000, XC5000, XC6000, XC7000, XC9000

Demonstrates

Choosing an appropriate Xilinx family based on the intended application

Table of Contents

SRAM-Based FPGAs

Antifuse-Based FPGAs

EPROM and FLASH-Based CPLDs

Selecting the Appropriate Xilinx Family

Introduction

Xilinx offers Field-Programmable Logic circuits, mass-produced standard integrated circuits that the user can customize for the specific application.

Xilinx products offer the following advantages:

- High integration (less space, lower power, higher reliability, lower cost) than solutions based on existing standard devices like MSI and PALs.
- No non-recurring engineering charges and associated risk, typically required for mask-programmed gate array solutions.
- Fast design time and easy design modification, important for early time-to-market.
- Designs can be upgraded in the field for added functionality.

Some potential users might be confused by the wide diversity of Xilinx product offerings. This application note provides a broad overview from the user's perspective.

Xilinx offers programmable logic circuits in two distinctly different technologies.

- SRAM-based FPGAs, the original Xilinx offering, now encompassing the XC2000, XC3000, XC4000, XC5200, and XC6200 series and their sub-families, like the XC3000A, XC3000L, XC3100, XC3100A, XC4000A, XC4000H, XC4000E, XC4000L, XC4000EX, and XC4000XL.
- Complex PLDs or EPLDs, XC7300, and XC9500 families.

SRAM-Based FPGAs

Xilinx SRAM-based FPGAs fall into two distinct categories. All are reconfigurable and can be programmed in-system; only the XC6200 family can be partially reconfigured and offers a built-in microprocessor interface. The two categories of devices are separately described below.

SRAM-Based FPGAs (XC2000, XC3000, XC3100, XC4000, XC5200)

These families represent an ongoing evolution of the original Xilinx FPGA architecture, characterized by structural flexibility and an abundance of flip-flops. Logic is implemented in look-up tables, and is interconnected by a hierarchy of metal lines controlled by pass transistors.

Attractive systems features include on-chip bidirectional busses and individual output 3-state and slew-rate control, common reset for all flip-flops, and multiple global low-skew clock networks.

The configuration can be loaded while the devices are connected into a system, and can be changed an unlimited number of times by reloading the "bitstream," the series of bits used to program the device. Configuration must be reloaded whenever Vcc is re-applied. Reconfiguration takes 20 to 200 ms, during which time all outputs are inactive.

Static power consumption is very low, down to microwatts for some of the families. Dynamic power consumption is proportional to the clock frequency, and depends on the logic activity inside the device and on the outputs.

The description "SRAM-based" refers primarily to the standard high-volume manufacturing process, and secondarily to the fact that configuration data is stored in latches. Different from typical SRAMs, these latches use low-impedance active pull-up and pull-down transistors. An on-chip voltage monitor 3-states the outputs and initiates reconfiguration when Vcc drops significantly (to 3.2 V in a 5-V system).

These FPGAs are available in different sizes and many different packages. Usually each device type is available in many package types. Any package can accommodate different sized devices with compatible pinouts, so the user can migrate to a larger or smaller device without changing the PC-board layout.

Overview of SRAM-Based FPGA Families

XC2000: Oldest, simplest, smallest, and lowest-cost FPGA family; not recommended for new designs

- Used for simple, very cost-sensitive applications.
- Accept limited logic flexibility, 3-input look-up tables, no clock enables, no output slew-rate control, only two device types covering the narrow complexity range of 600 to 1500 gates.

The XC5200 FPGA family or the XC7300 and XC9500 EPLD families, may often be a better alternative.

XC2000L: 3.3-V version of XC2000; not recommended for new designs

- Used for simple, battery-operated applications.
- Accept significantly slower speed at 3.3 V, compared to XC2000 at 5 V.

XC3000: Superseded

Don't use this venerable family for new designs, since it has been superseded by the improved, but fully backwards compatible, XC3000A family.

XC3000A: Newest version of the popular XC3000 family

Five device types cover a complexity range from 1,300 to 7,500 gates, with 256 to 928 flip-flops. Logic is implemented in 4-input look-up tables; two tables can be combined to implement any logic function of five variables with only one combinatorial delay of 4 or 5 ns. Flip-flop toggle rate is over 110 MHz.

Global choice of input thresholds (1.2 V or 2.5 V), output slew-rate control, and an on-chip crystal oscillator circuit are attractive system features.

- Use for medium-speed, medium-complexity applications.
- Accept lack of dedicated carry circuits, resulting in less efficient and slower arithmetic and counters than in XC4000E families. No on-chip RAM; data storage is thus limited to the available 256 to 928 flip flops.

XC3000L: 3.3-V version of XC3000A

- Use for battery-operated applications.
- Accept significantly slower speed at 3.3 V, compared to XC3000A at 5 V.

XC3100: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC3100A family.

XC3100A: Newest version of the popular high-speed XC3100 family

XC3100A devices are functionally and bitstream identical with the XC3000A, and are available in the same packages with the same pinouts. The only difference is the higher speed of the XC3100A, with a look-up table delay of 1.5 to 4 ns, and the slightly higher standby current of 8 to 14 mA. One additional high-end family member, the XC3195A, can implement up to 9,000 gates and 1,320 flip-flops.

- Use for high performance design with system clock rates up to 100 MHz.
- Accept lack of dedicated carry circuits, resulting in less efficient and possibly slower arithmetic and counters than in XC4000E. No on-chip RAM; data storage is thus limited to the available 256 to 1,320 flip-flops.

XC3100L: 3.3-V version of XC3100A

- Use for 3.3-V applications.
- Accept significantly slower speed at 3.3 V, compared to XC3100A at 5 V, as well as higher quiescent power and much higher powerdown current than XC3000L at 3.3 V.

XC4000: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC4000E family.

XC4000A: Superseded

Don't use this family for new designs, since it has been superseded by the improved, faster, less expensive, and pinout-compatible – but not bitstream-compatible – XC4000E family.

XC4000E: Enhanced superset of the XC4000 family

The XC4000E family is recommended for new designs.

The ten devices in this family stretch from 2,000 to 25,000 gate complexity. The emphasis is on systems features and speed. The function generators are more versatile than in the XC3000-Series parts, and there is a dedicated carry network to speed up arithmetic and counters and make them more efficient. Most importantly, the function generators can be used as user RAM with asynchronous or synchronous write addressing, even as dual-port RAMs. This capability makes register files, shift registers and especially FIFOs faster and much more efficient than in any other FPGA.

Logic speed is not as fast as XC3100, but dedicated carry logic can speed up wide arithmetic and long counters even above XC3100 speed.

- Use for general-purpose logic and data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Use for on-chip distributed RAMs, e.g. 50-MHz FIFOs up to 64 deep, 32 bits wide.
- Accept lack of crystal oscillator circuitry and lack of Powerdown feature.

XC4000EX: Larger version of the XC4000E family, largest devices made by Xilinx

Extension of the XC4000E family from 28k to 125k gates, with greatly increased routing resources, faster clocking options and more versatile output logic.

- Use for designs beyond 20,000 gate complexity.

XC4000H: High I/O version of XC4000, not recommended for new designs

Variations of XC4003 and XC4005, with significantly increased number of I/Os. Internal functionality identical to XC4003 and XC4005, but number of I/Os increased from 80 to 160 for XC4003H, from 112 to 192 for XC4005H. No input or output flip-flops in the IOBs, but 24 mA sink current and sophisticated slew-rate control that can minimize ground bounce.

- Used for I/O-intensive applications, but also consider XC5200 as a lower-cost alternative when internal RAM is not required.
- Accept lack of I/O flip-flops, thus larger output delay, larger uncertainty in input set-up time.

XC5200: Low-cost FPGA

New architecture optimized for low cost, good routability, and the ability to lock pinout while internal logic is being modified. Dedicated carry structure similar to XC4000, but no RAM. Four-input function generators avoid the XC3000 input constraints. IOBs are less rigidly coupled to the internal matrix of CLBs and interconnects, which greatly improves the flexibility of pin-locked designs. IOBs have no flip-flops.

The XC5200 family offers the lowest cost per gate of all Xilinx FPGAs, whenever RAM is not required.

Performance is similar to XC3000A, but dedicated carry logic can speed up wide arithmetic and long counters.

- Use for medium-speed general-purpose logic, and for data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Alternative to XC3000A at lower cost, and with additional benefits, such as dedicated carry for arithmetic and counters, improved routing, and ability to cope with locked pinout. High I/O count. Package pinout compatible with XC4000.
- Accept lack of internal RAM and lack of crystal oscillator circuitry.

Partially-Reconfigurable SRAM-Based FPGA with Bus Interface (XC6200)

This new fine-grained architecture is very different from the other Xilinx families. It offers partial and very fast reconfigurability, supported by an 8/16/32 bit wide microprocessor bus interface. This interface can directly write to and read from any internal cell, and can even treat part of the internal configuration as user RAM.

- Use for innovative reconfigurable-processor solutions, and for general purpose solutions where fast (re)configuration is an advantage, or for register-intensive, datapath-oriented, highly structured designs.
- Accept product availability starting later in 1996.

EPROM- and FLASH-Based CPLDs (XC7300, XC9500)

These device families are extensions of the popular PAL architecture, implementing logic as wide AND gates, ORed together, driving either a flip-flop or an output directly. The simple logic structure makes these devices easy to understand, and results in both fast design compilation and short pin-to-pin delays. Wide input gating and fast system clock rates up to 150 MHz are attractive features for state machines and complex synchronous counters.

The XC7300 CPLDs use EPROM technology.

The new XC9500 in-system programmable family, based on FLASH technology, eliminates the need for a separate programmer. These new devices also offer boundary scan (JTAG) to simplify board testing.

Overview of CPLD Families

XC7200A: Superseded

Not recommended for new designs. Use XC7300 instead.

XC7300: EPROM-Based CPLD

Six devices cover the range from 18 to 144 macrocells in 44- to 225-pin packages.

- Use for high-speed logic, short pin-to-pin delays, for state machines and flexible address decoding, and as PAL replacement. Dedicated carry logic offers fast and efficient adders, subtractors, comparators, and counters.
- Accept higher power consumption and fewer available flip-flops compared to SRAM-based or antifuse-based FPGAs.
- The XC7318, XC7336/Q, and XC7354 are very effective as PAL replacements. The XC7336Q boasts significantly reduced power consumption.

Delays are deterministic, and compile times are very short.

XC9500: FLASH-Based CPLD

Nine devices cover the range from 36 to 576 macrocells.

The new XC9500 family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration.

- Use XC9500 for CPLD applications requiring fast pin-to-pin speeds.
- Accept higher power consumption and fewer available flip-flops compared to SRAM- or antifuse-based FPGA.

Selecting the Appropriate Xilinx Family

It is not always obvious which Xilinx family is the “right” choice for a particular application. To make a decision, start with the known data, the target application. Then address the following questions:

- What type of logic is used in the application?
- What special features are required?

Type of Logic

All Xilinx devices are general-purpose. Any family can implement any type of logic. There are, however, some features that make certain families more appropriate than others. The following items should be interpreted as “soft” suggestions, not as absolute, unequivocal choices.

1. For shortest pin-to-pin delays and fastest flip-flops:

Use XC9500, XC7300, or, if fan-in is sufficient, XC3100A, XC4000E/EX.

XC9500 and XC7300 CPLDs have a PAL-like AND/OR structure that is inherently very fast. XC3100 has extremely fast logic blocks, but the single-level fan-in is limited to five.

XC4000E/EX have slower logic blocks, but a wider fan-in of nine. XC4000EX FPGAs offer a very fast pin-to-pin path using a FastClk buffer and a 2-input function generator in the IOB.

2. For fastest state machines:

For encoded state machines, use XC9500, XC7300.

For “one-hot” state machines, use XC3100, XC4000E/EX, XC5200.

3. For fast counters/adders/subtractors/accumulators/comparators:

Use XC4000E/EX, XC5200 or XC7300 for wide functions.

Use XC3100A for very fast, but short or simple counters.

XC4000E/EX and XC5200 have dedicated carry-logic that is most effective over the range of 8 to 32 bits.

XC7300 has dedicated carry within a function block, and can implement unlimited carry look-ahead in the Universal Interconnect Matrix.

XC3100A achieves high speed for short word-length and simple operations (such as non-loadable counters) through its extremely fast logic blocks.

4. For I/O-intensive applications with a high ratio of I/O to gates:

Use XC5200.

5. For shortest design compilation time:

Use XC9500, or XC6200.

XC9500 achieves fast compilation through the simplicity of its PAL-like architecture.

XC6200 achieves fast compilation through its ASIC-like small granularity, which requires no logic partitioning effort.

6. For lowest cost per gate, when on-chip RAM is not required:

Use XC5200, XC3000A (XC2000 for small devices in high volume).

7. For pinout compatibility within and between families:

Use XC4000E/EX, XC5200.

These three families are carefully designed to fit the same pinout in any given available package. This allows easy migration to different device sizes or families in the same package. The user can add logic or streamline the design or even use a less costly or faster family without any need to change the existing PC-board layout.

8. For Digital Signal Processing (multiply-accumulate) applications:

Use XC4000E/EX.

The look-up-table architecture and the dedicated carry structure are very efficient for distributed arithmetic, a fast and effective way to implement fixed-point multiplication in digital filters.

Special Features Required

The sixteen items below describe specific features and characteristics available only in the listed families. These are, therefore, “hard” selection criteria.

9. For on-chip RAM:

Use XC4000E, XC4000EX, or XC6200.

XC4000E/EX has many 16x1 or 32x1 RAMs with synchronous or asynchronous write and dual-port capability.

XC6200 can implement an arbitrary portion of the configuration-memory space as user RAM.

10. For on-chip (bidirectional) bussing:

Use XC3000A, XC3100A, XC4000E, XC4000EX, XC5200, XC7300, XC9500 (i.e., use any Xilinx family except XC2000).

XC3000A, XC3100A, XC4000, and XC5200 families have horizontal Longlines that can be driven by internal 3-state drivers.

XC9500 and XC7300 devices implement busses indirectly using the wired-AND capability in the switch matrix.

11. For on-chip crystal oscillator circuitry:

Use XC2000/L, XC3000A/L, XC3100A/L.

The on-chip circuit is just a dedicated single-stage inverting amplifier that can be configured between two dedicated pins. It is not recommended for designs requiring very low power consumption or crystal frequencies below 1 MHz.

12. For very fast or partial reconfiguration, and for a dedicated microprocessor interface:

Use XC6200.

All other SRAM-based families must be completely reconfigured.

13. For non-volatile single-chip solutions:

Use XC9500, XC7300, or any HardWire device.

The SRAM-based devices require an external configuration source, which may be contained in the microprocessor's memory. XC3000A and XC3000L devices can be used with a battery-backed-up supply, thus eliminating the need for external configuration storage.

14. For lowest possible static power consumption at 5V:

Use XC2000, XC3000A and, to a lesser extent, XC5200, XC4000E, XC4000EX.

For I_{cc} down to a few microamps, use XC2000/L or XC3000A/L in powerdown. The other families consume a few milliamps.

Configurations for CMOS input thresholds on all inputs reduce supply current significantly.

15. For avoiding pin-locking problems with routing-intensive designs:

Use XC9500, XC7300, XC4000EX, XC5200.

XC9500 and XC7300 have special architectural features to enable pin locking.

XC4000EX and XC5200 provide additional routing channels, called VersaRing, between the core logic and the I/O.

16. For Boundary-Scan support:

Use XC4000E, XC4000EX, XC5200, XC9500.

17. For rail-to-rail output voltage swing at 5 V V_{cc} :

Use XC2000, XC3000A, XC3100A, XC4000H, XC4000E, XC4000EX, XC5200, XC6200.

(In XC4000H/E/EX, rail-to-rail is a user-option.)

XC4000, XC7300, and XC9500 have a "totem-pole" output structure with lower V_{oh} .

XC4000E/EX can be configured with a global choice of either totem-pole or rail-to-rail outputs.

XC4000H has this option per individual pin.

18. For 3.3-V operation:

Use XC2000L, XC3000L, XC4000L, XC4000XL.

19. For 5-V operation Interfacing with 3.3-V devices:

Use XC9500, XC7300 or XC4000E/EX.

Any XC4000E/EX "totem-pole" output drives 3.3-V inputs safely, and the TTL-like input threshold can be driven from 3.3-V logic.

20. For In-system programmability:

Use all Xilinx families except XC7300.

21. For PCI compatibility:

Use XC4000E/EX and XC9500.

Target and Initiator designs are available for the XC4000E.

XC3100 and XC7300 can implement target-only interfaces.

22. For Hi-Rel, military, or mil temperature-range applications:

Use XC2018, XC3000, XC3100A, XC4003A, XC4005, XC4010, XC4013.

23. For battery-operated applications requiring low stand-by current:

Use XC2000/L, XC3000A/L, XC4000E/EX, XC5200, XC6200.

XC2000L and XC3000L have inherently very low static power consumption.

XC2000 and XC3000A can use powerdown to ignore all input activity and tolerate V_{cc} down to 2.3 V, while maintaining configuration.

XC4000E/EX must be configured for CMOS input thresholds, and must shut down clock and logic activities externally.

24. For best protection against illegal copying of a design (design security):

Use XC7300, XC9500 with security bit activated.

Use XC2000, XC2000L, XC3000A, XC3000L with powerdown battery-backed-up configuration.

Further Information

For further information on any of the Xilinx products discussed in this application note, see the Xilinx WEBLINX at <http://www.xilinx.com>, or call your local sales office.

Table 1: Selecting a Xilinx Family

Feature	XC3000A	XC3000L	XC3100A	XC3100L	XC4000E	XC4000L	XC4000EX	XC4000XL	XC5200	XC6200	XC7300	XC9500
1. Shortest pin-to-pin			X		X		X				X	X
2. Fastest state machines			X		X		X		X		X	X
3. Fastest arithmetic counters			X		X				X		X	
4. High I/O to gate ratio									X			
5. Fastest compilation										X	X	X
6. Lowest cost, no RAM	X								X			
7. Footprint compatible families					X	X	X	X	X			
8. DSP (multiply/accumulate)					X	X	X	X				
9. RAM					X	X	X	X		X		
10. Bidirectional busses	X	X	X	X	X	X	X	X	X		X	X
11. Crystal oscillator	X	X	X	X								
12. Fast/partial configuration										X		
13. Non-volatile/single chip											X	X
14. Low power @ 5 V	X				X		X		X			
15. Tolerates pin-locking							X	X	X		X	X
16. Boundary scan					X	X	X	X	X			X
17. Full-swing 5 V output	X		X		option		option		X	X		
18. 3.3 V operation		X		X		X		X				
19. 5 V out drives 3.3 V					option		option				X	X
20. In-system programmable	X	X	X	X	X	X	X	X	X	X		X
21. PCI-compatible			X		X		X				X	X
22. Hi-rel, mil, mil-temp	X		X		X							
23. Low standby current	X	X			X	X	X	X	X	X		
24. Design security	X	X									X	X