

The “Absolute Maximum Ratings” table in the Xilinx Data Book restricts the signal-pin voltage to a maximum 500 mV excursion above V_{CC} and below ground. The reason for this tight specification is to prevent uncontrolled current in the input-clamping ESD-protection diodes. Such tight specifications are common in the industry; some manufacturers limit the excursion to 300 mV.

This specification seems to be clean and simple, but it is violated in almost every practical design. When users put modern CMOS devices on PC boards, and interconnect them with unterminated traces, there are reflections, commonly called “ringing”, that cause overshoots and undershoots of substantial amplitude (2 V and more). The recent migration to smaller device geometries has made the IC outputs even faster and increased the slew-rate, causing more reflections even on short PC-board traces.

Fortunately, this problem has an easy solution:

The concern is not the input voltage, but rather the current through the input protection diode and other input structures. Excessive current can cause latch-up if it exceeds hundreds of milliamps AND if it lasts for microseconds (shorter duration current spikes do not activate the SCR-like latch-up mechanism).

PC-board reflections, on the other hand, usually have a short duration of just a few nanoseconds, and have an impedance of 40 to 100 Ω , which makes them incapable of causing latch-up. They don't drive enough current and they don't last long enough to cause any harm.

Here is the new Xilinx specification:

“Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to $V_{CC} + 2.0$ V, provided this over- or undershoot lasts less than 20 ns”.

