



XC3300A/L HardWire™ Array Design Verification Form

Company Name _____ Customer Name _____
Address _____ City _____ State _____ Zip _____
Telephone () _____ Fax () _____
Customer Internal Part Number _____
FPGA File Name and Revision Date _____
Xilinx HardWire Array Device # _____ Temp. Grade (Check One) ☐ C ☐ I
(see cross reference table in HardWire Data Book for correct part number)
☐ 5 V ☐ 3.3 V (Check One) Package _____

HardWire Array Options:

Input Voltage Levels TTL _____ CMOS _____ (for low voltage)
Power On Reset Time Interval 64 μ s _____ 16 ms _____ "Instant On" _____
Internal Reset Release Before I/O's _____ After I/O's _____ (forced to "After I/Os with "Instant On")
D/P Pull-up Resistor Yes _____ No _____
Oscillator Inactive _____ Active _____ Active/2 _____
Master Mode Selectable (Controlled by M0) _____ Unselectable (Forced On) _____
Boundary Scan: ☐ Not Used ☐ Always Active ☐ Active When M1 is High ☐ Active When M1 is Low
If Boundary Scan enabled: Pin assignment for TCK: _____ Pin assignment for TDO: _____
Pin assignment for TDI: _____ Pin assignment for TMS: _____

Package Marking Options:

☐ Custom Marking Form Attached ☐ Standard Xilinx Marking
Customer Part Marking for Device Package (Optional - 11 Characters max.)

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HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

- ☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.
- ☐ I certify that the above listed Design File and the revision date is the correct design.
- ☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.
- ☐ I authorize Xilinx to start the HardWire fabrication process.

Customer Name _____ Signature _____ Date _____

For Xilinx Use Only

Xilinx HardWire Design Center Manager: _____ Signature _____ Date _____
Xilinx Review Number (HD Code): _____
Xilinx Customer Service: _____ Signature _____ Date _____
NRE PO Number: _____
Xilinx Product Engineering Manager: _____ Signature _____ Date _____
Xilinx Part Number (HPC Code): _____
Mask Set _____ Hole Mask _____ Program Code _____