



# XH4000EX, XC4400/E, XC5400, XH8100 HardWire™ Array Design Verification Form

Company Name \_\_\_\_\_ Customer Name \_\_\_\_\_

Address \_\_\_\_\_ City \_\_\_\_\_ State \_\_\_\_\_ Zip \_\_\_\_\_

Telephone ( ) \_\_\_\_\_ Fax ( ) \_\_\_\_\_

Customer Internal Part Number \_\_\_\_\_

FPGA File Name and Revision Date \_\_\_\_\_

Xilinx HardWire Array Device # \_\_\_\_\_

Temp. Grade (Check One) ☐ C ☐ I

(see cross reference table in HardWire Data Book for correct part number)

☐ 5 V ☐ 3.3 V (Check One)

Package \_\_\_\_\_

## HardWire Array Options:

Configuration Mode:

☐ Master Serial

☐ Slave Serial

(not applicable to XH8100)

☐ Master Parallel Up

☐ Master Parallel Down

☐ Peripheral Synchronous

☐ Peripheral Asynchronous

☐ Express™ Mode

☐ None

Configuration Mode Emulation Needed? ☐ No ☐ Yes

Boundary Scan Emulation Needed? ☐ Always ☐ Only prior to configuration ☐ Never

## Package Marking Options:

☐ Custom Marking Form Attached ☐ Standard Xilinx Marking

Customer Part Marking for Device Package (Optional - 11 Characters max.)

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## HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

- ☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.
- ☐ I certify that the above listed Design File and the revision date is the correct design.
- ☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.
- ☐ I authorize Xilinx to start the HardWire fabrication process.

Customer Name \_\_\_\_\_ Signature \_\_\_\_\_ Date \_\_\_\_\_

### For Xilinx Use Only

Xilinx HardWire Design Center Manager: \_\_\_\_\_ Signature \_\_\_\_\_ Date \_\_\_\_\_

Xilinx Review Number (HD Code): \_\_\_\_\_

Xilinx Customer Service: \_\_\_\_\_ Signature \_\_\_\_\_ Date \_\_\_\_\_

NRE PO Number: \_\_\_\_\_

Xilinx Product Engineering Manager: \_\_\_\_\_

Xilinx Part Number (HPC Code): \_\_\_\_\_

Mask Set \_\_\_\_\_ Hole Mask \_\_\_\_\_