

# PCI Master Interface, PCI Slave Interface

February, 1997

Product Description

## Features

- Fully 2.1 PCI compliant 32 bit, 33MHz PCI Interface
  - ◊ Master (Initiator/Target), LC-DI-PCIM-C
  - ◊ Slave (Target-only), LC-DI-PCIS-C
- Pre-defined implementation for predictable timing in Xilinx XC000E FPGAs or HardWire (see *LogiCORE Facts* for listing of supported devices)
- Fully verified design
  - ◊ Simulated using VirtualChips™ PCI testbench
  - ◊ Tested in hardware (silicon proven)
- Configurable on-chip FIFO can be added for maximum burst speed (see *Xilinx Documents* section)
- 100% programmable single-chip solution with customizable back-end functionality
- Design Once™ - automatic conversion to HardWire for cost reduction
- Supported Initiator functions (PCI Master only)
  - ◊ Initiate Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL) commands
  - ◊ Initiate I/O Read, I/O Write commands
  - ◊ Initiate Configuration Read, Configuration Write commands
  - ◊ Bus Parking
- Supported Target functions (PCI Master and Slave)
  - ◊ Type 0 Configuration Space Header
  - ◊ Up to 2 Base Address Registers (memory or I/O with adjustable block size from 16 bytes to 256 Mbytes, slow decode speed)
  - ◊ Parity Generation (PAR), Parity Error Detection (PERR# and SERR#)
  - ◊ Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Real Line (MRL), Memory Write, Invalidate (MWI) commands
  - ◊ I/O Read, I/O Write commands
  - ◊ Configuration Read, Configuration Write commands
  - ◊ 32-bit data transfers, burst transfers with linear address ordering
  - ◊ Target Abort, Target Retry, Target Disconnect
  - ◊ Full Command/Status Register

## LogiCORE™ Facts

### PCI Master and Slave Interfaces V1.1.0

Core Specifics		
XC4000E		
CLBs Used	152 - 268	
IOBs Used (Master/Slave)	53/51	
System Clock $f_{\max}$	$\leq 33\text{MHz}$	
Device Features Used	Bi-directional data buses SelectRAM™ (optional user FIFO) Boundary scan (optional)	
Supported Devices <sup>1</sup> /Resources Remaining		
	I/O <sup>2</sup>	CLBs <sup>2</sup>
XC4013E PQ160 (Slave only)	76	308 - 424
XC4013E PQ208/HQ208 (Master/Slave)	107/109	308 - 424
XC4013E HQ240 (Slave only)	141	308 - 424
XC4020E HQ208 <sup>3</sup> (Slave only)	107	516 - 632
XC4020E HQ240 <sup>3</sup> (Slave only)	141	516 - 632
Provided with Core		
Documentation	User's Guide PCI Interface Protocol Checklist V1.0 to V1.1 Comparison	
Design File Formats	VIEWlogic schematics	
Verification Tool	VIEWlogic command files	
Schematic Symbols	VIEWlogic	
Constraint Files	TimeSpecs, RPMs, Guide files	
Evaluation Model	None	
Reference designs & application notes	Example design	
Additional Items	Reference book, PCI System Architectures	
Design Tool Requirements		
Xilinx Core Tools	XACTstep 5.2.1/6.0.1	
Entry/Verification Tools	Powerview V5.3.2 Workview Office V7.1.2 or V7.2	
Additional Information		
Netlist instantiatable in VHDL and Verilog		
VHDL and Verilog simulation model generated by user		
Support		
Xilinx provides technical support for this LogiCORE product when used as described in the User's Guide or supporting Application Notes. Xilinx cannot guarantee timing, functionality, or support of the product if implemented in devices not listed above, or customized beyond that referenced in the product documentation, or if any changes are done in sections of the design marked as "DO NOT MODIFY"		

#### Notes

- 1) Speed grade is determined by PCI configuration and user back-end, see Figure 3. Choice of speed grade
- 2) The exact number of CLBs and IOBs depends on user configuration of the core and level of resource sharing with adjacent logic.
- 3) Available on Xilinx Home Page, in the LogiCORE PCI VIP Lounge <http://www.xilinx.com/products/logicore/logicore>

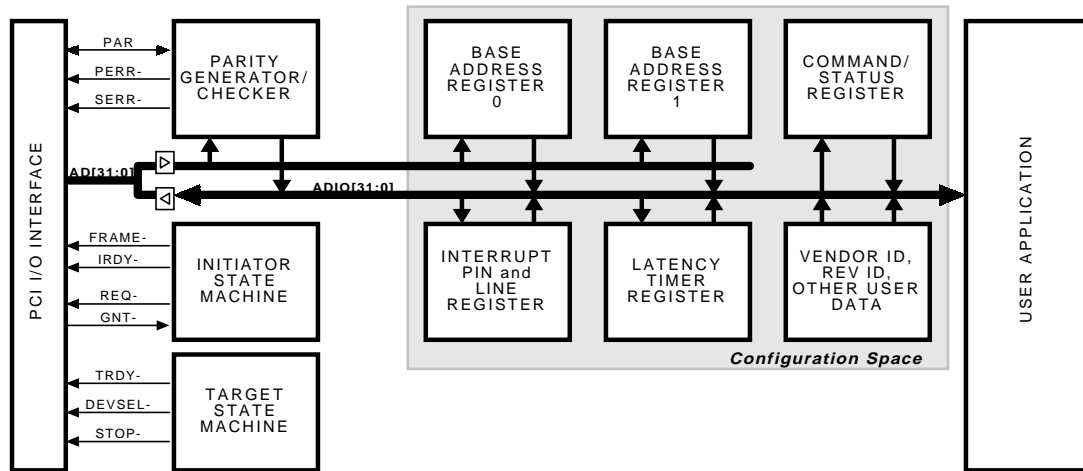


Figure 1. LogiCORE PCI Interface Block Diagram

## Potential Applications

- Add-in boards such as graphic cards, video adapters, LAN adapters and data acquisition boards.
- Embedded applications within telecommunication and industrial systems.

## General Description

The LogiCORE™ Master and Slave Interfaces are pre-implemented and fully tested modules for Xilinx XC4000E FPGAs (see LogiCORE Facts for listing of supported devices). The pin-out and the relative placement of the internal Configurable Logic Blocks (CLBs) are pre-defined. Critical paths are controlled by TimeSpec's to ensure that timing is always met. This significantly reduces engineering time required to implement the PCI portion of your design. Resources can instead be focused on the unique back-end logic in the FPGA and the system level design. As a result, the LogiCORE™ PCI products can cut your development time by several months.

Xilinx XC4000E Series FPGAs enables designs of fully PCI-compliant systems. The devices meet all required electrical and timing parameters including AC output drive characteristics, input capacitance specifications (10pF), 7 ns setup and 0 ns hold to system clock, and 11 ns system clock to output. The *PCI Compliance Checklist XC4000E* has additional details (see the *Xilinx Documents* section). Other features that enable efficient implementation of a complete PCI system in the XC4000E includes:

- Select-RAM™ memory: on-chip ultra-fast RAM with synchronous write option and dual-port RAM option. Used in the PCI Interfaces to implement the FIFO.
- Individual output enable for each I/O
- Internal 3-state bus capability
- 8 global low-skew clock or signal distribution networks
- IEEE 1149.1-compatible boundary scan logic support

See *Xilinx 1996 Data Book* for more details.

The module is carefully optimized for best possible performance and utilization in the XC4000E FPGA architecture. Implemented in the XC4013, more than 50% of the FPGA's resources remain for integrating a unique back-end interface and other system functions into a fully programmable one-chip solution. Xilinx DesignOnce™ service allows an automatic conversion to a low cost Hard-Wire™ device for high-volume production.

## Functional Description

The LogiCORE PCI Master Interface is partitioned into five major blocks, plus the user application, shown in Figure 1. Each block is described below.

### PCI I/O Interface Block

The I/O interface block handles the physical connection to the PCI bus including all signaling, input and output synchronization, output three-state controls, and all request-grant handshaking for bus mastering.

### Parity Generator/Checker

Generates/checks even parity across the AD bus, the CBE lines, and the PAR signal. Reports data parity errors via PERR- and address parity errors via SERR-.

### Target Control Logic

This block manages control over the PCI interface for Target functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus Specification*. The controller is a high-performance state machine using state-per-bit (one-hot) encoding for maximum performance. State-per-bit encoding has narrower and shallower next-state logic functions that closely match the Xilinx FPGA architecture.

### Initiator Control Logic (PCI Master only)

This block manages control over the PCI interface for Initiator functions. The states implemented are a subset of equations defined in "Appendix B" of the *PCI Local Bus*

**Specification.** The Initiator Control Logic also uses state-per-bit encoding for maximum performance.

### PCI Configuration Space

This block provides the first 64 bytes of Type 0, version 2.1, Configuration Space Header (CSH) (see table 1) to support software-driven “Plug-and Play” initialization and configuration. This includes Command, Status, and two Base Address Registers (BARs). These BARs illustrate how to implement memory- or I/O-mapped address spaces. Each BAR sets the base address for the interface and allows the system software to determine the addressable range required by the interface. Using a combination of Configurable Logic Block (CLB) flip-flops for the read/write registers and CLB look-up tables for the read-only registers results in optimized packing density and layout.

**Table 1. PCI Configuration Space Header**

31	16		15	0	
Device ID			Vendor ID		00h
Status			Command		04h
Class Code				Rev ID	08h
BIST	Header Type	Latency Timer	Cache Line Size		0Ch
Base Address Register 0 (BAR0)					10h
Base Address Register 1 (BAR1)					14h
Base Address Register 2 (BAR2)					18h
Base Address Register 3 (BAR3)					1Ch
Base Address Register 4 (BAR5)					20h
Base Address Register 5 (BAR5)					24h
Cardbus CIS Pointer					28h
Subsystem ID		Subsystem Vendor ID			2Ch
Expansion ROM Base Address					30h
Reserved					34h
Reserved					38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line		3Ch

**Note:** Shaded address locations are not implemented in the LogiCORE PCI Interface default configuration. These locations return zero during configuration read accesses.

### User Application with Optional Burst FIFOs

The LogiCORE PCI Interface provides a simple, general-purpose interface with a 32-bit data path and latched address for de-multiplexing the PCI address/data bus. The general-purpose user interface allows the rest of the device to be used in a wide range of applications.

Typically, the user application contains burst FIFOs to increase PCI system performance (Application Note is available, see the *Xilinx Documents* section). An on-chip read/write FIFO, built from the on-chip synchronous dual-port RAM (SelectRAM™) available in XC4000E devices, support data transfers in excess of 33 MHz.

### Core Customization

The LogiCORE PCI Interface can easily be customized to fit unique system requirements. Following customization is supported by the LogiCORE product and described in accompanying documentation.

- Initiator or target functionality (PCI Master only)

- Base Address Register configuration (1 - 2 Registers, size and mode)
- Configuration Space Header ROM
- Initiator and target state machine (e.g., termination conditions, transaction types and request/transaction arbitration)
- Burst functionality
- User Application including FIFO (back-end design)

### Supported PCI Commands

Table 2 illustrates the PCI bus commands supported by the LogiCORE PCI Interface. The *LogiCORE™ PCI Interface Protocol Checklist (2.1)* has more details on supported and unsupported commands (see the *Xilinx Documents* section).

**Table 2. PCI Bus Commands**

CBE [3:0]	Command	PCI Master	PCI Slave
0000	Interrupt Acknowledge	No*	Ignore
0001	Special Cycle	No*	Ignore
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No*	Ignore
1110	Memory Read Line	Yes	Yes
1111	Memory Write Invalidate	No*	Yes

\* The Initiator can present these commands, however, they either require additional user-application logic to support them or have not been thoroughly tested.

### Burst Transfer

The PCI bus derives its performance from its ability to support burst transfers. The performance of any PCI application depends largely on the size of the burst transfer. A FIFO to support PCI burst transfer can efficiently be implemented using the XC4000E on-chip RAM feature, SelectRAM™. Each XC4000E CLB supports two 16x1 RAM blocks. This corresponds to 32 bits of single-ported RAM or 16 bits of dual-ported RAM, with simultaneous read/write capability. Table 3 provides a summary of different FIFO sizes and performance in a XC4000E-2.

**Table 3. XC4000E-2 Synchronous FIFO modules**

Depth x Width	# CLBs	Single port performance	Equivalent dual-port performance
16x16	23	65 MHz	130 MHz
32x8	28	50 MHz	100 MHz
64x8	48	50 MHz	100 MHz
16x32	48	50 MHz	100 MHz

To reliably perform a burst transfer in a generic PCI system the LogiCORE Interface automatically inserts a wait

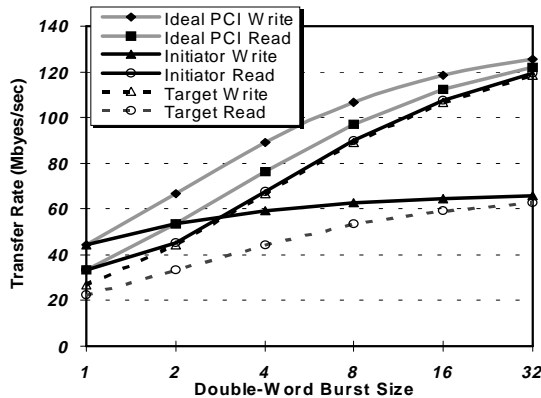
state when it is supplying data to the PCI bus. Consequently, the LogiCORE Interface can accept data at 100% burst transfer rate and supply data at 50%. See table 4 for a PCI bus transfer rates for various operations.

**Table 4. LogiCORE PCI transfer rates**

Operation	Transfer Rate
Initiator Write (PCI ← LogiCORE)	3-2-2-2
Initiator Read (PCI → LogiCORE)	4-1-1-2
Target Write (PCI → LogiCORE)	5-1-1-1
Target Read (PCI ← LogiCORE)	6-2-2-2

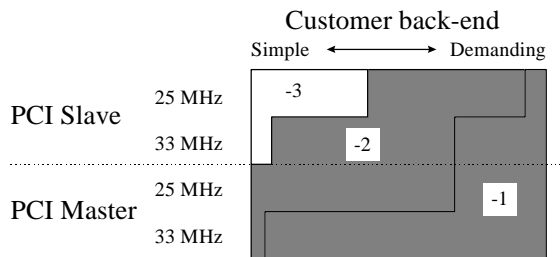
**Note:** Initiator Read and Target Write operations have effectively the same bandwidth for burst transfer.

The resulting PCI bus bandwidth is shown in figure 2.


**Figure 2. PCI Bus bandwidth**

## Pin Description

The LogiCORE™ PCI Master and Slave Interfaces support the PCI-SIG recommended pin-out for add-in cards. Table 7 to 9 describes the pin-out for the LogiCORE PCI Master and Slave Interfaces.


**Figure 3. Choice of speed grade**

## Timing Specification

The XC4000E family, together with the LogiCORE PCI products enables design of fully compliant PCI systems. The choice of FPGA speed grade for your PCI application is determined by the PCI configuration and your back-end design as illustrated in Figure 3. Factors affecting your back-end designs include loading of hot signals coming directly from the PCI bus, gate count and floorplanning. Table 5 shows the key timing parameters for the Logi-

CORE PCI Interfaces that must be met for full PCI compliance.

**Table 5. Timing Parameters [ns]**

Parameter	Ref.	PCI Spec.		LogiCORE PCI, XC4000E-2	
		Min	Max	Min	Max
CLK Cycle Time		30	∞	30 <sup>1</sup>	∞
CLK High Time		11		11	
CLK Low Time		11		11	
CLK to Bus Signals Valid <sup>4</sup>	T <sub>ICKOF</sub>	2	11	2 <sup>2</sup>	9.4 <sup>3</sup>
CLK to REQ# and GNT# Valid <sup>4</sup>	T <sub>ICKOF</sub>	2	12	2 <sup>2</sup>	9.4 <sup>3</sup>
Tri-state to Active		2		2 <sup>2</sup>	
CLK to Tri-state			28		28 <sup>1</sup>
Bus Signals Setup to CLK (IOB)	T <sub>PSU</sub>		7		6 <sup>3</sup>
Bus Signals Setup to CLK (CLB)			7		7 <sup>1</sup>
GNT# Setup to CLK	T <sub>PSU</sub>		10		6 <sup>3</sup>
Inputs Hold Time After CLK (IOB)	T <sub>PH</sub>		0		0 <sup>3</sup>
Inputs Hold Time After CLK (CLB)			0		0 <sup>2</sup>
RST# to Tri-state			40		40 <sup>2</sup>

Notes:

- 1) Controlled by TimeSpecs, included in product
- 2) Verified by analysis and bench-testing
- 3) Advanced speed grade data
- 4) IOB configured for Fast slew rate

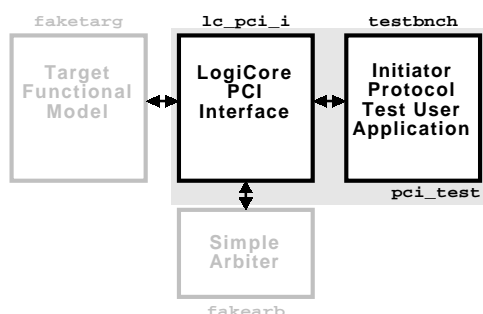
## Verification Methods

The LogiCORE PCI Interfaces have been extensively simulated using the VirtualChips VHDL PCI test bench from Phoenix Technologies, Ltd. (not included with the LogiCORE™ PCI products). The Interface has also been verified in hardware in the XC4013E-2 PQ208C FPGA.

Included with the LogiCORE™ PCI Master and Slave Interface is an example design and a VIEW<sup>logic</sup> based PCI protocol test bench that verifies the PCI interface functions according to the test scenarios specified in the *PCI Local Bus Specification* see Figure 4. This test bench consists of 28 test scenarios, each designed to test compliance to a specific PCI bus operation. Refer to the *LogiCORE PCI Interface Protocol Checklist* for a complete list of supported test scenarios (see the *Xilinx Documents* section).

## Recommended Design Experience

The LogiCORE PCI interface is pre-implemented allowing engineering focus at the unique back-end functions of a PCI design. Regardless, PCI is a high-performance system that is challenging to implement in any technology, ASIC or FPGA. Therefore, we recommend previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, Floorplanner, TIMESPECs, and guide files. The challenge to implement a complete PCI design including back-end functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.



**Figure 4. PCI Protocol Testbench**

## Ordering Information

Table 6 shows the part numbers for the LogiCORE™ products. Before placing an order, please read and sign the attached LogiCORE™ license agreement and fax it to Xilinx at (408) 879 4780. For pricing and availability please contact your local Xilinx sales office.

**Table 6. Part numbers**

Product	Part number	Supplier
LogiCORE™ PCI Master Interface	LC-DI-PCIM-C	Xilinx, Inc.
LogiCORE™ PCI Slave Interface	LC-DI-PCIS-C	Xilinx, Inc.

## Related Information

### Recommended Design Centers

Listed below are design centers and design consultants that have experience with the LogiCORE PCI products.

HighGate Design  
12380 Saratoga-Sunnyvale Road, Suite 8  
Saratoga, CA 95070-3090, USA  
TEL: (408) 255-7160 FAX: (408) 255-7162  
E-MAIL: [highgate@highgatedesign.com](mailto:highgate@highgatedesign.com)  
WEB: <http://www.highgatedesign.com>

Memec Design Services  
1819 S. Dobson Rd, Ste. 203  
Mesa, Arizona 85202, USA  
TEL: (602) 491-4311 FAX: (602) 491-4907  
E-MAIL: [info@mds.memec.com](mailto:info@mds.memec.com)  
WEB: <http://www.mds.memec.com>

Comit Systems  
1250 Oakmead Pkwy, Suite 210  
Sunnyvale, CA 94088, USA  
TEL: (408) 988-2988 FAX: (408) 988-2133  
E-MAIL: [preeth@comit.com](mailto:preeth@comit.com)  
WEB: <http://www.comit.com>

### PCI Special Interest Group (PCI-SIG) Publications

The PCI-SIG publishes various PCI specifications and related documents such as *PCI Local Bus Specification*, *PCI Compliance Checklist* and *PCI System Design Guide*.

PCI Special Interest Group  
2575 NE Kathryn St #17  
Hillsboro, OR 97124  
TEL: (800) 433-5177 (inside the US)  
TEL: +1 503 693-6232 (outside the US)  
FAX: (503) 693-8344  
Office hours: 8:30am - 4:00pm PST  
E-MAIL: [info@pcisig.com](mailto:info@pcisig.com)  
WEB: <http://www.pcisig.com>

### Xilinx Documents

More PCI related information is available on Xilinx Web:  
<http://www.xilinx.com/products/logicore>.

**Table 7. PQ160 package pin-out (LogiCORE PCI Slave in XC4013E)**

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
P1	GND	P19	GND	P37	I/O,SGCK2	P55	AD1	P73	I/O	P91	GND	P109	I/O	P127	I/O(CS1,A2)	P145	I/O
P2	CLK (A16)	P20	VCC	P38	O (M1)	P56	AD0	P74	I/O	P92	I/O	P110	GND	P128	I/O (A3)	P146	I/O
P3	AD22 (A17)	P21	DEVSEL-	P39	GND	P57	I/O	P75	I/O	P93	I/O	P111	I/O	P129	I/O	P147	AD31(A10)
P4	AD21	P22	STOP-	P40	I (M0)	P58	I/O	P76	I/O	P94	I/O (D5)	P112	I/O	P130	I/O	P148	AD30(A11)
P5	AD20	P23	LOCK-	P41	VCC	P59	I/O (INIT-)	P77	I/O	P95	I/O (CS0-)	P113	I/O (D1)	P131	GND	P149	AD29
P6	TDI	P24	PERR-	P42	I (M2)	P60	VCC	P78	I/O,SGCK3	P96	I/O	P114	I/O (RCLK-, RDY/BUSY-)	P132	I/O	P150	AD28
P7	TCK	P25	SERR-	P43	I/O,PGCK2	P61	GND	P79	GND	P97	I/O	P115	I/O	P133	I/O	P151	GND
P8	AD19	P26	PAR	P44	I/O (HDC)	P62	I/O	P80	DONE	P98	I/O (D4)	P116	I/O	P134	I/O (A4)	P152	AD27
P9	AD18	P27	I/O	P45	AD8	P63	I/O	P81	VCC	P99	I/O	P117	I/O (D0,DIN)	P135	I/O (A5)	P153	AD26
P10	GND	P28	CBE1	P46	CBE0	P64	I/O	P82	PROGRAM-	P100	VCC	P118	I/O,SGCK4 (DOUT)	P136	I/O	P154	AD25(A12)
P11	AD17	P29	GND	P47	AD7	P65	I/O	P83	RST- (D7)	P101	GND	P119	CCLK	P137	I/O	P155	AD24(A13)
P12	AD16	P30	AD15	P48	I/O (LDC-)	P66	I/O	P84	I/O,PGCK3	P102	I/O (D3)	P120	VCC	P138	I/O	P156	CBE3
P13	TMS	P31	AD14	P49	AD6	P67	I/O	P85	I/O	P103	I/O (RS-)	P121	TDO	P139	I/O (A6)	P157	IDSEL
P14	CBE2	P32	AD13	P50	AD5	P68	I/O	P86	I/O	P104	I/O	P122	GND	P140	I/O (A7)	P158	AD23(A14)
P15	I/O	P33	AD12	P51	GND	P69	I/O	P87	I/O (D6)	P105	I/O	P123	I/O(A0,WS-)	P141	I/O	P159	I/O,SGCK1 (A15)
P16	FRAME-	P34	AD11	P52	AD4	P70	GND	P88	I/O	P106	I/O (D2)	P124	I/O,PGCK4 (A1)	P142	GND	P160	VCC
P17	IRDY-	P35	AD10	P53	AD3	P71	I/O	P89	I/O	P107	I/O	P125	I/O	P143	I/O		
P18	TRDY-	P36	AD9	P54	AD2	P72	I/O	P90	I/O	P108	I/O	P126	I/O	P144	I/O		

**Table 8. PQ208, HQ208 package pin-out (LogiCORE PCI Master and Slave in XC4013E and XC4020E\*\*)**

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
P1	N.C.	P25	GND	P49	GND	P73	I/O	P97	I/O	P121	I/O	P145	I/O	P169	I/O	P193	AD30
P2	GND	P26	VCC	P50	I (M0)	P74	I/O	P98	I/O	P122	I/O (D5)	P146	I/O	P170	I/O	P194	GND
P3	N.C.	P27	LOCK-	P51	N.C.	P75	I/O	P99	I/O	P123	I/O (CS0)	P147	I/O (D1)	P171	GND	P195	AD29
P4	CLK (A16)	P28	PERR-	P52	N.C.	P76	I/O	P100	I/O,SGCK3	P124	I/O	P148	I/O (RCLK-, RDY/BUSY-)	P172	I/O	P196	AD28
P5	I/O (A17)	P29	SERR-	P53	N.C.	P77	I/O (INIT-)	P101	GND	P125	I/O	P149	I/O	P173	I/O	P197	AD27
P6	AD23	P30	PAR	P54	N.C.	P78	VCC	P102	N.C.	P126	I/O	P150	I/O	P174	I/O (A4)	P198	AD26
P7	AD22	P31	REQ-*	P55	VCC	P79	GND	P103	DONE	P127	I/O	P151	I/O (D0,DIN)	P175	I/O (A5)	P199	AD25 (A12)
P8	TDI	P32	CBE1	P56	I (M2)	P80	I/O	P104	N.C.	P128	I/O (D4)	P152	I/O,SGCK4 (DOUT)	P176	I/O	P200	AD24 (A13)
P9	TCK	P33	AD15	P57	I/O,PGCK2	P81	I/O	P105	N.C.	P129	I/O	P153	CCLK	P177	I/O	P201	CBE3
P10	AD21	P34	AD14	P58	I/O (HDC)	P82	I/O	P106	VCC	P130	VCC	P154	VCC	P178	I/O	P202	I/O
P11	AD20	P35	AD13	P59	CBE0	P83	I/O	P107	N.C.	P131	GND	P155	N.C.	P179	I/O	P203	IDSEL (A14)
P12	AD19	P36	AD12	P60	AD7	P84	I/O	P108	PROGRAM-	P132	I/O (D3)	P156	N.C.	P180	I/O (A6)	P204	I/O, GCK1 (A15)
P13	AD18	P37	GND	P61	AD6	P85	I/O	P109	RST- (D7)	P133	I/O (RS-)	P157	N.C.	P181	I/O (A7)	P205	VCC
P14	GND	P38	AD11	P62	I/O (LDC-)	P86	I/O	P110	I/O,PGCK3	P134	I/O	P158	N.C.	P182	GND	P206	N.C.
P15	AD17	P39	AD10	P63	AD5	P87	I/O	P111	I/O	P135	I/O	P159	TDO	P183	VCC	P207	N.C.
P16	AD16	P40	AD9	P64	AD4	P88	I/O	P112	I/O	P136	I/O	P160	GND	P184	I/O (A8)	P208	N.C.
P17	TMS	P41	AD8	P65	AD3	P89	I/O	P113	I/O (D6)	P137	I/O	P161	I/O(A0,WS-)	P185	I/O (A9)		
P18	CBE2	P42	I/O	P66	AD2	P90	GND	P114	I/O	P138	I/O (D2)	P162	I/O,PGCK4 (A1)	P186	I/O		
P19	GNT-*	P43	I/O	P67	GND	P91	I/O	P115	I/O	P139	I/O	P163	I/O	P187	I/O		
P20	FRAME-	P44	I/O	P68	AD1	P92	I/O	P116	I/O	P140	I/O	P164	I/O	P188	I/O		
P21	IRDY-	P45	I/O	P69	AD0	P93	I/O	P117	I/O	P141	I/O	P165	I/O(CS1,A2)	P189	I/O		
P22	TRDY-	P46	I/O	P70	I/O	P94	I/O	P118	I/O	P142	GND	P166	I/O (A3)	P190	I/O (A10)		
P23	DEVSEL-	P47	I/O,SGCK2	P71	I/O	P95	I/O	P119	GND	P143	I/O	P167	I/O	P191	I/O (A11)		
P24	STOP-	P48	O (M1)	P72	I/O	P96	I/O	P120	I/O	P144	I/O	P168	I/O	P192	AD31		

\* PCI Master (Initiator) only, \*\* Only PCI Slave supported in XC4020E

**Table 9. HQ240 package pin-out (LogiCORE PCI Slave in XC4013E and XC4020E)**

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
P1	GND	P28	STOP-	P55	I/O	P82	I/O	P109	I/O	P136	I/O	P163	I/O	P190	I/O	P217	I/O
P2	CLK (A16)	P29	GND	P56	I/O	P83	N.C.	P110	I/O	P137	I/O	P164	I/O	P191	I/O	P218	I/O
P3	I/O (A17)	P30	VCC	P57	I/O,SGCK2	P84	I/O	P111	I/O	P138	I/O	P165	I/O	P192	I/O	P219	N.C.
P4	AD23	P31	LOCK-	P58	O (M1)	P85	I/O	P112	I/O	P139	I/O	P166	GND	P193	I/O	P220	I/O (A10)
P5	AD22	P32	PERR-	P59	GND	P86	I/O	P113	I/O	P140	VCC	P167	I/O	P194	I/O	P221	I/O (A11)
P6	TD1	P33	SERR-	P60	I (M0)	P87	I/O	P114	I/O	P141	I/O (D5)	P168	I/O	P195	N.C.	P222	VCC
P7	TCK	P34	PAR	P61	VCC	P88	I/O	P115	I/O	P142	I/O (CS0-)	P169	I/O	P196	GND	P223	I/O
P8	AD21	P35	I/O	P62	I (M2)	P89	I/O (INIT-)	P116	I/O	P143	N.C.	P170	I/O	P197	I/O	P224	I/O
P9	AD20	P36	CBE1	P63	I/O,PGCK2	P90	VCC	P117	I/O	P144	I/O	P171	I/O	P198	I/O	P225	AD31
P10	AD19	P37	N.C.	P64	I/O (HDC)	P91	GND	P118	I/O,SGCK3	P145	I/O	P172	I/O	P199	I/O	P226	AD30
P11	AD18	P38	I/O	P65	CBE0	P92	I/O	P119	GND	P146	I/O	P173	I/O (D1)	P200	I/O	P227	GND
P12	I/O	P39	I/O	P66	AD7	P93	I/O	P120	DONE	P147	I/O	P174	I/O (RCLK-, RDY/BUSY-)	P201	VCC	P228	AD29
P13	I/O	P40	VCC	P67	AD6	P94	I/O	P121	VCC	P148	I/O (D4)	P175	I/O	P202	I/O (A4)	P229	AD28
P14	GND	P41	AD15	P68	I/O (LDC-)	P95	I/O	P122	PROGRAM-	P149	I/O	P176	I/O	P203	I/O (A5)	P230	AD27
P15	AD17	P42	AD14	P69	AD5	P96	I/O	P123	RST- (D7)	P150	VCC	P177	I/O (D0,DIN)	P204	N.C.	P231	AD26
P16	AD16	P43	AD13	P70	AD4	P97	I/O	P124	I/O, PGCK3	P151	GND	P178	I/O,SGCK4 (DOUT)	P205	I/O	P232	AD25 (A12)
P17	TMS	P44	AD12	P71	AD3	P98	N.C.	P125	I/O	P152	I/O (D3)	P179	CCLK	P206	I/O	P233	AD24 (A13)
P18	CBE2	P45	GND	P72	AD2	P99	I/O	P126	I/O	P153	I/O (RS-)	P180	VCC	P207	I/O	P234	I/O
P19	VCC	P46	I/O	P73	I/O	P100	I/O	P127	I/O	P154	I/O	P181	TDO	P208	I/O	P235	I/O
P20	I/O	P47	I/O	P74	I/O	P101	VCC	P128	I/O	P155	I/O	P182	GND	P209	I/O (A6)	P236	CBE3
P21	I/O	P48	AD11	P75	GND	P102	I/O	P129	I/O (D6)	P156	I/O	P183	I/O(A0,WS-)	P210	I/O (A7)	P237	I/O
P22	N.C.	P49	AD10	P76	AD1	P103	I/O	P130	I/O	P157	I/O	P184	I/O,PGCK4 (A1)	P211	GND	P238	IDSEL(A14)
P23	I/O	P50	AD9	P77	AD0	P104	I/O	P131	I/O	P158	N.C.	P185	I/O	P212	VCC	P239	I/O,SGCK1 (A15)
P24	FRAME-	P51	AD8	P78	I/O	P105	I/O	P132	I/O	P159	I/O (D2)	P186	I/O	P213	I/O (A8)	P240	VCC
P25	IRDY-	P52	I/O	P79	I/O	P106	GND	P133	I/O	P160	I/O	P187	I/O(CS1,A2)	P214	I/O (A9)		
P26	TRDY-	P53	I/O	P80	VCC	P107	I/O	P134	I/O	P161	VCC	P188	I/O (A3)	P215	I/O		
P27	DEVSEL-	P54	I/O	P81	I/O	P108	I/O	P135	GND	P162	I/O	P189	I/O	P216	I/O		

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