

Graphically based, XACT^{step}™ Floorplanner makes it easy to achieve hand-crafted levels of performance and density

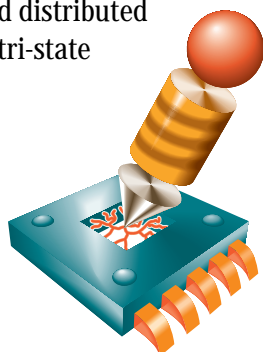
The PLD industry's first full-featured, hierarchical Floorplanner makes it easy for any designer to achieve hand-crafted levels of performance and density.

With just a few minutes of basic floorplanning, designers can quickly place critically-timed logic and graphically plan their data flow. Placement is done at a high level using the design hierarchy and a floorplan of the device.

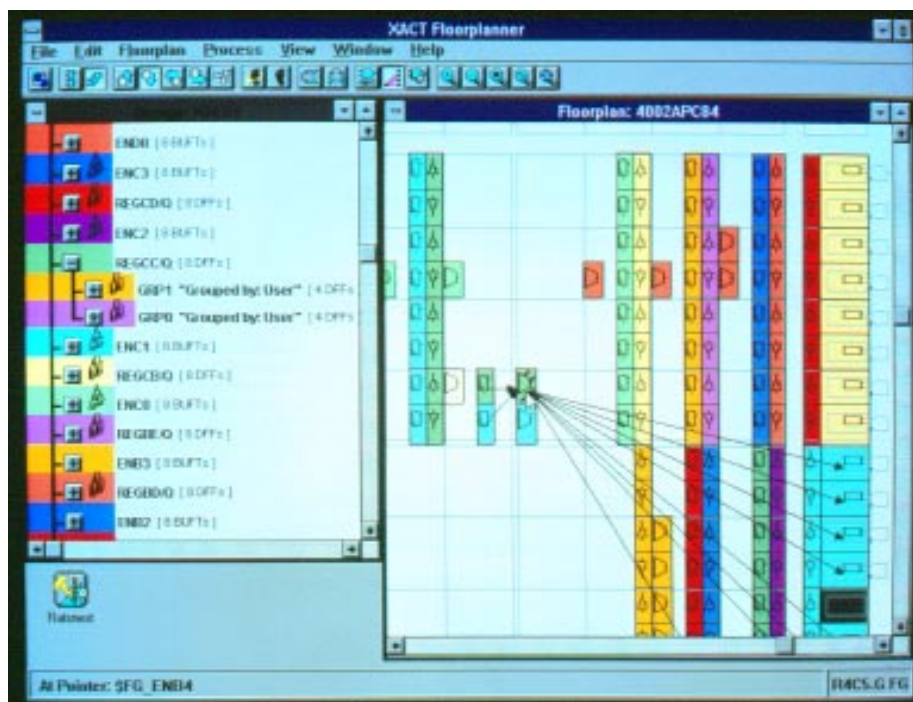
Designers that need the highest levels of performance can easily implement a detailed floorplan employing proven optimization techniques such as bus interleaving, register grouping and I/O pin alignment.

Benefits include speed and density improvements methodologies and increases in productivity over time consuming, manual techniques.

Floorplanning is especially effective for designs that are high density or highly structured and designs that take advantage of specialized resources like the Xilinx high-speed distributed RAM and tri-state internal busses.



X_S A_T C_E T_P



Software Highlights

Basic Floorplanning

- Easy to learn using on-line, interactive tutorial
- Drag and drop elements into your floorplan
- Graphically plan your dataflow
- Place critically timed logic elements
- Place structured design elements
- Optimize high-speed distributed RAM structures
- Easily view FPGA resources required for any level of the design

Detailed Floorplanning

- Align TBUFS with common enables
- Interleave busses
- View interconnect ratsnest
- Easily analyze net congestion
- Rearrange hierarchy without modifying schematic
- Use powerful search and find capabilities
- Use interactive rip-up and redo
- Capture results to placement map for reuse

When to Floorplan

The Floorplanner allows designers to easily pass their knowledge about a design to the automatic tools. They can quickly place structured design elements and graphically plan their data flow. The placement is done at a high level using their own design hierarchy and a floorplan of the device.

This powerful technique is especially effective for designs that are high density, contain a lot of structured logic or push the limits of performance for a given technology.

Design Flow With Floorplanning

Floorplanning is an optional step that is done before or after design implementation. When used before implementation, the Floorplanner creates a set of constraints that are used by the automatic placement and routing tools. When used after implementation, the Floorplanner makes it easy to analyze and further optimize placement.

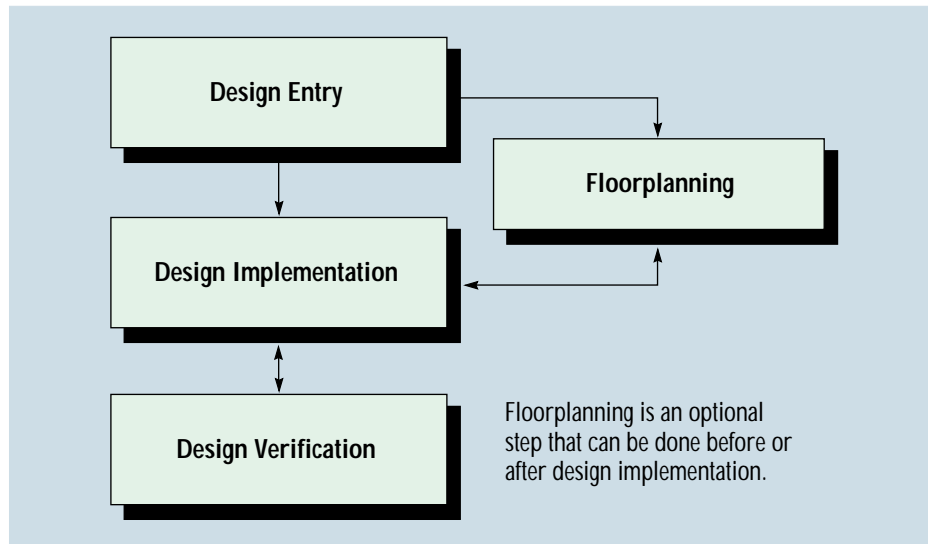
The Floorplanner can also place and route a design incrementally by interactively calling the automatic tools.

Using the Floorplanner

The Floorplanner presents designers with a graphical view of their design labeled with original schematic or HDL names. By expanding or collapsing the hierarchy, the designer can easily view the FPGA resources required for any level of the design.

Using the mouse pointer, the designer selects a hierarchical group and drags it onto the floorplan of the device. The tool displays a ratsnest of connections between the new group and all the logic currently placed on the die.

Users direct the tool to place logic elements vertically or horizontally or they assign the logic to an area of the die and let the automatic tools determine the optimal block assignments.



Using this process, logic with critical timing or density requirements are easily grouped together and placed on the die.

Throughout the process, powerful features in the Floorplanner assist the designer. Search and find commands make it easy to locate specific logic elements. Ratsnests views make it easy to align structures and use long lines and tri-state buffers efficiently.

Once the designer finds an optimal placement for their logic they can capture it to a placement map and impose it on similar structures in the design. This makes it easy to tile repeated logic or reuse portions of the design in future projects.

Powerful Floorplan Analysis

Once the floorplan is complete, a powerful set of commands make it easy to analyze its efficiency. These commands can also be used to examine results of the automatic placement tools.

The Check Floorplan command verifies resource allocation, tri-state buffer alignment and CLB packing. If errors or warnings are found, a dialog box is used to navigate to the problem spot with a single click.

For more detailed analysis designers can view ratsnest connections for any resource and display a routing congestion map for each CLB.

The Floorplanned Design

Whether the design requires a few minutes of basic floorplanning or detailed analysis and optimization, designers can experience a boost in engineering productivity and significant improvements in performance and density.

Devices Supported

The Floorplanner can be used for all devices in the XC3000A, XC4000 and XC5000 families.

Ordering Information

The Floorplanner is available with XACT^{step} version 6 Standard and version 5.2, Extended packages.

Platforms Supported

PC with Microsoft Windows 3.1 or DOS, Sun and Hewlett Packard Workstations

Sales Offices

Corporate Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124 U.S.A.
Tel: 1 (408) 559-7778
FAX: 1 (408) 559-7114

Europe England

Xilinx, Ltd.
Suite 1B, Cobb House
Oyster Lane, Byfleet
Surrey KT14 7DU
United Kingdom
Tel: (44) 1932-349401
FAX: (44) 1932-349499

Asia

Japan

Xilinx K. K.
Daini-Nagaoka Bldg. 2F,
2-8-5, Hatchobori Chuo-ku.
Tokyo 104, Japan
Tel: 81-33-297-9191
FAX: 81-33-297-9189

Hong Kong

Xilinx Asia Pacific
Unit No. 2308-2319
Tower 1, Metroplaza
Hing Fong Road
Kwai Fong, N.T.
Hong Kong
Tel: (852) 2-410-2739
FAX: (852) 2-494-7159



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