

## Summary

This Application Note contains additional information that may be of use when designing with the XC4000 families of devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

## Xilinx Family

XC4000/XC4000A/XC4000H

## Introduction

This application note describes the electrical characteristics of the output drivers, their static output characteristics or I/V curves, the additional delay caused by capacitive loading, and the ground bounce created when many outputs switch simultaneously.

## Voltage/Current Characteristics of XC4000-Family Outputs

Figures 1 through 4 show the output source and sink currents, both drawn as absolute values. Note that the XC4000 families have an n-channel only, totem-pole like output structure that pulls a High output to a voltage level that is one threshold drop lower than  $V_{CC}$ . When driving inputs that have a 1.4-V threshold, this lower  $V_{OH}$  offers faster speed and more symmetrical switching delays. The XC4000H outputs offer an optional p-channel output driver and thus rail-to-rail switching a configuration option for each individual pin.

These curves represent typical devices. Measurements were taken at  $V_{CC} = 5\text{ V}$ ,  $T = 25^\circ\text{C}$ . These characteristics vary by manufacturing lot, and will be affected by future changes in minimum device geometries, notably a change from  $0.8\text{ }\mu\text{m}$  to  $0.6\text{ }\mu\text{m}$ . These characteristics are not production-tested as part of the normal device test procedure; they can, therefore, not be guaranteed. Although these measurements show that the output sink and source capability far exceeds the guaranteed data sheet limits, continuous high-current operation beyond the data sheet limits can cause metal migration of the on-chip metal traces, permanently damaging the device. Output currents in excess of the data-sheet limits are, therefore, not recommended for continuous operation. These output characteristics can, however, be used to calculate or model output transient behavior.

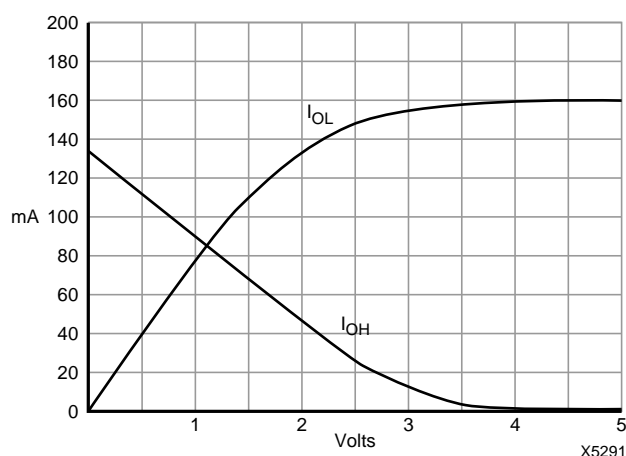


Figure 1. Output Voltage/Current Characteristics for XC4005-5

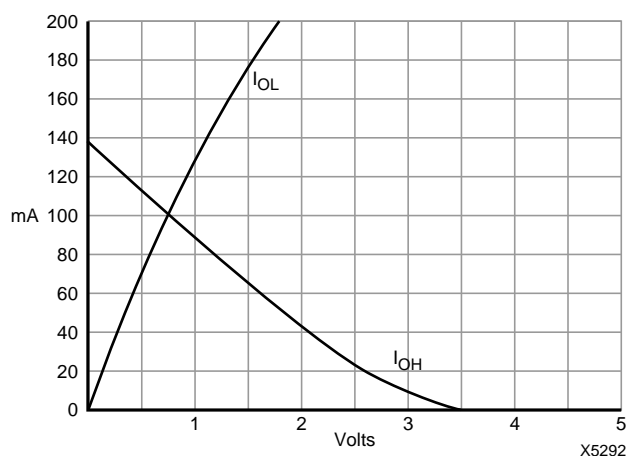
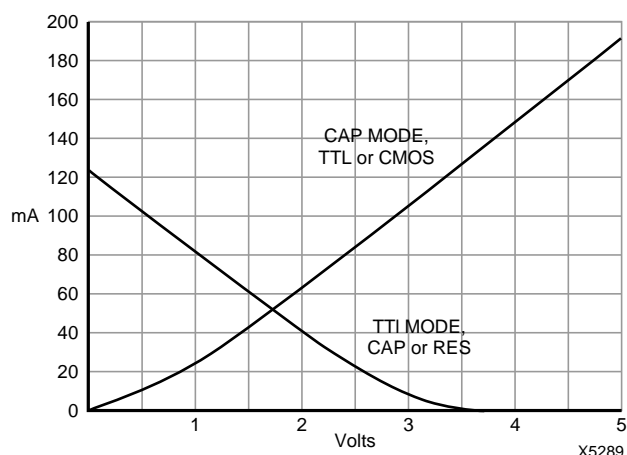


Figure 2. Output Voltage/Current Characteristics for XC4002A



**Figure 3. Output Voltage/Current Characteristics for XC4005H**

### Additional Output Delays When Driving Capacitive Load

Xilinx Product Specifications in Section 2 give guaranteed worst-case output delays with a 50-pF load.

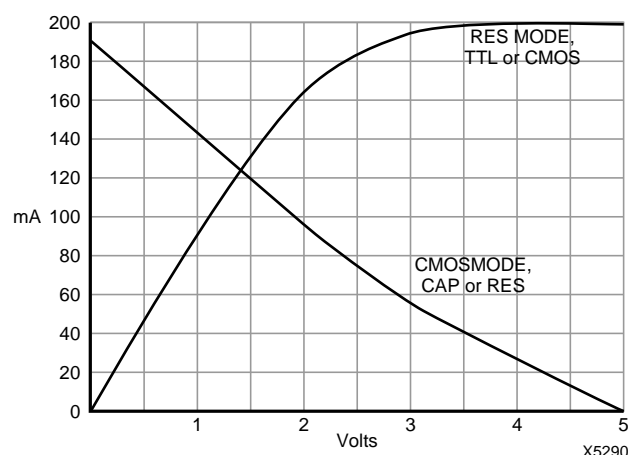
The values given in Table 1 are actual measurements on a small number of mid-93 production XC4005-5, XC4005A-5 and XC4003H-5 devices, all in PQ208 packages, measured at room temperature and  $V_{CC} = 5.5$  V. Listed is the additional output delay, measured crossing 1.5 V, relative to the delays specified in this 1994 Data Book, Section 2.

These parameters are not part of the normal production test flow, and can, therefore, not be guaranteed.

**Table 1. Increase in Output Delay When Driving Light Capacitive Loads (<150 pF)**

Family	Slew Mode	High-to-Low			Low-to-High			pF	
		10	50	100	10	50	100		
XC4000	Slow	-1.6	0*	1.4	-1.4	0*	1.4	ns	
	Fast	-1.6	0*	1.2	-1.2	0*	1.1	ns	
XC4000A	Slow	-2.2	0*	1.7	-1.5	0*	1.4	ns	
	MedSlow	-1.8	0*	1.6	-1.3	0*	1.1	ns	
	MedFast	-1.8	0*	1.3	-1.3	0*	1.1	ns	
	Fast	-2.0	0*	1.2	-1.0	0*	1.3	ns	
XC4000H	Cap-CMOS	-2.2	0*	1.9	-0.5	0*	0.7	ns	
	Res-CMOS	-1.4	0*	1.2	-1.0	0*	0.8	ns	
	Cap-TTL	-1.9	0*	1.6	-1.2	0*	1.2	ns	
	Res-TTL	-1.1	0*	1.0	-1.1	0*	1.0	ns	

\*Zero by definition.



**Figure 4. Output Voltage/Current Characteristics for XC4005H**

Table 2 lists the additional output delay, measured crossing 1.5 V, relative to the delay with 100 pF load shown in Table 1.

Example:

$\Delta T$  High-to-Low for XC4005-5 with Fast-mode output driving 250 pF:

$$1.2 \text{ ns (from Table 1) plus } (250-100) \text{ pF} \cdot 1.5 \text{ ns/100 pF} \\ = 1.2 \text{ ns} + 2.25 \text{ ns} = 3.45 \text{ ns}$$

Total propagation delay, clock OK to pad:

$$T_{OKPOF} + 3.45 \text{ ns} = 7.0 \text{ ns} + 3.45 \text{ ns} = 10.45 \text{ ns}$$

**Table 2. Increase in Output Delay When Driving Heavy Capacitive Loads (>150 pF)**

Family	Slew Mode	High-to-Low		Low-to-High	
		10	50		
XC4000	Slow	1.7	1.2	ns/100 pF	
	Fast	1.5	1.2	ns/100 pF	
XC4000A	Slow	2.1	1.2	ns/100 pF	
	MedSlow	1.5	1.1	ns/100 pF	
	MedFast	1.0	1.1	ns/100 pF	
	Fast	0.9	1.1	ns/100 pF	
XC4000H	Cap-CMOS	2.7	0.9	ns/100 pF	
	Res-CMOS	1.8	1.0	ns/100 pF	
	Cap-TTL	2.1	1.3	ns/100 pF	

## Ground Bounce in XC4000 Devices

Ground-bounce is a problem with high-speed digital ICs, when multiple outputs change state simultaneously causing undesired transient behavior on an output, or in the internal logic. This is also referred to as the Simultaneous Switching Output (SSO) problem. Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC-internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously. Ground bounce affects outputs that are supposed to be stable Low, and it also affects all inputs since they interpret the incoming level by referencing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input will be interpreted as a short pulse with a polarity opposite to the ground bounce.

$V_{CC}$  bounce is not as important as ground bounce, because it is of lower magnitude due to the weaker pull-up transistors. Also, the noise immunity in the High state is usually better than in the Low state, and input levels are referenced to ground, not  $V_{CC}$ . All this is the result of our industry's TTL heritage.

### Test Method

Data was taken on XC40005-5, XC40005A-5, and XC40003H-5 devices, all in the PQ208 package, soldered to the Xilinx Ground Bounce Test Board. Pin 82, two pins away from the nearest ground pin, was configured as a permanently Low output driver, effectively monitoring the inter-

nal ground level. The simultaneously switching outputs were on pins 80 and 83, for two outputs switching; additionally, pins 80 and 86 were used for four outputs switching (81 and 84 on the XC40003H). The closest ground pins are 79 and 90.

Four ground-bounce parameters were measured at room temperature, with  $V_{CC}$  set at 5.5 V as shown in Figure 1.

$V_{OLP-HL}$	Peak ground noise when outputs switch High-to-Low
$V_{OLV-HL}$	Valley ground noise when outputs switch High-to-Low
$V_{OLP-LH}$	Peak ground noise when outputs switch Low-to-High
$V_{OLV-LH}$	Valley ground noise when outputs switch Low-to-High

All four parameters can affect system reliability.

The two positive peak values can cause problems with a signal leaving the ground-bounce chip, driving another chip. The positive ground bounce voltage is added to the  $V_{OL}$ , and may exceed the receiving input's noise margin. A continuously logic Low input may thus be interpreted as a short-duration High pulse.

The two negative valley parameters can cause problems with a signal arriving at the ground-bounce chip, where the on-chip ground reference is negative, reducing the Low-level noise immunity. The incoming voltage may not be Low enough, and may, therefore, be interpreted as a short-duration High input pulse.

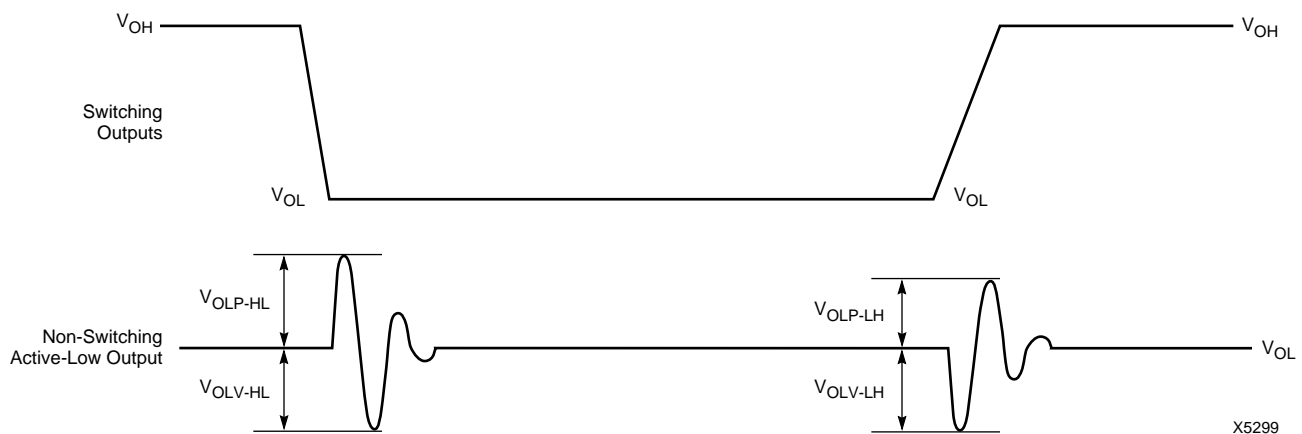


Figure 5. Ground Bounce

**Table 3. Ground Bounce, 16 Outputs Switching, Each With 50 pF Load,  $V_{CC} = 5.5\text{ V}$**

Family	Slew Mode	High-to-Low		Low-to-High		mV
		$V_{OLP}$	$V_{OLV}$	$V_{OLP}$	$V_{OLV}$	
XC4000	Slow	670	480	240	240	mV
	Fast	1,170	710	480	660	mV
XC4000A	Slow	565	425	290	310	mV
	MedSlow	950	610	500	780	mV
	MedFast	1,140	860	500	780	mV
	Fast	1,240	910	500	810	mV
XC4000H	Cap-CMOS	940	660	660	770	mV
	Res-CMOS	1,250	1,210	590	480	mV
	Cap-TTL	830	460	450	570	mV
	Res-TTL	1060	980	440	350	mV

### Interpretation of the results

Ground bounce is a linear phenomenon. When multiple outputs switch, the total ground bounce is the sum of the ground-bounce values caused by individual outputs switching. Since the actual switching of multiple outputs is usually not quite simultaneous, small timing differences between the switching outputs, caused by routing delays, can indirectly affect the amplitude. With low capacitive loading, < 50 pF, the peaks and valleys might even partially cancel each other. With larger capacitive loads, the tendency is for valleys to combine with valleys and peaks to combine with peaks.

In most devices tested, the load capacitance does not directly affect the ground-bounce **amplitude**, but it does affect the **duration** of the ground-bounce signals.

On the fastest outputs, minimal load capacitance created a ground-bounce resonant frequency of 340 MHz, with a half-cycle time of 1.5 ns. Such a signal exceeds 90% of its peak amplitude for about 0.4 ns.

With a 50 pF load on the switching outputs, the ground bounce resonant frequency is 85 to 97 MHz, with a half-cycle time of 5 to 6 ns, staying 1.7 ns above 90% of peak amplitude.

With a 150 pF load on the switching outputs, the ground bounce resonant frequency is 40 to 60 MHz, with a half-cycle time of 8 to 12 ns, staying 3 ns above 90% of peak amplitude.

The main problem with large load capacitances is not an increase in amplitude, but rather an increase in duration of the ground-bounce signal. The amplitude is mainly affected by the number of outputs switching simultaneously, and by the slew-rate mode of these outputs. Switching outputs closer to the monitoring output also cause larger peaks and valleys than outputs further away.

**Table 4. Ground Bounce, 16 Outputs Switching, Each With 150 pF Load,  $V_{CC} = 5.5\text{ V}$**

Family	Slew Mode	High-to-Low		Low-to-High		mV
		$V_{OLP}$	$V_{OLV}$	$V_{OLP}$	$V_{OLV}$	
XC4000	Slow	740	330	210	280	mV
	Fast	1,180	420	350	710	mV
XC4000A	Slow	615	270	245	330	mV
	MedSlow	960	310	820	370	mV
	MedFast	1,140	620	370	790	mV
	Fast	1,200	640	370	810	mV
XC4000H	Cap-CMOS	1,080	390	470	860	mV
	Res-CMOS	1,500	820	420	590	mV
	Cap-TTL	900	250	320	610	mV
	Res-TTL	1,170	660	300	470	mV

### Guidelines for reducing ground-bounce effects

- Minimize the impedance of the system ground distribution network and its connection to the IC pins. PQFPs are best suited, PGAs are worst, and PLCCs are in-between.
- Use PC-boards with ground- and  $V_{CC}$ -planes, connected directly to the ICs' supply pins. Place decoupling capacitors very close to these ground and  $V_{CC}$  pins.
- Keep the ground plane as undisturbed as possible. A row of vias can easily cause a dynamic ground-voltage drop.
- Keep the clock inputs physically away from the outputs that create ground bounce, and connect clocks to input pins that are close to a ground pin. Make sure that all clock and asynchronous inputs have ample noise margin, especially in the Low state.
- If possible, avoid simultaneous switching by staggering output delays, e.g. through additional local routing of signals or clocks.
- Spread simultaneously switching outputs around the IC periphery. For a 16-bit bus, use two outputs each on either side of four ground pins.

### Ground-Bounce vs Delay Trade-Off

After the external sources of ground bounce have been reduced or eliminated, the designer can trade reduced ground bounce for additional delay by selecting between families and slew-rate options. Figures 2 and 3 show the available choices, based on 16 outputs switching simultaneously High-to-Low.

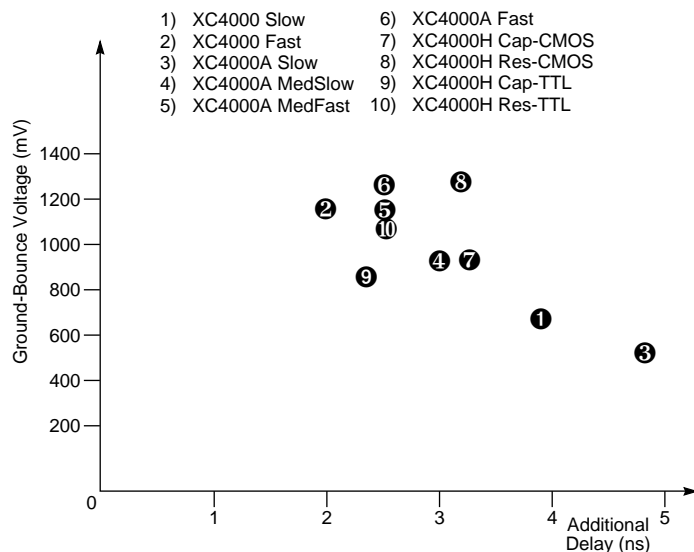
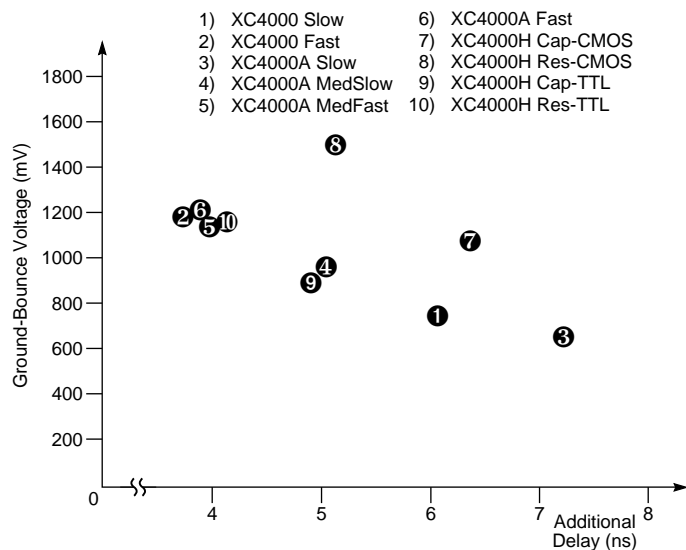


Figure 6. Ground-Bounce vs Delay Trade-off for 16 Outputs Switching 50 pF each

### Summary

For light capacitive loads, the XC4000 and XC4000A, both in slow mode perform well, with ground bounce below 800 mV; the additional delay, compared to fast mode, is only 4 to 5 ns. For larger capacitive loads, the XC4000H in Capacitive-TTL mode offers the best trade-off.



X5250

Figure 7. Ground-Bounce vs Delay Trade-off for 16 Outputs Switching 150 pF each