



Design Migration from XC4000 to XC4000E

XAPP 062 October 15,1996 (Version1.0)

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Summary

The XC4000E is an enhanced architecture based on the XC4000 family, but offers many new features, particularly Select-RAM™ memory. When converting XC4000, XC4000A, XC4000D, and XC4000H designs, the XC4000E is an excellent choice. The conversion process may be as simple as downloading the same bitstream into the XC4000E device (XC4000 and XC4000D bitstreams only), or it may involve changes to the schematic or HDL code. This Application Note describes techniques that should be employed to convert from any of the XC4000, XC4000A, XC4000D, or XC4000H families to the XC4000E family.

Xilinx Family

XC4000E

Demonstrates

Techniques for migrating XC4000 designs to the XC4000E architecture

Introduction

Some variations of the XC4000 family are no longer recommended for new designs. These include the XC4000 standard family, XC4000A, XC4000D, and XC4000H (referred to in this application note as the older XC4000 families). These have been superseded by the newer XC4000 Series families, which include the XC4000E, XC4000L, XC4000EX, and XC4000XL families. Designs in the older versions of the XC4000 can be converted to the new XC4000 Series. In some cases, particularly for XC4000D designs or other designs not including RAM, the XC5200 family should be considered for its lower cost. For a discussion of converting XC4000 family designs to the XC5200 family, see the Xilinx application note XAPP060, "Design Migration from XC4000 to XC5200."

Converting an older XC4000 design to an XC4000E design may or may not require schematic changes. Except for certain I/O capabilities, the XC4000E architecture offers a superset of the architectural features in the older XC4000 families, in addition to many new enhancements. (See [Table 1](#).) Therefore, if none of the special I/O features in the XC4000A or XC4000H are used, the conversion becomes merely a matter of selecting the XC4000E speed grade that will give comparable performance, and recompiling the design targeting the selected device. If retargeting an XC4000 or XC4000D design, in fact, the XC4000E can actually accept the original bitstream. XC4000A and XC4000H designs must be recompiled.

Table 1: Comparison of Features in XC4000 Families

	XC4000	XC4000A	XC4000D	XC4000H	XC4000E
Output Drive/Pin (mA)	12	24	12	4/24	12
Output Slew Rate Options	Fast, Slow	Fast, Slow, Medium Fast, Medium Slow	Fast, Slow	SoftEdge/Resistive load	Fast, Slow
RAM	Yes	Yes	No	Yes	Yes
I/O Registers	Yes	Yes	Yes	No	Yes
Input Thresholds	TTL only	TTL only	TTL only	TTL or CMOS, per I/O	TTL or CMOS, Global
Output High Levels	TTL only	TTL only	TTL only	TTL or CMOS, per I/O	TTL or CMOS, Global
Wide Edge Decoders (per edge)	4	2	4	4	4
Speed Grades	-6, -5, -4	-6, -5, -4	-6, -5, -4	-6, -5	-4, -3, -2

Enhancements

The XC4000E offers a number of architectural improvements to the XC4000. Although the simplest conversion path uses only the resources provided in the originally targeted older XC4000 device, a design can be altered to take advantage of these features if desired.

- **PCI Compliance:** Fully compliant for -3 speed grades and faster.
- **Select-RAM Memory:** In addition to the XC4000 modes, RAM can now be configured for synchronous, edge-triggered Write operation or for dual-port RAM with simultaneous Read/Write. Also, XC4000E RAM can now be configured with user-defined initial values at power-up.
- **Increased System Speed:** Improvements in both device processing and system architecture result in path performance benefits that may have significant impact on the critical paths in a design.
- **More Flexible H Function Generator:** Additional inputs gives this resource the capability of being either partially or fully independent of the other two function generators, increasing the logic capacity and routability of the device.
- **Input/Output Block (IOB) Clock Enable:** I/O flip-flops have clock enables, making them more useful in many applications.
- **Increased Global Access to F and G Function Generators:** More function generator inputs are available to global routing resources, increasing flexibility and performance.
- **CMOS Threshold Compatibility:** Both inputs and/or outputs can be globally programmed for CMOS threshold compatibility.
- **Increased Carry Logic Speed:** The speed of the carry logic chain has increased dramatically, doubled in some cases.
- **Soft Startup:** When the configuration process is complete, outputs programmed for fast slew-rate operation are initially kept slow, avoiding ground-bounce problems when all the outputs are switched on.
- **Configuration Pin Pull-up Resistors:** During configuration, the three mode pins, M0, M1, and M2, have weak pull-up resistors. The effect on converted designs is discussed in ["Configuration" on page 2](#).

Design Guidelines & Considerations

Because the XC4000E is a superset of the older XC4000 architecture, migrating a design from one of the older families to the XC4000E is relatively straightforward. The following issues may need to be addressed.

Configuration

The XC4000E can be configured using the same bitstream as an XC4000 or XC4000D device, or the design can be altered and recompiled to take advantage of some of the new features available in the XC4000E. XC4000A and XC4000H designs must be recompiled, targeting the new device.

One of the new features in the XC4000E is the addition of weak (50 k Ω) pull-up resistors to the configuration mode pins. These internal resistors make it possible to configure in Serial Slave mode (the most common configuration mode) without the addition of any external resistors. Older XC4000 families did not include these pull-up resistors, therefore a high-value pull-down resistor was acceptable to establish a Low value on any of these inputs. The XC4000E requires a resistor value of less than 7 k Ω to reliably generate a logic Low on the input.

When converting from an older XC4000 device to an XC4000E, check the design for pull-down resistor values and change them, if necessary, to 4.7 k Ω resistors. Resistor values above the recommended level may prevent the XC4000E from properly configuring.

Footprint

Older XC4000 and XC4000E devices are footprint compatible for every common package. All control pins, configuration pins, and power pins are in the same locations. In general, no board re-layout is necessary when replacing an XC4000 device with an XC4000E.

An exception may occur when converting from an XC4000A or XC4000H to an XC4000E. In these transitions, the design is moved from a device with a maximum 24 mA sink current to one with a maximum 12 mA sink current, and it may be necessary to split the load across two outputs.

Design Performance

The XC4000E is available in -4, -3 and -2 speed grades. Consequently, the fastest XC4000E is significantly faster than any of the older XC4000 families. However, when converting an existing design, it is recommended that an XC4000E speed grade two grades faster than the original design be used for the initial compilation run. The resulting design should then be tested using XDelay, the Timing Analyzer, or timing simulation, to verify functionality at the required speed.

The reason for the recommended speed grade change is that the XC4000E is optimized for a three layer metal process and a higher overall system level performance, not for each individual specification. Although the majority of specifications are faster in the XC4000E than in any of the older XC4000 families, a few parameters are slower. The recommended approach should result in a successful conversion for the vast majority of designs.

After this first pass, it may be possible to use a slower speed grade. The best way to ensure that design performance will be met in the XC4000E is to use XACT-Performance™ to define the timing requirements of the design.

To place this suggestion in perspective, 80% of designs show equal or better performance in an XC4000E with the same speed grade as the original design. This conservative approach is recommended to maximize the chance that a given design will meet the required timing. See ["Reporting Performance at Various Speed Grades" on page 5](#) for a quick method of evaluating the performance of a single routed design in several different speed grades.

Development System

The XC4000E is supported by the same XACTstep™ development system and uses the basic software tools that support the older XC4000 families. A new XC4000E library has been added to the set of Unified Libraries to support the architectural features of the XC4000E.

A software version that supports the XC4000E must be used. Users who have upgraded to at least the 6.0.1 (Windows) or 5.2.1 (DOS and UNIX) versions of XACTstep have the XC4000E library features and the necessary place and route tools. Otherwise, contact the local Xilinx sales representative for the availability of the most recent upgrade.

Input/Output Pads

For XC4000A and XC4000H designs, the difference in I/O capabilities may affect the conversion to an XC4000E.

XC4000A to XC4000E

XC4000A I/O have a 24 mA output drive, while the XC4000E has only 12 mA. Where a 24 mA drive is required, use two pins tied together to double the drive. Add the FAST parameter where speed is important.

XC4000A I/O allow two additional slew rate options, Medium Fast (MEDFAST) and Medium Slow (MEDSLOW). These parameters, if used in an XC4000A design, will need to be changed to FAST in the XC4000E version to achieve higher-than-default speed.

XC4000H to XC4000E

XC4000H devices have a higher I/O count than the corresponding XC4000E devices. If a high I/O count is required, a larger XC4000E device must be used to provide the same number of pins, as shown in [Table 2](#).

Table 2: XC4000H Device Replacement Guide

XC4000H	Max. I/O	XC4000E	Max. I/O
XC4003H	160	XC4010E	160
XC4005H	192	XC4013E	192

XC4000H I/O have a default SoftEdge slew-rate control that limits drive to 4 mA. This is intended for capacitively loaded outputs, and can be selected with the CAP parameter. The alternative is the resistive (RES) mode, which increases drive to 24 mA. XC4000H designs will need the CAP or RES parameters removed when converted to the XC4000E. Add the FAST parameter where speed is important, and use two pins tied together to double the drive to 24 mA if necessary.

XC4000H I/O allow per-pin designation of CMOS or TTL thresholds and output levels, selected for each pin using a CMOS or TTL parameter (TTL is default). In the XC4000E, all input thresholds have the same value, and all output levels are the same, although the two are selected independently. If the XC4000H design has mixed I/O, the recommended approach is to designate the XC4000E inputs as TTL, since an input set for TTL can resolve both TTL and CMOS levels. The output level must depend on the destination devices. XC4000H designs will need the CMOS or TTL parameters removed when converted to the XC4000E.

Migration Methodology

If none of the new features in the XC4000E are used, an existing design can be compiled to the XC4000E using the XC4000 library, which supports all of the XC4000, XC4000A, XC4000D, and XC4000H families. If certain of the new features are to be used, new library components will be required. In this case, it is necessary to change the design to use the new XC4000E libraries. The features requiring the XC4000E library are:

- Synchronous (edge-triggered) or dual-port memory
- IOB clock enables

The library elements supporting these features are described in the *Libraries Supplement Guide*.

Because of the Xilinx Unified Library approach, a design can be migrated between families with a minimum of effort. The migration methodology itself is simple, and following the guidelines and considerations prescribed in this document will greatly improve the success of the migration.

This section describes how to perform the actual migration of an XC4000 design into the XC4000E library for three third-party CAE interfaces.

VIEWlogic

To migrate an XC4000 VIEWlogic schematic to the XC4000E library, perform the following steps:

1. Add the XC4000E library to the VIEWlogic library search path. Edit the `viewdraw.ini` file in the project directory and add the XC4000E library path so that it appears in `viewdraw.ini` before the path to the XC4000 library.
2. To convert the XC4000 alias to XC4000E, run `altran`, the VIEWlogic library alias maintenance program:

```
altran -l primary xc4000=xc4000e
```

where `xc4000` is the alias assigned to the XC4000 library, and `xc4000e` is the alias assigned to the XC4000E library.
3. Reprocess the design by running XMake or the Flow Engine.

Mentor

To migrate an XC4000 Mentor schematic to the XC4000E library, perform the following steps:

1. Invoke `PLD_DA` (it is not necessary to open the schematic).
2. On DA's desktop background (that is, outside of any schematic or symbol windows), call up the session pop-up menu with the mouse button on the right and select **Convert Design**.

Of the fields in the resulting dialog box these are the most relevant:
 3. **Select a group of designs from a list file?** Whether you answer "yes" or "no" to this question affects the following field.
 4. **Enter Design name (List file = no).** The name of the design to retarget. **Convert Design** does *not* traverse the hierarchy of a schematic.
 5. **Enter list file name (List file = yes).** A file which lists designs, one per line, to retarget. This is useful if your design has many lower-level schematics.

TIP: A list file can easily be created by typing:

```
ls *.mgc_component.attr | sed  
s/\.mgc_component.attr//g > listfile
```

The `ls` command lists all MGC components within a single directory. The `sed` command strips away the `.mgc_component.attr` trailer. The result is redirected to `listfile`.

6. **Schematic name.** The name of the schematic model (the default is "schematic").
7. **Check & Save switch.** Because all schematic sheets in **Convert Design** are literally re-drawn in Design Architect, you must apply **Check & Save** to each sheet. This switch controls whether to do this automatically. By default, this switch is set for manual checking because it allows you to spot Xilinx components that did not convert properly. Use the manual setting until you are comfortable with how **Convert Design** works and you are certain that all Xilinx components will convert properly.
8. **From Technology.** The device family from which you are converting (e.g., `XC4000`). This and the next field are case insensitive.
9. **To Technology.** The device family to which you are converting.
10. After filling out the fields in the dialog box and selecting "OK," you will see **Convert Design** doing its job directly in Design Architect.
11. Reprocess the design by running XMake or the Flow Engine.

Foundation

To migrate an XC4000 Foundation schematic to the XC4000E library, perform the following steps:

1. Select the **Project Type** option from the **Menu** file. Change **Family**, **Part**, and **Speed** settings, as desired, and click the **Change** button.
2. Open and save each schematic sheet macro. To do so, run the Schematic Editor and select the **open** option from the **File** menu. The Open Sheet window allows you to quickly open all project top-level sheets and project schematic macros. Inspect the Project Manager messages for any warnings and errors.
3. Re-synthesize and update all FSM and HDL macros. Use the hierarchy browser in the Project Manager to search the project for the macros.
4. Note: if your project contains components that are not available in the new system library, you have to modify the project so as to preserve its functionality. In the case of a top level HDL project, you will need to re-synthesize the entire project.
5. Reprocess the design by running XMake or the Flow Engine.

Additional Software Tips

Following are some additional tips that may help in converting a design.

Using the Old Design as a Guide

An XC4000 or XC4000D design can be used as a guide for an XC4000E design. Rename the old design, for example to "guide.lca", and add the following parameter when running PPR:

```
guide=guide.lca
```

Alternatively, in the Windows environment simply choose a previous XC4000 revision in the Guide File pull-down of the implementation window.

Converting a Routed LCA File

The XDelay "convert" option can be used to translate a routed XC4000 or XC4000D LCA file to an XC4000E. The syntax is as follows:

```
xdelay -convert <design name>.lca <part & package>  
<new name>.lca
```

For example, to convert an XC4003 to an XC4003E, type:

```
xdelay -convert old.lca 4003EPC84 new.lca
```

The conversion utility will not allow you to choose a speed grade or write delay information into the new LCA file, so to perform these steps, run XDelay again with the following syntax:

```
xdelay -w -u -<new speed> <design name>
```

For example:

```
xdelay -w -u -3 new.lca
```

This command writes the new speed grade and delay information into the file without otherwise changing the design.

Reporting Performance at Various Speed Grades

XDelay can be used to report performance at various speed grades without changing the LCA file. To show the delays of the most critical paths, create a short XDelay report using the following command:

```
xdelay -u -<speed> -o critical.rpt <design name>
```

For example:

```
xdelay -u -2 -o critical.rpt new.lca
```

This command produces a text file called critical.rpt that contains the minimum worst-case pad-to-setup, clock-to-setup, and clock-to-pad values allowable for each clock in the design. Effectively, this report provides all the information necessary to evaluate the performance of the new speed grade.

Alternatively, in the Windows environment use the Performance Summary in the Timing Analyzer. Both XDelay and the Timing Analyzer can also be used to examine specific path delays in more detail if desired.

Additional Information

If there are problems with the conversion process, please contact the Xilinx Technical Support hotline for assistance.

Email: hotline@xilinx.com (24 hours)

Voice: 1-800-255-7778 (6:30AM - 5PM PST)

FAX: 1-408-879-4442 (24 hours)



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