



XC4000E Select-RAM™: Flexibility with Speed

XBRF 001 July 1, 1996 (Version 1.0)

Application Brief

Summary

The Xilinx XC4000 Select-RAM offers the best size flexibility and at the same time offers high speed operation with very little waste.

Xilinx Family

XC4000E/EX

Introduction

FPGA Memory is used for two specific types of functions: System Integration functions such as control and status bits or Large Integrated memory functions for handling data, such as FIFOs etc. The new XC4000E with fast Dual-Port RAM efficiently implements both these types of RAM applications. Altera's Flex 10K series touted with limited number of Large, Slow and Inflexible RAM block, fails to perform the simplest of memory functions.

System Integration Functions

Frequently FPGA designs require a multiple, small, fast and configurable memories for system configuration, control and status functions. These memories are usually distributed all over the design. The XC4000E family fast Select-RAM memory at 4 ns, is ideal for such applications. As in

the XC4000 family, the XC4000E CLBs can be used as memory instead of logic "on demand". These memories can then be linked together for various data width or depth sizes.

Altera's large 2K bit memory blocks are wasteful because all of the memory within a block, is seldom utilized. Also, for most designs all of the blocks can not be utilized, wasting valuable silicon. And they are slow due to their large size; Altera datasheet says 20 ns. The table below compares the XC4000E memory implementation with the Altera Flex 10K for system Integration functions.

For example, when implementing a standard PCI 64 X 8 FIFO the XC4000E allows designers to instantiate multiple FIFOs with no wastage (see [Figure 1](#) and [Table 1](#)).

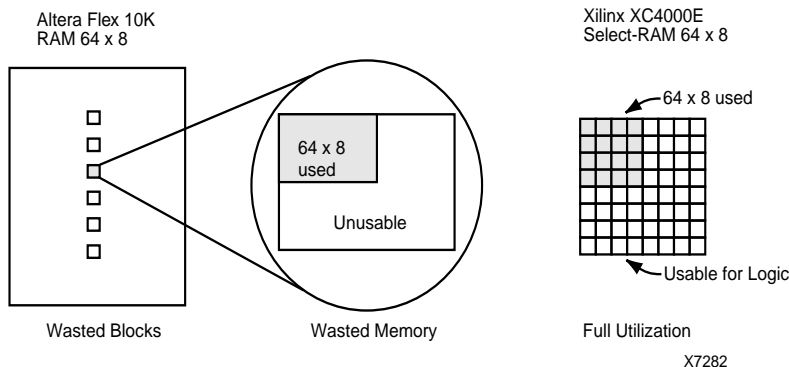


Figure 1: 64 x 8 FIFO Memory Utilization Comparison

Table 1: Memory Function Summary

Feature	Xilinx 4000E	Altera 10K	Design Impact of 10K
Dual-Port RAM	Dedicated	Emulated	- Half the Speed - Half the Memory
Performance for FIFO etc.	FAST(5-15 ns)	SLOW (20-40 ns)	- Limited to Slow Applications

Large Integrated Memory Functions

FPGA designs frequently implement large FIFOs/RAM Buffers especially in Datacomm and DSP intensive areas. Most FIFO/RAM Buffer functions require Dual Port RAMs along with fast speed. The Xilinx XC4000E Select-RAM now offers Dual-Port RAMs with independent access from both sides.

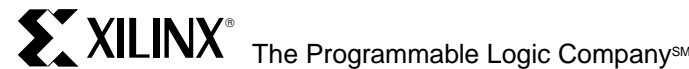
The Altera Flex 10K requires emulating dual-port RAM which cuts down the available memory size and speed in half! This makes a 20ns memory operate on certain key timings at a slow 40ns speed, eliminating a number of fast speed applications (see Table 1). The limited interconnect

capability of Flex devices complicates this (see Application Brief XBR 003) further slowing down the effective performance. Once again XC4000E with dual port RAM offers fast performance to address leading edge designs.

Finally Altera claims that the large memory blocks can be used for logic functions. At 20 ns speeds the RAM blocks implement slower logic than PALs used to do five years ago. tPD from input to output using Altera 10K for simple Address Decodes will take over 30 ns. That is four times longer than what a 386 microprocessor required five years ago!

Table 2: Select-RAM Feature Summary

Feature	Xilinx 4000E	Altera 10K	Design Impact of 10K
Flexibility	High	Low Large & Inflexible	Inflexible For Configuring Different Sizes Wasteful For Most Applications
Logic/Memory Trade-off	Logic or Memory On-Demand!	No Choice!	Unused blocks wasted
Performance	FAST (4-10 ns)	SLOW (20 ns)	Limited to Slow Applications!



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