

# X<sub>S</sub> A<sub>T</sub> C<sub>E</sub> T<sub>P</sub> V E R S I O N 6

The newest version of the Xilinx development system—named XACTstep, version 6—combines power and ease-of-use to provide the highest-productivity tool set in the programmable logic industry. Targeted for shipment in August, 1995, XACTstep runs under Microsoft Windows 3.1 on the PC and Motif on workstations.

XACTstep, version 6 features six powerful, easy-to-use tools intended for a wide range of programmable logic designs. On one end of the spectrum, simple PAL replacements can be implemented in EPLDs using fully automatic techniques. At the other end of the spectrum, large, complex FPGA designs can be fine-tuned using a configurable flow engine and the programmable logic industry's first graphically-based, hierarchical floorplanner.

The new graphical user interface (GUI) in XACTstep includes many features that shorten the learning curve and simplify design implementation and debug. With this GUI, programs are executed and options are set using tool bars and icons. Tool tips give instant descriptions of commands and on-line help provides more in-depth information. New report browsers display message files with "plain English" titles and allow the simultaneous viewing of multiple documents.

The results are faster implementation and debug cycles, a shorter learning curve and a dramatic boost in engineering productivity.

## Six Powerful New Tools

XACTstep contains six powerful new tools that accelerate design implementation, verification and debug cycles.

- The new *Design Manager* provides a complete project management environment for the XC2000, XC3000, XC3100,

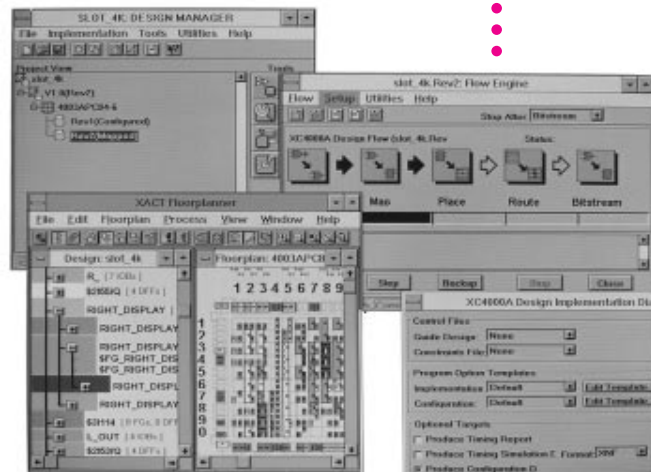
## A Revolutionary Combination of Power and Ease-of-Use

XC4000, XC5000 and XC7000 families.

It supports unlimited version control and manages all the underlying files for each design revision.

- The configurable *Flow Engine* lets users choose the desired amount of control over the implementation process. Users can choose a fully automatic flow or set break points that allow the analysis and optimization of results before proceeding to the next step.

For each step in the implementation process, the automatic tools can be easily

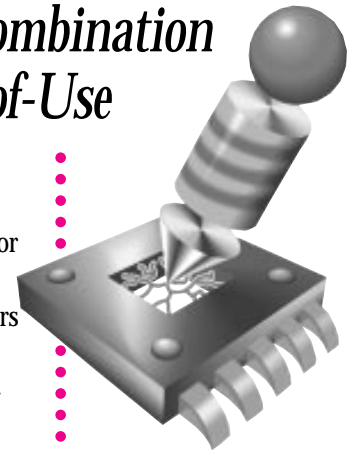


directed to achieve the desired result. For example, the automatic placement and routing tools can be set to optimize the design or minimize run time; the selection is made using a slide bar that appears in a pop-up menu.

The entire collection of settings can be stored in a template for later use. New users can choose from standard templates provided with the system. Experienced users can create an unlimited number of custom templates and distribute these to other members of their group.

For users who don't want to take advantage of the new, easy-to-use interface,

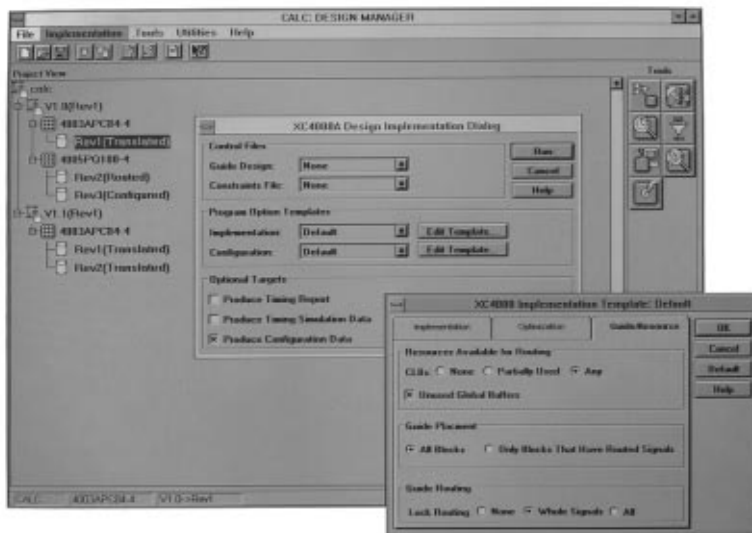
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all program options from XACT 5.0 can be entered using the old command line syntax.

- XACTstep contains a new graphics-based, hierarchical *floorplanner*. With XACT-Floorplanner™, users can easily achieve “hand-crafted” levels of performance and density in FPGA designs. (See related article on page 19).

Floorplanning is valuable for any design that has a high degree of structure or a large number of gates. With just a few minutes of basic floorplanning, designers can quickly place



critically-timed logic and graphically plan the data flow. Placement is performed at a high level using the designs' hierarchy and a floorplan of the target device. Floorplanning also allows optimal use of specialized FPGA architectural structures like high-speed distributed RAM and internal three-state buffers. Users needing to maximize performance can easily implement a detailed floorplan employing proven optimization techniques like bus interleaving, register grouping and I/O pin alignment.

- The interactive *Timing Analyzer* makes it easy to analyze the designs' performance with custom timing reports. Using pop-up menus, the tool can generate reports that show the delay along any

specific path or group of paths, such as all the paths of a certain type or those associated with specific clock signals. In addition, the *Timing Analyzer* can automatically compare the implemented design's actual performance to the goals entered using XACT-Performance™, and show the estimated maximum frequency for each clock in the design.

- The new *Hardware Debugger* provides for the verification of configuration data and the viewing of internal signal activity during system debug and test. It takes advantage of the re-programmable, SRAM-based devices by configuring the FPGA in-circuit using a cable connected to a host PC or workstation. After configuring the device, bitstream data is read back through the cable for automatic verification.

While the device is running, an unlimited number of internal nodes can be viewed, with the results displayed in a wave-form window. By giving the hardware debugger control of the system clock, designers can easily step through state machines and other synchronous circuits to verify functionality.

- The new graphics-based *PROM Formatter* in XACTstep creates PROM programming files. It chooses the best PROM size for the design, and automatically splits the data into multiple files if smaller PROMS are being used. Serial and byte-wide PROMS in four different formats are supported. If the target system includes a daisy chain of FPGAs, the PROM formatter graphically creates the load order and verifies the load sequence.

## Free To Users On Maintenance

Registered Xilinx development system owners with an active software maintenance agreement will receive the XACTstep, version 6 update automatically. To check on the status of your maintenance agreement, call Xilinx customer service at 408-559-7778, or contact your local Xilinx sales office. ♦