

3. Synthesis of the design's modules into XNF or EDIF netlists. The area and speed requirements should be specified before the design is synthesized.
4. Translation of the XNF file or EDIF file into a Xilinx Unified Library XNF file.
5. Functional simulation with a gate-level simulator (optional).
6. Floorplanning of structured design elements such as RPMs and on-chip memory blocks to improve routability and performance (optional).
7. Implementation of the design with the automated "place & route" tools.
8. Timing simulation with a gate-level simulator.

In summary, an increasing number of FPGA users are adopting top-down design methodologies using HDLs and logic synthesis. While still not a panacea, synthesis technology is starting to live up to its promise of enabling efficient, high-level FPGA design. ♦

Measuring Speed and Temperature

All CMOS circuits experience increased signal delay with increasing chip temperature, typically about a one percent speed degradation for every three degrees centigrade temperature increase. This is a basic phenomenon, and cannot be changed by any manufacturer.

A chip's temperature is affected by ambient temperature and device power dissipation. More specifically:

$$T_j = T_A + P_D * \theta_{JA}$$

That is, the silicon junction temperature exceeds the ambient temperature by the product of the dissipated power multiplied by the thermal resistance of the package. This thermal resistance is primarily a function of package size, package material, internal package structure and air velocity.

SRAM-based FPGAs have no significant static power consumption. Practically all internal power dissipation is due to the dynamic charging and discharging of capacitive nodes. This makes it impossible to generalize the device power consumption of Xilinx FPGAs; it can vary by orders of magnitude, depending on the application. Years ago, the power consumption was always relatively low because FPGAs were limited to less than 5,000 gate density, were often not used fully and employed clocks of 20 to 30 MHz. Today, capacity has increased beyond 20,000 gates, better software allows

utilization of up to 100 percent, and clock rates can go well beyond 50 MHz. As a result, power dissipation can be several watts for the largest FPGA devices running at full speed.

This has rendered the traditional 70°C specification unsatisfactory for most demanding applications.

Xilinx has responded to this problem. We are now testing commercial devices at 85°C and industrial devices at 100°C. The new edition of the *1994 Data Book* (3rd edition) provides derating factors for higher junction temperatures (0.35 percent per °C for XC4000 devices, 0.30 percent per °C for XC3000 and XC2000 devices). The thermal resistance for the various device/package combinations, with derating values for airflow, are listed in this new edition as well.

The change to the higher test temperatures was implemented in April. All devices with date codes 9512 or later are tested in this new manner.

SRAM-based or antifuse-based FPGA performance parameters cannot be guaranteed at a specified ambient temperature, independent of power consumption and package type. Depending on the design, the clock rate and the package, the device junction temperature might vary by more than 50°C.

It is our goal to provide clearly-defined device parameters that are meaningful for the user. ♦