

# HDL Synthesis Design Guide for FPGAs

To help designers who are new to HDL-based design with Xilinx FPGAs, Xilinx has created the *HDL Synthesis Design Guide for FPGAs*. This 250-page guide provides general design methodologies for targeting FPGAs from synthesis.

Hardware Description Languages (HDLs) are used to describe the behavior and structure of system and circuit designs. The HDL source code is then synthesized to the target device (e.g., an FPGA). In general, synthesis can produce results that are equal to or exceed those of a well-designed schematic. However, synthesis results depend on the quality of the synthesis tool and the style in which the HDL code is written. Often, it is not sufficient that the HDL code is just “functionally correct”; the code must be written in a manner that directs the synthesis tool to generate an efficient hardware implementation and that matches the idiosyncrasies of the particular synthesis tool being used.

For designs that push the limits of FPGA speed and density, synthesis alone is not good enough—designer intervention is necessary. Synthesis tools are not a substitute for good digital design techniques and knowledge of an FPGA’s architecture.

Most documentation available today describes how to use synthesis tools effectively to target ASICs. However, not all of the methods used for ASICs apply to programmable logic design. ASICs have more gates and routing resources than FPGAs. Poorly written code or the use of a synthesis tool not designed for FPGAs can result in an inefficient design. The Xilinx *HDL Synthesis Design Guide for FPGAs* addresses the use of HDLs and synthesis tools for FPGA design.

Although the guide uses the Synopsys FPGA Compiler and the XC4000 device to illustrate the design methodologies, the

concepts also apply to other synthesis tools and other Xilinx FPGAs. Synopsys and non-Synopsys users alike will find this document extremely useful. All design examples are available in Verilog and VHDL. Xilinx endorses both (though some find VHDL more difficult to learn than Verilog).

To get the most from this guide, Xilinx recommends that you be conversant with VHDL (or Verilog), the synthesis tool and the Xilinx Development tools.

## Table of Contents

*This guide covers the following topics.*

- Chapter 1, “Getting Started,” provides a general overview of designing Field Programmable Gate Arrays (FPGAs) with HDLs. It includes installation requirements and instructions.
- Chapter 2, “HDL Coding Hints,” discusses design hints and examples to help you develop an efficient coding style.
- Chapter 3, “HDL Coding for FPGAs,” provides design examples to help you incorporate FPGA system features into your HDL designs.
- Chapter 4, “Floorplanning Your Design,” describes basic operations of the XACT-Floorplanner™ and provides HDL design examples that illustrate which HDL constructs benefit from floorplanning.
- Chapter 5, “Building Design Hierarchy,” describes how to partition your designs to improve synthesis results and reduce routing congestion.

*“For designs that push the limits of FPGA speed and density, synthesis alone is not good enough.”*

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# HDL Synthesis Design Guide

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- Chapter 6, “Understanding High-Density Design Flow,” discusses the design flow for high-density HDL designs.
- Appendix A, “Accelerate FPGA Macros with One-Hot Approaches,” reprints an article describing one-hot encoding in detail.
- Appendix B, “Top Design Scripts,” includes the three script files used to compile the Top design described in the “Building Design Hierarchy” chapter of the manual.
- Appendix C, “Tactical Software and Design Examples,” lists the tactical software and design examples that are described in this manual.

## How Do I Get a Copy?

The manual and the design examples are available at the Xilinx Internet FTP site ([ftp.xilinx.com](ftp://ftp.xilinx.com)), the World Wide Web site (<http://www.xilinx.com>), and the Xilinx Technical Bulletin Board (XTBB); they also will be included on the XACTstep

version 6 CD-ROM when it is released.

To read the online version, you will need a copy of the Adobe Acrobat™ reader. You can obtain instructions and a free copy of the software from the Xilinx WEB site, XTBB, the Xilinx Programmable Logic Breakthrough '95 CD-ROM, or the appLINX July '95 CD-ROM.

The design guide refers to three utility programs, 27 VHDL design examples and 25 Verilog design examples. Two utilities, AddTNM and MakeTNM were created using Perl. To run these utilities, you will need Perl 4.0 or 5.0 (*see right*).

The instructions on how to retrieve the manual and the design examples from the Xilinx FTP site, World Wide Web site and Xilinx Bulletin Board are described below. A description of the design examples' files and instructions on how to extract the files are in the “Extracting the Files” section of “Getting Started” in the design guide.

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## Xilinx Internet FTP

The manual and design examples are available on the Xilinx FTP site. Descriptions and sizes of the files are shown in the following table.

Files	Description	Compressed File	File/Direct-ory Size
hdl_dg.pdf	HDL Synthesis Design Guide for FPGAs in Adobe Acrobat format	—	1.9 MB
XSI_files	<ul style="list-style-type: none"><li>• Tactical code</li><li>• XNF files for RPMs</li><li>• Default Synopsys setup file</li></ul>	83 K	344 K
XSI_vhdl	VHDL Examples with SIM, SYN and MRA files in Work directory	5.1 MB	13 MB
XSI_vhdl_no_work	VHDL Examples without SIM, SYN and MRA files in Work directory.	3.3 MB	10.2 MB
XSI_verilog	Verilog Examples	3 MB	9.2 MB

*Procedures to retrieve the manual from the Xilinx FTP site:*

1. Go to the directory on your local machine where you want to download the files:  
`cd directory`
2. Invoke the FTP utility — Unix users, type: **ftp**  
PC users: contact your system administrator for assistance.
3. Connect to the Xilinx Internet FTP machine, [ftp.xilinx.com](ftp://ftp.xilinx.com):  
`ftp> open ftp.xilinx.com`

4. Log onto the guest account. It gives you download privileges.

Name (machine:user-name):**ftp**  
Password: **your\_email\_address**

5. Go to the pub/XSI\_HDL directory.  
`ftp> cd pub/XSI_HDL`
6. Retrieve the manual hdl\_dg.pdf and the appropriate design files as follows. Both VHDL and Verilog users should retrieve XSI\_files.tar.Z. VHDL users can retrieve the smaller design file XSI\_vhdl\_no\_work.tar.Z or the file with the WORK directory, XSI\_vhdl.tar.Z. Verilog users should retrieve the file XSI\_verilog.  
`ftp> get hdl_dg.pdf`  
`ftp> get XSI_file.tar.Z`  
`ftp> get design_files.tar.Z`
7. Extract the example files as described in the “Extracting the Files” section of this article.

## World Wide Web

A copy of the manual and design examples can be obtained from the Xilinx World Wide Web site. Access the Xilinx home page under "Product Information -> Application Notes -> HDL Design Guide."

You can download the Adobe Acrobat reader for Windows, Mac and SPARC from a link to Adobe's home page in the Application Notes section. The design examples are also available on the Web.

### Xilinx Technical Bulletin Board

The manual and design examples are available on the Xilinx Bulletin Board (XTBB). XTBB is a 24-hour electronic bulletin board available to all registered XACTstep customers. Refer to the 1994 version of *The Programmable Logic Data* book for a complete description of XTBB, including how to locate and download files.

A description and size of the files are shown in the table following. Note: The manual hdl\_dg.zip is very large and may take a long time to download.

Files	Description	Compressed File	Directory Size
hdl_dg.zip	HDL Synthesis Design Guide for FPGAs in Adobe Acrobat format Zipped (using PKZIP)	1.6 MB	
tactical.uu	<ul style="list-style-type: none"><li>• Tactical code</li><li>• XNF file for RPMs</li><li>• Default Synopsys setup file</li></ul>	115 K	344 K
vhdl_ex.uu	Source files and major files for VHDL Examples	2.6 MB	5.1 MB
ver_ex.uu	Source files and major files for Verilog Examples	2.5 MB	4.7 MB

To retrieve the files from the XTBB:

1. Go to the directory on your local machine where you want to download the files:  
`cd directory`
2. Access the XTBB as described in of *The Programmable Logic Data* book (Chapter 6).
3. Locate the files in the application area of the XTBB. The directory names are listed in the table above.
4. Retrieve the zip and encoded design files.
5. Unzip the file hdl\_dg.zip file:  
`unzip hdl_dg.zip`
6. Follow the instructions below to decode and uncompress the files.

### Extracting the Compressed and Encoded files

After you have retrieved the manual and design examples, perform the following to extract the compressed and encoded files:

1. If the file is uu encoded (i.e. has an .uu extension) decode the file as follows:  
`uudecode file.uu`
2. Uncompress the files:  
`uncompress file.tar.z`
3. Extract the files:  
`tar xvf file.tar`

### How to Get Perl

Get information about Perl (Perl FAQ) from the Unix FTP site:

- North America:  
`ftp://fpt.cis.ufl.edu/pub/perl/doc/FAQ`  
`ftp://fwp.khoros.unm.edu/pub/perl/faq.gz`
- Europe:  
`ftp://ftp.cs.ruu.nl/upb.NEWS.ANSWERS/perl-faq/`  
`ftp://ftp.funet.fi/pub/languages/perl/doc/faq`
- Access Perl All-Sorts information on the World Wide Web:  
`http://www.khoros.unm.edu/staff/neilb/perl/`  
`http://www.metronet.com/1h/perlinfo`  
`http://www.cis.ufl.edu/perl`

### Software Requirements

To synthesize, floorplan and implement the design examples, you need the following versions of software installed on your system. (Either XACTstep or XACTstep Foundry is required, but not both.)

SOFTWARE	VERSION
Xilinx Synopsys Interface (XSI)	3.2.0 or later
XACTstep	5.1.0 or later
XACTstep Foundry*	7.0 or later
Synopsys FPGA Compiler	3.2 or later
Xilinx Floorplanner	Contact Xilinx sales rep.
XC4025 die files	Contact Xilinx sales rep.

\* XACTstep Foundry v7 does not support the Xilinx Floorplanner.