



XC5200 Family Now In Volume

All XC5200 family devices and the supporting XACTstep™ design software are now in volume production. With five devices — ranging from 2,000 to 18,000 usable gates — offered in 15 different packages, there are now more than 100 different device/package/speed combinations available to meet the most exacting design requirements. Complete footprint compatibility between all devices in a common package allows the migration to higher or lower density devices without modifying the printed circuit board. All XC5200 devices are also footprint-compatible with the XC4000 and XC8100 families.

By optimizing the XC5200 family for a 0.6 micron, three-layer-metal SRAM process

and by delivering architectural innovations, Xilinx has dramatically reduced die area and size. Xilinx now provides the industry's highest value family of FPGAs.

DEVICE	USABLE GATES
XC5202	2,200–2,700
XC5204	3,900–4,800
XC5206	6,000–7,500
XC5210	10,000–12,000
XC5215	14,000–18,000

With powerful new features such as the VersaRing™ I/O interface, dedicated JTAG logic for increased testability, and fast carry logic for high speed arithmetic functions, the XC5200 is the optimal solution

XC3100A-09: The World's Fastest FPGA

The popular XC3100A family has attained a 50 percent boost in performance from changes in manufacturing process and layout. The new XC3100A-09 and XC3100A-1 devices were designed with an optimized 0.6μ, triple-layer-metal process technology.

The XC3100A-09 has 40 percent shorter block delays, 50 percent faster chip-to-chip speed and decoding functions, as well as 100 percent faster interconnect speed compared with the XC3100A-2 device (see Table 1).

Fully PCI compliant, the XC3100A is ideal for high-speed serial-to-parallel conversions, fast ATM switches, video control functions and 3D graphics/imaging. Designs which require high-speed clock distribution can also benefit.

The Software Help area of the Xilinx bulletin board (408-559-9327) contains advance speed files for use with XACT™ design software. The combination of XC3100A silicon and XACTstep-Performance™, Xilinx's timing-driven placement software, provide a high level of productivity for high-performance designs.

The new XC3100A devices are fully backward compatible with earlier XC3100A devices (that is, they may be dropped in with the same bitstream). See Table 2 for device availability. ♦

Table 1

-09 vs. -02 Performance Comparisons

	XC3100A-09	XC3100A-2
Combinatorial Delay	1.4 ns	2.2 ns
Clock to Out (pin-to-pin)	6 ns	7.8 ns
Setup (pin-to-pin)	3.5 ns	6.5 ns
Interconnect (normalized)	4.4 ns	10 ns
State Machine	112 MHz	68 MHz
Data Path	356 MHz	233 MHz
Max Chip-to-Chip	110 MHz	70 MHz

Table 2

XC3100A-09 and XC3100A-1 Availability

Device	Sampling	Production
XC3120A	December	2Q96
XC3130A	December	2Q96
XC3142A	Now	2Q96
XC3164A	December	2Q96
XC3190A	Now	1Q96
XC3195A	Now	1Q96

Production

for high density designs not requiring the high performance and on-chip RAM of the XC4000 series.

The XC5200 family is completely integrated into the powerful XACTstep design tools. All in-warranty users will receive XC5200 software as part of the XACTstep version 6 (Windows) and XACTstep 5.2 (DOS) production release.

VersaRing Increases Pin Locking Flexibility

As an increasing number of users design with the XC5200 family, one thing is becoming clear — the VersaRing I/O interface is delivering on its promise of allowing users to make last minute logic changes **without** having the pinouts change, forcing a new PCB layout. Designers have long wanted an FPGA solution that allowed the flexibility of pre-assigning, or “locking,” I/O locations before the logic design was completed. This facilitates an early release of the PCB design, thereby accelerating total system design time.

The VersaRing feature of the XC5200 architecture provides an incremental layer of routing resources along the edge of the device (*see diagram*). This gives the routing software dramatically improved freedom to pre-assign pins, since connections between IOBs and CLBs can now be made by routing along the edge of the device rather than through the core logic. It's important to note, however, that while the VersaRing provides a dramatic improvement in pin-locking capability, it cannot provide the same pin-locking guarantee that can be made by Xilinx EPLDs, with their 100-percent connectivity of the Universal Interconnect Matrix (UIM™).

It's a fact that designs change during all stages of the design/manufacturing cycle. The XC5200 VersaRing enhances the benefits of reprogrammability by allowing

more of these changes to occur without forcing a PCB modification. Combined with the lowest cost per gate of any FPGA solution and system performance extending to 50 MHz, the XC5200 delivers a very robust solution for designs up to 18,000 gates.

Please contact your local Xilinx sales representative for the latest information on XC5200 family availability and pricing. ♦

