

Logic Synthesis for FPGAs - An Update

As FPGA designs get larger and more complex and time-to-market pressures continue to increase, more designers are turning to VHDL or Verilog-HDL based design flows. Xilinx remains firmly committed to supporting these users.

Synthesis for Xilinx FPGAs has taken major steps forward during 1995. We are now seeing cases where synthesis tools can produce results that are smaller and faster than a schematic design for modest size functions (such as a digital filter).

At the beginning of the year, only a few vendors were performing full mapping to the basic logic elements of Xilinx devices. This "what you synthesize is what you get" (WYSIWYG) methodology is preferred by ASIC designers familiar with VHDL/Verilog-HDL design. It provides a very high degree of correlation between the synthesis results and the final device, while also assuring that cell delay and interconnect delay estimates made during the synthesis process are consistent with the actual delays calculated by the FPGA implementation software later in the design process.

This design methodology was first supported by the **Synopsys** FPGA Compiler; it began supporting full mapping to XC4000 CLB and IOB structures in February 1993. Synopsys extended their FPGA support to include generic look-up table (LUT) mapping in the FPGA Compiler v3.3a release in March 1995. Xilinx took advantage of this feature to implement full mapping to the function generators (LUTs) of the XC3000 and XC5200 families with libraries released in the Xilinx-Synopsys Interface (DS-401) version 3.3 in June 1995. Other vendors, including **Data I/O**, **Viewlogic**, **Exemplar Logic**, **IST**, and **Synplicity**, have followed Synopsys' lead by implementing WYSIWYG design flows

for the XC3000, XC4000 and XC5200 families during 1995.

The **XC5200** family is of particular interest because, from a synthesis standpoint, its architecture is simpler and more regular than the XC3000 and XC4000. If a synthesis tool can map to 4-input look up tables (LUTs) and registers, and map arithmetic functions to X-BLOX™ elements (in order to use the fast carry logic), that synthesis compiler will be using all of the XC5200 logic resources. With the attractive pricing of the XC5200 family, these devices can be used as a production solution for 5,000-15,000 gates.

The new **XC8100** FPGA family also supports a WYSIWYG synthesis. Its fully-

What You
SYNTHESIZE
Is What You Get

configurable logic cell can be supported by any conventional, cell-based synthesis tool, eliminating the need for special synthesis algorithms. These tools, rather than targeting the look-up table elements found in the SRAM-based Xilinx devices, target a set of logic functions in a library. For each of the library's logic cells, there will be a particular configuration of one or more Configurable Logic Cells (CLCs) in the XC8100 architecture that corresponds to that function. The XC8100 is supported by synthesis libraries for

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Executing from the



C E T P

CD-ROM

To preserve precious space on your PC's hard disk, XACTstep™ version 6 and Viewlogic PRO Series programs can be executed directly from the CD-ROM without being installed on the system's hard drive. Users must configure the system properly and set up a program group in Windows® to access the software located on the CD-ROM correctly. When executing from CD-ROM, the graphical tools will seem to take longer. Non-graphical programs, such as PPR, will be delayed only two to five minutes depending on the program loading time. ♦

XACTstep only

This procedure for running XACTstep from the CD-ROM assumes that C:\ is a local drive and that D:\ is the CD-ROM

drive containing the XACTstep CD-ROM.:

- 1) If running Windows, exit.
- 2) Create a local XACTstep directory.

Example: C:\CDXACT

- 3) Make the following changes to the AUTOEXEC.BAT file:

SET XACT=D:\XACT;

SET PATH=D:\XACT;<other_paths>

NOTE: The only path added to the PATH environment variable is the CD-ROM executable path XACT. The local path created in the previous steps does not need to be added.

SET XACTUSER=C:\CDXACT

NOTE: To ensure that the XACTstep software has a directory that can be written to, the XACTUSER environment variable should be set to a local directory.

- 4) Reboot your machine or execute your AUTOEXEC.BAT file so that the new changes take effect.
- 5) Start Windows.

Now that the system has been properly configured to run the software from the CD-ROM, all that remains is to create a

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Synopsys, Viewlogic, Mentor Graphics, and Exemplar Logic tools.

Table 1 shows the current state of synthesis support from major EDA vendors for the Xilinx FPGA products. Support is indicated as either "gates" or "mapped,"

where mapped supports indicates that the synthesis compiler maps to the fundamental logic cell elements of that architecture.

VHDL or Verilog-HDL designers now have a number of choices in FPGA synthesis, both in terms of tools and device architectures. Many synthesis vendors are supporting full ASIC design methodologies for Xilinx. With the fast, PCI-compliant XC3100A, the cost-effective XC5200, the high density XC4000 with on-chip RAM, and the highly-configurable and non-volatile XC8100 families, Xilinx offers cost-effective, high-performance FPGA solutions for HDL-based design. ♦

Table 1 - Xilinx FPGA Synthesis Support by Third-Party Vendors

	XC3000	XC4000	XC5200	XC8100
Data I/O	Mapped	Mapped	Mapped	
Exemplar Logic	Gates	Mapped	Mapped	Mapped
IST	Mapped	Mapped	Mapped	
Mentor Graphics	Gates	Gates	Gates	Mapped
Synopsys	Mapped	Mapped	Mapped	Mapped
Synplicity	Mapped	Mapped	Mapped	
Viewlogic	Mapped	Mapped	Gates	Mapped