

Minimizing Power Consumption in FPGA Designs

In general, the CMOS technology used to produce FPGAs is a low-power technology. Virtually all power consumption results from the dynamic charging and discharging of internal capacitive nodes and capacitive loads on the device outputs.

Here are some techniques that can be used to minimize power consumption in an FPGA design:

- *Chip outputs dissipate a lot of power.* Use as few as possible, and have them switch as infrequently as possible. Although there is no need to three-state outputs unnecessarily, don't allow an output to change continuously if the external circuitry is ignoring the data.
- Similarly, *don't allow internal FPGA nodes to toggle unnecessarily.* Clock enable functions on flip-flops often can be used to "turn off" inactive portions of a synchronous circuit.
- *Use APR or PPR (or even XDE) to maximize the performance of the design,* even if the resulting performance is far in excess of requirements. Power dissipation is proportional to capacitance, and routing capacitance is the main cause of low performance. Circuits that are able to run faster can do so because of lower routing capacitance. Consequently, they dissipate less power at any given clock frequency.

- *For XC3000A/XC3100A designs, use ACLK for global clocking,* and floorplan to minimize the number of vertical clock segments used. This minimizes the power associated with clock distribution.

For very power-sensitive applications, power consumption can be dramatically reduced by using the 3.3 V Zero+ XC2000L and XC3000L FPGA families. These devices were designed to provide very low quiescent current consumption, and consume less than half the dynamic power of their 5 V counterparts. Also, remember that the XC2000 and XC3000 FPGAs feature a power-down mode, wherein the FPGA's configuration is preserved, but all other circuitry is powered down. ♦

User-Defined Schmitt Triggers

All inputs to Xilinx FPGAs have a hysteresis of 100 to 200 mV. It helps avoid noise propagation from slowly rising or falling input signals. Users requiring more hysteresis can design their own **Schmitt trigger** circuits easily with only two resistors. However, it uses one additional output pin, driven (non-inverted) from the input pin, as in the diagram.

A 10 k Ω serial input resistor combined with a 100 k Ω feedback resistor gives 500 mV

of hysteresis. (Hysteresis is the difference between the effective input threshold voltages on the Low-to-High transition and the High-to-Low transition. That difference is equal to V_{cc} times the resistor ratio.)

A 1 k Ω /10 k Ω combination gives the same hysteresis, but reduces the delay caused by the pin-to-ground capacitance from 100 ns to 10 ns. On the other hand, it requires more input current.

For TTL-threshold inputs, the hysteresis should be kept below 1 V; for CMOS inputs, it can be up to 2 V. ♦

