

Designing with XC9500 CPLDs — *First In-System*

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XC9500 CPLDs are the first in-system programmable (ISP) devices based on 5 V flash technology. The XC9500 architectural features enhance ISP by permitting design changes without altering pin assignments.



The powerful XC9500 architecture supports a wide variety of design methodologies. Each function block and macrocell is identical. This assists the designer when using HDLs, synthesis and/or schematic capture tools by

allowing the software to fit and route the design quickly and efficiently.

The XC9500 family allows easy migration across multiple density options in a given package footprint. Designs initially targeted at a small part can be migrated into a larger part. This capability helps designs maintain their pin assignments if additional logic capacity is needed in a

socket already committed to a printed circuit board.

The design software also incorporates a number of strategies permitting future edits without altering pinouts. The *XC9500 Application Guide* outlines many of these architectural features and software strategies.

Macrocells

Understanding the macrocell and interconnect capability is key to designing with XC9500 CPLDs. Detailed knowledge is not required, but general facts are helpful.

The XC9500 macrocell performs most logic functions at the bit level in a single macrocell. Counters, shifters, multiplexers and decoders require a single macrocell to perform one bit of corresponding function. Adding and subtracting functions generally require two macrocells per bit. Parity can be calculated over four bits in one macrocell. The design software automatically implements appropriate mapping and optimization.

Product terms are automatically distributed among macrocells. Any macrocell easily receives up to 15 product terms with additional product terms delivered from local neighboring macrocells. There are few logic functions needing more than 25 product terms. However, up to 90 product terms can be assigned to a

Low Voltage Product Line Expands

Xilinx Announces First 3 V PCI and CardBus Compliant Devices

Xilinx has significantly expanded its product offerings for 3.3 V systems with the introduction of the XC3100L and XC4000L FPGA families. These new product offerings include more than 30 combinations of device, speed, and package, tripling the size of the Xilinx 3 V FPGA product line. Engineering samples are available now, with full production scheduled for the second quarter of this year.

XC3100L FPGAs, the highest-performance 3 V FPGAs available today, are

architecturally and functionally identical to the XC3100A family. Family members include the XC3142L and XC3190L. The -2 speed grade of the XC3100L is the first 3 V PCI and CardBus compliant programmable logic device. The XC3100L family is targeted towards speed-sensitive, low-voltage applications such as PC-Card modems and video peripherals.

The XC4000L family offers the broadest density range of any 3 V FPGA product family, ranging from 5,000 gates to an industry-leading 13,000 gates. Family members include the XC4005L, XC4010L and XC4013L devices. The XC4000L FPGAs have all the

Programmable Devices Based on 5-V Flash Technology

macrocell within a particular function block. The XACTstep™ design software handles the details of product term assignment.

In-System Programming

XC9500 devices are programmed in-system via an IEEE 1149.1 standard 4-pin JTAG protocol. Multiple XC9500 CPLDs as well as other JTAG-compatible devices (such as XC4000E and XC5200 FPGAs) can be linked together in the same JTAG chain. In-system programming offers quick and efficient design iterations and eliminates package handling. Once designs are compiled, their configuration patterns are downloaded automatically using the EZTAG download software. Users need only provide the JTAG chain ordering sequence to the software that targets the specific CPLD being programmed.

All XC9500 CPLDs are in-system programmable for at least 10,000 program/erase cycles. In addition, the JTAG downloading and programming circuitry is the most comprehensive and advanced available today. Each XC9500 device supports EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, and HIGHZ instructions. All in-system programming, erase and verify instructions fully comply with extensions of the IEEE 1149.1 boundary-scan.

The XC9500 family supports **mixed voltage systems** combining both 3.3 V and 5 V components. XC9500 CPLDs can implement both logic and level shifting functions in a single programmable device. This eliminates the need for discrete level translation buffers.

The XC9500 family also includes **User Programmable Ground** for internal signal management. User Programmable Ground allows the device I/O pins to be configured as additional ground pins. Tying programmable ground pins to the external ground connection reduces system noise.

Superior Performance

These additional features enhance the overall electrical capabilities of this new family, relieving designers of many critical signal management responsibilities.

In summary, the XC9500 family offers a superior high-performance, general-purpose logic integration solution. The powerful CPLD architecture expands in-system programming capabilities with the industry's most comprehensive JTAG support. The architecture also permits design changes without altering pin assignments. ♦

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architectural features of the XC4000E family, including Select-RAM™ memory.

These low-voltage FPGA products are bitstream compatible with their 5 V counterparts; designers can use the current XACTstep v6 and XACT 5.2 development systems to design with these new devices.

While in the past 3 V designs have been limited mostly to laptop computer and cellular telephone applications, there now is a significant increase in design activity in the mainstream telecommunications, data communications and instrumentation markets. The expansion of the 3 V FPGA product line

addresses this growing market. Please contact your local Xilinx representative for the latest availability information. ♦

DEVICE	SPEED GRADES	ENG. SAMPLES	LIMITED PRODUCTION	VOLUME PRODUCTION	PACKAGE AVAILABILITY
XC3142L	-2/-3	Now	March	2Q 96	PC84, VQ100, TQ144
XC3190L	-2/-3	Now	March	2Q 96	PC84, TQ144, TQ176
XC4005L	-5/-6	Now	March	2Q 96	PC84, PQ208
XC4010L	-5/-6	Now	March	2Q 96	PC84, TQ176, PQ208
XC4013L	-5/-6	Now	March	2Q 96	PQ208, PQ240, BG225