

XABEL-CPLD Software Available NOW!

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XABEL-CPLD software is available **now** for immediate ordering and delivery!

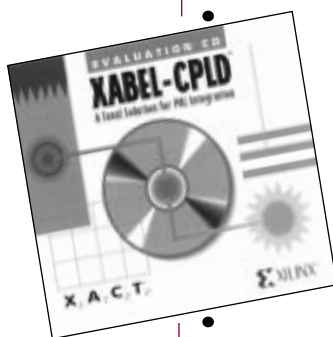
XABEL-CPLD is the new Xilinx development system designed for PAL and CPLD users. With this completely self-contained system, PC-based customers can quickly and easily integrate their logic into Xilinx CPLDs using the industry-standard ABEL hardware description language.

This new design software combines the well-known, windows-based Data I/O ABEL6 front-end with the new Xilinx XACTstep™ v6 core software; the result is an extremely easy-to-use, industry-standard user interface capable of targeting Xilinx CPLDs.

Designed for the PC and priced at only \$495, XABEL-CPLD is the perfect software solution for users familiar with ABEL, PALASM, CUPL and MACHXL who design with PALs and CPLDs.

Features

- Familiar Data I/O ABEL, Windows-based environment for design entry, simulation and fitting.
- Industry-standard ABEL-HDL supports state machines, high level logic descriptions, truth tables and equation entry.
- Hierarchical design entry and JEDEC file conversion for integration of existing PALs into Xilinx CPLDs.
- Functional simulation with graphical waveform viewer and static timing reports
- Advanced XACTstep v6 fitter with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing-driven fitting.
- On-line tutorial and on-line help reduces learning curve. ♦



XABEL-CPLD Evaluation CD-ROM Available

The XABEL-CPLD software offers a truly accurate method for evaluating the performance, power, board real estate and cost savings gained by integrating multiple PALs into a single Xilinx XC7000 CPLD device. Simply enter the design and the evaluation software does the rest.

To obtain an evaluation CD, contact your local Xilinx sales representative or distributor. You also can request a CD from the Xilinx WebLINX web page (www.xilinx.com). ♦

XC8100 Family Adds Schematic Support

Production version 1.1 of XACTstep Series 8000 is now available. This release adds support for the PC platform and the use of Viewlogic's ProCapture and Mentor's Design Architect schematic editors for XC8100 FPGA design.

As a result, schematic-based designs can now access the advanced features of the XC8100 FPGA family:

- Extremely high design security
- Near 100% utilization regardless of logic type

X_S A_T C_E T_P

- Abundant routing resources
- Internal 3-state buffers
- Pin-locking tolerance
- Footprint compatibility with XC4000 and XC5200 FPGAs

New XC7000 Core Software in XACTstep v6

The Xilinx XC7000 core software delivered in XACTstep v6 contains new features and enhancements of existing features that address user productivity and design performance for Xilinx CPLD designs.

Productivity Improvements

Automatic Device Selection - The software automatically implements the design in the smallest device possible using device type, package type and speed constraints entered by the designer

XACT-Performance™ - Timing-driven optimization collapses logic to meet user-specified critical timing requirements.

Static Timing Analyzer - Provides a complete pin-to-pin timing report of the design, including detailed internal path analysis

Performance Improvements

New Design Optimization Algorithms - New design optimization and partitioning algorithms better utilize the XC7300 architecture *without user intervention*. Designs fit in smaller devices, take about 10% fewer macrocells and run about 10% faster than before.

Multiple-Pass Optimization, Partitioning and Mapping - The software will try a different optimization and partitioning strategy if necessary to achieve a first-time fit, *without user intervention*.

Schematic and VHDL Design Entry

Xilinx provides an open design environment that allows designers to choose from a variety of schematic entry, VHDL synthesizer and simulation tools, such as those from OrCAD, Viewlogic, Men-

tor Graphics, Exemplar and Synopsys. When combined with the appropriate library and interface software, XACTstep v6 provides a complete environment for the processing of Xilinx XC7000 CPLD designs

ABEL-HDL Entry

XABEL owners can continue to embed macros in their schematics or enter complete chip designs for the XC7000 family and use XACTstep v6 to complete the design implementation. This core software is included in the new Xilinx XABEL-CPLD package, a complete ABEL-HDL based tool designed specifically for PAL users who want to use Xilinx XC7000 CPLDs.

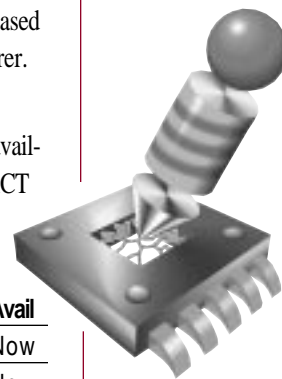
Embedded Third Party Compilers

Xilinx licenses its fitter technology to third-party development tool vendors, giving you the flexibility and versatility of industry-standard design software environments with the speed, density and routability of Xilinx CPLDs. The Xilinx CPLD fitter is fully integrated into the Data-I/O Synario, Logical Devices CUPL and IsDATA LOGiC environments. For price and availability of the XACTstep v6 based fitter, contact the development tool manufacturer.

Product Availability and Pricing

The XC7000 XACTstep v6 core software is available on the PC for immediate delivery. The XACT 5.2 core software is available for workstation platforms. ♦

Part Number	Version	Platform	Pricing	Avail
DS-550-PC1-C	6.0	PC	\$89.95	Now
DS-550-SN2-C	5.2	Sun	\$995	Now
DS-550-HP7-C	5.2	HP	\$995	Now



The table summarizes the supported CAE interfaces. Many other third-party CAE vendors are working on XC8100 solutions that will be released in the first half of 1996.

Now Runs on PC — Version 1.1 adds PC support (DS-8000-STD-PC1-C or DS-8000-EXT-PC1-C). It

runs under Windows 3.1, Windows 95 and Windows NT. The CAE interfaces available on the PC include Viewlogic and Exemplar. Workstation versions are available for SunOS, Solaris, HPPA, and RS6000 platforms. ♦

CAE Tools Supporting XC8100 FPGA Design

Schematic	Synthesis	Simulation	Timing Analysis
Viewlogic ProCapture Mentor Design Architect	Synopsys Design Compiler Synopsys FPGA Compiler Viewlogic ViewSynthesis Mentor Autologic I, II Exemplar	Synopsys VSS Cadence Verilog Viewlogic ViewSim Mentor QuickSim Mentor QuickVHDL Model Tech VITAL VHDL	Synopsys Motive Mentor QuickPath Cadence Veritime