

In-System Programming and Flash Technology for CPLDs

By NICK KUCHARAWSKI ♦ Vice President, EPLD Division

The latest wave of complex programmable logic devices (CPLDs) has been targeted at an emerging applications area: **In-System Programmability (ISP)**. In-system programmable CPLDs allow the user to mount an unprogrammed device on the PC board, then program the device as part of the manufacturing flow. This greatly eases the handling problems associated with fine pitch packages such as the popular plastic quad flat pack (PQFP). But this is far from the only advantage of ISP CPLDs.

Designers can use ISP devices to meet a wide range of needs — from facilitating an integrated design, program, and test environment that allows easy prototyping and system debug, all the way to providing the ability to upgrade a design in the field through CPLD reconfiguration. Of course, manufacturing support must be provided for integrated device programming and board-level test. We refer to supporting this range of user requirements as “supporting the total product life cycle” with in-system programmable CPLDs. As more and more users begin to take full advantage of ISP capabilities during all stages of a product’s life, the use of ISP CPLDs will continue to increase. In turn, CPLD manufacturers will need to offer device architectures and development tools that support this full range of user needs in order to remain competitive.

Introducing the FastFLASH™ XC9500™ Family

The XC9500 family is the first CPLD family specifically developed to meet all the typical user requirements for in-system programmability. Xilinx used those requirements to drive the XC9500 development process, including basic device architecture decisions and process technology choices. Let’s take a closer look at some of these requirements, and their impact on the CPLD.

As mentioned in Brad Fawcett’s editorial (*see page 2*), the flexibility of ISP is enhanced by the ability to fix the chip pinouts (“lock the pins”) while continuing to implement design changes. Obviously, the reconfiguration of CPLDs already in the field requires maintaining fixed pinouts to be successful. The approach we have taken to solving this challenge is quite complex and involves several architectural innovations as well as improvements to the optimization and fitter software. The result is the industry’s best pin-locking CPLD.

Many users require complete support of industry-standard IEEE 1149.1 JTAG boundary scan test capabilities. By including the in-system programming control within the JTAG controller, both board test and device programming are accomplished with a single interface, and in an integrated environment. This greatly simplifies the manufacturing engineering requirements. The XC9500 is the only CPLD to include support for JTAG instructions such as INTEST and USERCODE. The INTEST instruction is used to test internal logic after device programming on the PC board,

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Xilinx Enters Into Joint Venture for Foundry Capacity

In a joint venture with United Microelectronics Corporation (UMC) and others, Xilinx has invested a 25% equity stake in a semiconductor manufacturing facility in Hsin Chu City, Taiwan.

Xilinx is one of more than 100 semiconductor companies that use independent silicon "foundries" rather than their own wafer fabrication facilities. Being "fabless" allows the company to focus on what Xilinx does best — the design and marketing of programmable logic devices. Xilinx transcends the scope of traditional customer-supplier relationships by employing its own process experts, who work closely with our foundry partners in the development and implementation of process technology improvements.

The Taiwan facility will ensure a steady and reliable supply of product as the demand for programmable logic devices continues to grow. Starting its two-year ramp up cycle in early 1996, the factory

will produce eight-inch wafers using submicron CMOS processes. In the meantime, UMC will provide Xilinx with interim capacity at its other facilities in Taiwan.

Xilinx will maintain its existing foundry partnerships with Seiko Epson, Yamaha, Taiwan Semiconductor Manufacturing Company (TSMC) and IC Works. While the UMC investment marks the first time Xilinx has taken an equity position in a foundry, it is not the first Xilinx investment involving its foundry partners. For example, in early 1994, Xilinx helped fund Seiko Epson's expansion of an IC facility in Sakata, Japan.

"This new venture ensures foundry capacity of leading-edge process technologies to meet the rising demand for FPGAs," noted Xilinx CEO Bernie Vonderschmitt. "This agreement, combined with our other foundry partnerships, favorably positions the company to meet customer demand to the end of the decade." ♦

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while the USERCODE function allows the user to "program in" information such as version numbers, assembly locations, or dates as part of the manufacturing process.

Flash Process Technology

An easy-to-use, integrated design and programming environment allows designers to implement multiple design iterations per day. This can translate into a need to support hundreds, and perhaps thousands, of program-erase cycles. Flash process technology provides this capability, with margin to spare. The Xilinx proprietary FastFLASH Technology is the industry's first 5-volt flash technology developed specifically for CPLD applications. It is an extension of industry-standard flash memory technology, and offers the proven reliability of 10,000 program-erase cycles — a factor of up to 100 times more than competing ISP CPLDs.

The benefits of flash technology extend beyond program-erase endurance. The flash memory cell provides the basic programmable "switch" in the XC9500 CPLDs. The size of the flash memory cell is about 1/3 that of other non-volatile technologies, allowing the implementation of many more "switches" in the same chip area. These added resources lead to improved routability and pin-locking capability.

In-system programmability is an increasingly important requirement for CPLDs. The needs of ISP CPLD users extend beyond easier handling of PQFP packages to more complete support of "the total product life cycle." The architecture, process technology and development tools of the XC9500 FastFLASH family meet these needs, allowing users to take full advantage of the flexibility of ISP technology. ♦