

**Q Do I require any additional settings for XC3000 or XC5200 designs in Synopsys?**

There is one additional setting that you should include into your .synopsys\_dc.setup file, if you are using the FPGA Compiler to synthesize XC3000 or XC5200 designs. Include the following line in your .synopsys\_dc.setup file:

```
fpga_improved_delay_mapping = 1 ◆
```