

# PLDs, Pins and PCBs (part 2)

By BRADLY FAWCETT ♦ Editor

Part 1 of this article (XCELL 20, page 2) discussed the inevitability of design changes during all stages of an electronic system's lifecycle. Changes can occur as a result of the debugging and testing of the initial design, due to specification changes during the design, or even to add features to a mature product to extend that product's life.



An important benefit of user-programmable logic is tolerance of

change; with PLDs, design changes can be implemented quickly and easily. However, printed circuit board (PCB) designs are not as easy to change, typically requiring new drawings (masks) and the manufacturing of new prototypes, with all the associated expenses and delays. Thus, to garner all the benefits of the flexibility of programmable logic, programmable logic device architectures should isolate the PCB design from logic changes that occur within the PLD device. Device

architectures should do this in two ways — by supporting pin-locking and with footprint compatibility.

**Pin-locking** — that is, for signals entering and leaving a PLD, maintaining the pin locations during design changes internal to the PLD — was discussed at length in part 1. Support for pin-locking is a key feature of the latest generations of Xilinx CPLDs and FPGAs.

Equally important, **footprint compatibility** maximizes PLD design flexibility, and has been incorporated in all Xilinx components since the XC2000 family — the world's first FPGA! Footprint compatibility refers to the availability of PLDs of various gate densities with the same package and with an identical pinout. With a range of footprint-compatible devices available, users may migrate a given PLD design to a higher- or lower-density device without changing the printed circuit board.

## Footprints in the Silicon

There are several scenarios where a common device footprint provides a significant advantage. The most prevalent of these is when a design is being modified to add features without changing the pinout requirements, and, as a result, the design grows to exceed the gate density of the PLD device that was initially selected.

By moving the design to a footprint-compatible device with higher capacity, a re-layout of the printed circuit board is avoided, saving both time and money.

On the other hand, a design can be initially prototyped in a larger device than needed, to allow room for expansion and experimentation. Once the design is fixed, it can be migrated to a smaller, less-expensive device in the same package as a cost reduction. Again, footprint compatibility between the devices avoids changes to the printed circuit board. (There is, however,

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one caveat to consider when migrating a design from a larger to a smaller PLD device. For some smaller devices, the package may have more physical pins than there are input/output pads on the device. Thus, some package pins may be left unconnected. A larger device in the same family may have more I/O pads on the die and, therefore, have connections to all the pins of the given package. Thus, if migration to a smaller part is anticipated, the initial design in the larger device should avoid using those pin locations that are not connected in the smaller device.)

In other words, **footprint compatibility lessens any risks associated with the initial device selection**, which often must be based on a rough estimate of the design's requirements. If the selected device turns out to be too small, the design is migrated to a larger device. If the selected device is too big, the design can be moved to a smaller device. In either case, potentially expensive and time-consuming changes to the PCB are not necessary.

Footprint-compatible devices also provide the user with more inventory flexibility. Devices that are on-hand can be used for prototyping or initial production, and the design can then be migrated to a footprint-compatible device for quantity production. If a sudden demand "upside" should develop, users have the option to move to a larger device in the same family or a similar-sized device from another footprint-compatible family.

### Compatible From the Start

Recognizing these benefits, Xilinx always has maintained footprint compatibility within component product families and subfamilies whenever multiple devices share common packages. For example, the XC3030 and XC3042 devices share a common footprint in the PC84, TQ100, and VQ100 packages. That same

footprint is maintained in the equivalent density members of the XC3000A, XC3100, XC3100A, and XC3000L sub-families. (The only exceptions are the XC3000 series and its derivatives in the PC 84 package, where some of the larger devices need two additional GND and  $V_{CC}$  connections, and in the PQ208 package, where the XC3090 and XC3195 devices do not have compatible footprints.)

Cross-family compatibility began with the XC4000 series of FPGAs and includes the XC5000 series and the XC8100 series — all sharing common footprints in common packages. This provides designers with many options. For example, as reported in *XCELL* 19, VTEL Corp., a manufacturer of video teleconferencing systems and one of the first adopters of the XC5000 family, prototyped their designs in XC4000 series FPGAs while awaiting the availability of XC5000 components and development tools. The resulting designs were easily migrated to lower-cost, footprint-compatible XC5000 devices for production systems. In a similar scenario, a designer could exploit the re-usable nature of the SRAM-based XC4000 or XC5000 FPGAs for debug and prototyping purposes, and then switch to the one-time-programmable XC8100 family for production.

Designers should avoid getting locked into programmable logic solutions that offer little flexibility in pin assignments and device selection. Xilinx CPLDs and FPGAs offer the best pin-locking capabilities in the industry, and the broadest spectrum of footprint-compatible devices. These features allow users to avoid modifications to printed circuit board designs, thereby accelerating time-to-market and accommodating the inevitable design changes that occur throughout a product's total life cycle. ♦

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