

VHDL Made Easy!

Introducing the Xilinx

Foundation Series Software Solutions

22

The software packages in the Xilinx Foundation Series™ are complete, fully-integrated sets of development tools that support a broad range of CPLD and FPGA design requirements. They include combinations of Windows-based design tools, integrating industry-standard hardware description languages (HDLs), synthesis, schematic entry and simulation tools with the Xilinx XACTstep™ implementation tools. Emphasis has been placed on providing an easy-to-learn, HDL-based design environment.

Foundation Series packages are the lowest-cost and most complete design software packages in the programmable logic industry, featuring:

- Packages starting at \$495
- Technology-independent migration paths
- Industry-standard HDL support: VHDL and ABEL-HDL
- Easy-to-achieve quality results with the Xilinx HDL Wizard
- Easy-to-use, push-button software
- Interactive tutorials for all tools including VHDL synthesis
- Tight integration with schematic, simulation, HDLs and XACTstep
- Complete project and flow management

Breaking the Barriers to VHDL Synthesis

Xilinx provides the easiest way to obtain and learn VHDL with low-cost packages that include both a VHDL synthesis tool and a multimedia tutorial for learning VHDL at your own desk and at your own pace.

The multimedia tutorial educates users on:

- The VHDL Language
- How to write VHDL code for synthesis
- How to use VHDL successfully using the Xilinx Foundation Series tools
- How to write VHDL code to obtain the best results when targeting any Xilinx technology

The HDL Wizard, a set of tools that help users quickly learn and implement VHDL and ABEL-HDL designs, includes:

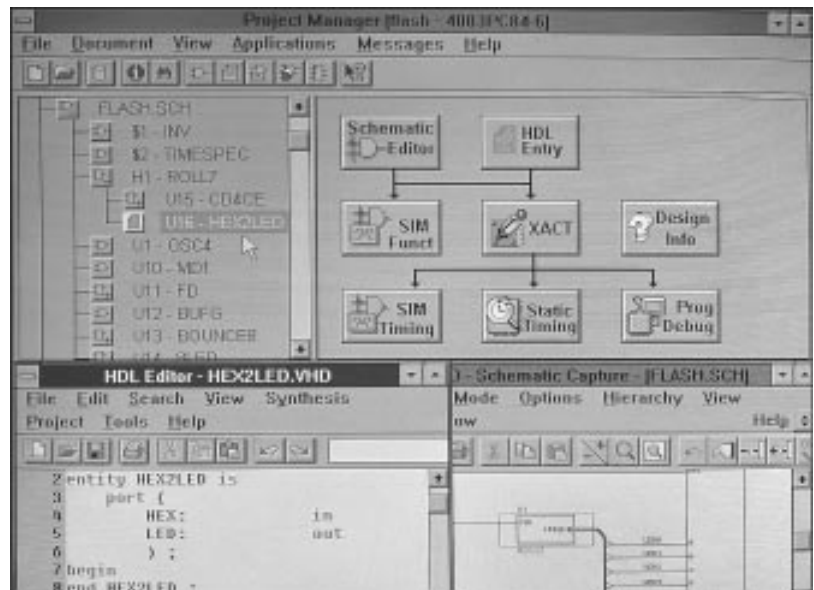
- Templates in the Language Assistant for cutting and pasting efficiently written code for common-functions (including user-created code)
- Error navigation and color coding in the HDL Editor for instant recognition of VHDL key words for easy debugging
- Tight integration of VHDL synthesis with the Schematic Editor to ease into VHDL design
- Automatic symbol generation and port declarations to accelerate design time and minimize the learning curve

These tools not only make it easier to learn, write, and debug VHDL code, but also aid in producing high-quality code. The templates are written in coding styles specifically developed to produce efficient VHDL code for Xilinx device architectures.

The VHDL synthesis tool is not a subset VHDL tool; it is IEEE 1076 with 1164 std_logic compliant and will accept Synopsys-compatible code without modifications. Benchmark tests have demonstrated the competitiveness of the tool's results and execution run times. Typically, VHDL modules between 2,000 and 3,000 gates can be synthesized in two to three minutes.

There are five Xilinx Foundation Series packages to match different needs, design entry preferences and budgets.

The breadth of technology supported in these packages makes them flexible enough to meet current and future programmable logic design needs. The tight integration of the toolset makes migration of designs from one Xilinx technology to



another an easy, single-step process.

All of the Xilinx Foundation Series packages are available today for PC platforms running Windows v3.1. Versions for Windows 95 and Windows NT platforms will be introduced later this year. Contact your local Xilinx representative for more information or to request a demonstration. ♦

The five Xilinx Foundation Series packages, prices and features:

