

A Look at “Minimum” Delays

Why They’re So Elusive to Specify and How to Estimate Them

All of the timing parameters reported by the XACTstep timing calculator (for example, when using the static timing analyzer) are worst-case delays that take into account process, temperature, and voltage variations.

However, in order to complete a true “worst-case” analysis of hold times at the system level (e.g., between interconnected devices on a board), CPLD

and FPGA users often ask for minimum or “best-case” timing.

In defining product specifications, we try to balance user needs with our requirement to publish honest specifications that are feasible to test and can be guaranteed for years to come. Thus, like most IC manufacturers, Xilinx does not provide minimum or “best-case” timing parameters. Unfortunately, minimum delays are not easily tested. Today’s CMOS devices are very fast, and, even if fast enough testers were

readily available and the test times were affordable, the minimum numbers would change every time fabrication processes are changed, particularly when moving to finer-grained geometries. Thus, best-case timing parameters would be impossible to guarantee over the typical product life of an IC component.

This is further complicated by an industry practice known as “down-binning”, which involves shipping a fast device against an order for a slower part. For example, “-2” speed grade devices might be marked as slower “-3” parts in order to fill an order for -3 devices. More

typically, a device will get tested against the speed grade needed to fulfill a given order, even though it might qualify as a faster device had it been tested against the faster specification.

In most cases, users do not have to concern themselves with “best-case” delays. Internal to the CPLD or FPGA device, we guarantee that minimum delays will never cause hold-time problems. For chip-to-chip interconnections, good synchronous design practices alleviate potential hold-time violations, particularly if hold time requirements for incoming signals are not positive.

If two devices are directly interconnected and share a common clock without any skew, then any positive hold-time requirement on an input can only be satisfied by a guaranteed minimum clock-to-out delay on the output that drives that input. Thus, positive hold-time requirements on data inputs are very undesirable. Xilinx IC designers have gone to great lengths to guarantee zero hold time requirements for input registers in our CPLD and FPGA products. For example, the XC4000 and XC5200 series FPGAs feature an optional delay element in the input path that increases the data set-up time so that the pin-to-pin hold-time requirement on the input is never positive.

However, what if you are driving a device with a positive hold time requirement from an FPGA output? What minimum clock-to-out delay can be “guaranteed” for the FPGA? Without on-chip phase-locked-loops, there can never be a zero ns clock-to-output delay. The laws of physics are on your side.

In CMOS technology, all delays decrease when the temperature is lowered and when the supply voltage is increased. Therefore, to ensure operation under

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worst-case conditions, our devices are tested at a high temperature (85° C junction temperature) and a low supply voltage (4.75 V for 5 V commercial parts).

Estimating Best Case Delays

How short can the “best case” delay be when compared to the guaranteed and tested “worst-case” parameters? As an estimate, let’s first subtract 10% for tester guardband (devices are always tested to slightly tighter parameters than specified, in order to avoid disagreements over tester calibration. Ten percent is probably very conservative, but 5% would be aggressive.) Then let’s subtract 10% for the difference between the 4.75 V test voltage and the 5.25 V best-case supply voltage. Next, we’ll subtract 30% for the difference between the 85° C test and the 0° C best-case junction temperature. Finally, we must subtract 40% for the difference be-

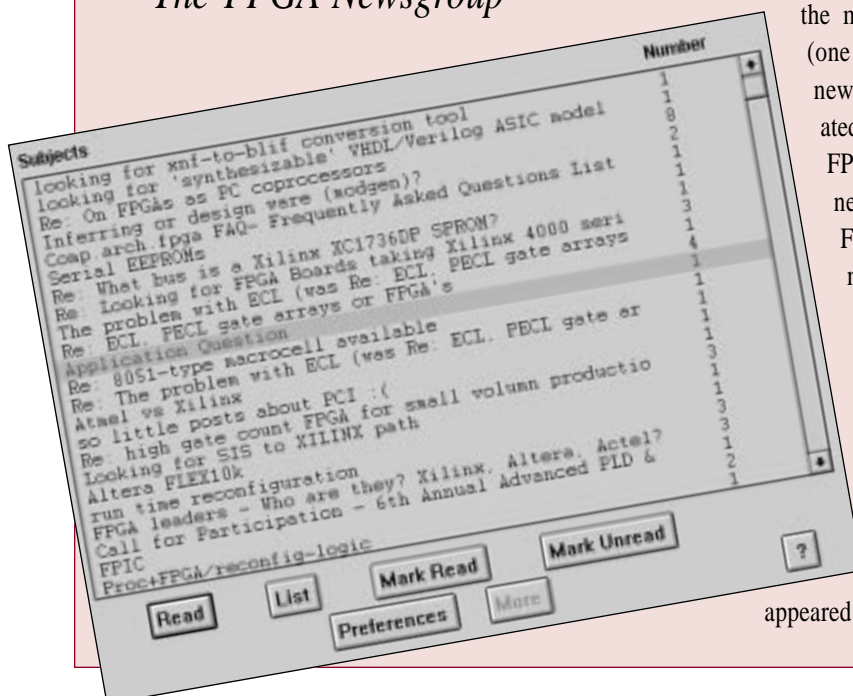
tween our slowest processing and fastest processing.

Multiplying $0.9 \times 0.9 \times 0.7 \times 0.6$ yields 0.34. That means, **you can expect to get a “best-case” delay of about a third of the specified worst-case value** for commercial grade products.

To be very conservative, for any given parameter we suggest that you assume a best-case value of 25% of the worst-case number that we specify for the same parameter *at the fastest available speed grade*. Thus, for the top-of-the-line, fastest part, the ratio between worst- and best-case delay is conservatively estimated as 4:1; for slower parts it is a larger ratio.

However, rather than relying on this estimate, the best advice is to design synchronously, whenever possible, and use devices with non-positive hold time requirements on data inputs. ♦

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Xilinx users with Internet access should review the material in the comp.arch.fpga newsgroup (one of more than 10,000 unmoderated newsgroups on the Internet!). Originally created as a forum for sharing ideas on using FPGAs for new computer architectures, this newsgroup has expanded to discuss all FPGA-related issues. It is a well-mannered newsgroup that covers a wide variety of subjects. Xilinx sometimes “takes it on the chin,” as do our competitors, but the newsgroup can be helpful in clarifying confusing issues and tapping into other engineers’ experience.

The discussion of minimum timing delays in the article on the page at left is a summation of material that first appeared as a “thread” in this newsgroup. ♦