

# Using XC9500 Slew Rate Controls

Designers need options for managing the many signal switching conditions that occur in their systems. One simple but effective option is the output slew rate control provided in the XC9500 family CPLDs. This feature permits the simple selection between a slew-rate-limited output drive and a high-speed output drive. The result is easy, convenient control of switching characteristics on a pin-by-pin basis.

Currently, the default condition of the design software provides a slew-rate-limited configuration on all output pins. This is consistent with the default condition pro-

vided by the Xilinx FPGA development tools. To obtain faster switching speeds, the designer must configure the appropriate output buffers for the fast slew rate.

Since the slower slew rate is the default, reported timing for an implemented design may be slower than expected for a given speed grade. This is simply due to the fact that a slower slew rate output crosses the switching threshold at a later time than a faster slewing signal (see **Figure 1**). The Xilinx timing report simply adds a small time delay to the output signal, accounting for the added delay.

## A number of methods are available for specifying the fast slew rate, dependent on the design style chosen.

- For XABEL-CPLD, include one or more of the following directives:

```
XEPLD Property 'FAST ON';
```

Sets all pins to fast slew rate

```
XEPLD Property 'FAST ON A B C';
```

Pins A,B and C will be fast & all others remain slew rate limited

- For schematic entry, attach a FAST attribute to the appropriate output pad symbol.
- For Synopsys VHDL, use the following DC Shell commands to set all outputs for the fast slew rate:

```
set_port_is_pad "*"
set_pad_type -slewrates NONE all_outputs()
insert_pads
```

Alternatively, the fast slew rate can be specified for individual outputs by replacing the second line above with commands of the form:

```
set_pad_type -slewrates NONE port_name
```

- For Metamor VHDL, add the Metamor library to your VHDL file with the commands:

```
library metamor;
use metamor.attributes.all
```

Then, after your signal declarations, assign the fast attribute to a signal with the command:

```
attribute property of port_name : signal is "Fast"
```

**Figure 1:** Effect of slew rate control on output switching times

