

Xilinx Takes the Lead in ISP Standardization Effort

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In-system programming (ISP) allows users to program and re-program parts that are already soldered on a system board to facilitate prototyping, streamline manufacturing flows and enable remote system updating.

As ISP proliferates, end-users are strained by the difficulty of finding third party applications solutions that address the system-level issues for the wide variety of ISP parts available. In addition, their own test and diagnostic software development costs escalate as new devices come on-line, requiring extensive programming algorithm re-work.

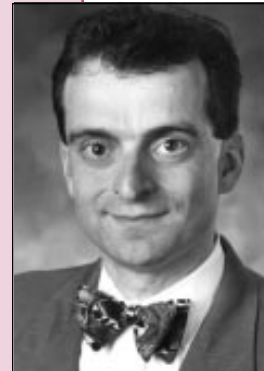
At the last IEEE 1149.1 (JTAG) working group meeting, it was recognized that the use of the 4-pin 1149.1 test access port (TAP) as the platform for ISP development is becoming a de facto standard among most PLD manufacturers. (For example, XC9500 family CPLDs are always programmed through the TAP, and XC4000 series FPGAs optionally can be programmed through the TAP). The working group chose to take an active role in bringing an ISP extension to 1149.1 under its purview, with Xilinx taking the lead in this effort.

Xilinx and Hewlett Packard organized a meeting of more than 30 participants from about 20 companies. This first 'study group' meeting was held on April 19 at Hewlett Packard's Manufacturing Test Division in Loveland, CO. The attendees included PLD manufacturers such as Xilinx, Altera, Lattice, AMD, Cypress and IBM; third-party tool manufacturers such as Asset Intertech, Corelis, Intellitech and APG Test Consultants; automatic test equipment manufacturers such as HP, GenRad and Teradyne; and ISP end-users such as Cisco Systems and HP.

There was broad agreement that the value of standardization was great. Immediate applications could be envisioned in fields as diverse as emulation technologies and remote field test and diagnostics. The vendor approaches to ISP were close enough to one another for the development of a standard approach to be meaningful. General consensus seems to be forming in the following areas:

A. The IDCODE and USERCODE registers are a vital part of any ISP device and will probably be made mandatory.

The XC9500 CPLD architecture already includes these optional 1149.1 functions. Indeed, not supporting these part, program content and version identification instructions makes ISP impractical since the revision level and contents of a system would be otherwise unobtainable.



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B. The system-level issues related to ISP (i.e., safe pin states during ISP operations, describing how parts can safely initialize after ISP is completed, etc.) must be addressed.

The XC9500 ISPEN and ISPEX instructions provide a framework for protecting the user's system during ISP operations. This type of functionality is absolutely critical for developing a truly workable ISP-based system — Xilinx has it now.

C. The interchange of information should be included as part of the

overall standard. Serial vector format (SVF), suitably modified, might best serve as that vehicle.

The EZTag software generates SVF files to describe all XC9500 ISP operations.

D. The RUN-TEST/IDLE state is the “action” state in which programming or erase latency times are spent.

This is exactly the way XC9500 parts function.

A final report will be made to the 1149.1 working group at the International Test Conference in October. At that time, it will be decided whether to pursue this as a separate standard within the 1149 framework or as an application of the 1149.1 standard.

Either way, Xilinx has already equipped the new XC9500 family with the industry's best JTAG/ISP capabilities and is spearheading the next generation of programming and testing standards. ♦

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