

## Mentor Graphics

**Q** While compiling my Autologic design through Timsim8, PLD\_DVE\_BA returns the following warning, that may repeat several times:

```
# WARNING: Unknown design
object: /JE/I1101S$37$5
```

**What does this mean and how can I fix it?**

Autologic may write out percent signs (%) in its instance names. Although this is legal in Mentor schematics, it is *not* legal in Xilinx netlists. To remedy this, EDIF2XNF changes each “%” in a netlist to “\$37\$” (so used because 37 is the ASCII code for the percent sign). Unfortunately, the Mentor back-annotation file is written with this change, so that I1101S\$37\$5 in the MBA file does not match up with the true I1101S%5 in the schematic.

The problem may be fixed by modifying the mbapp.nawk script, which processes the MBA file for use in PLD\_DVE\_BA, to change the \$37\$’s back to %’s. For more information, send E-mail to [xdocs@xilinx.com](mailto:xdocs@xilinx.com) with **send 618** in the subject line. Once this modification is made, Timsim8 should run smoothly.

**Q** I have an Autologic design that, during Men2XNF8, gives me the following error in EDIF2XNF:

```
Error: 5 No direction/pintype
for port:PINBALL/WIZARD
```

**What’s happening and how can I fix this?**

The pin in question does not have a PINTYPE property associated with it. The PINTYPE property indicates a pin’s directionality, and is required in XACT 5.x by EDIF2XNF and XNFMerge. Autologic may omit PINTYPE properties when synthesizing hierarchical symbols, following the rules of pre-XACT 5.0 software.

If the offending symbol was created by Autologic II, a patch is available on Mentor Graphics’ FTP site at [supportnet.mentorg.com](http://supportnet.mentorg.com) (137.202.128.4).

Autologic II version A.x requires Patch 244, located in the directory:

```
/pub/patches/release_A/
autologic2
```

with the filenames:

```
README_P244
(patch information)
INSTALL_P244
(installation instructions)
sg_p244.sss.tar.Z
(SunOS 4.x)
sg_p244.ss5.tar.Z
(Solaris 2.x)
sg_p244.hpu.tar.Z
(HP-UX)
```

Autologic II version B.x requires Patch 320, located in the directory:

```
/pub/patches/release_B/
autologic2
```

with the filenames:

```
README_P320
(patch information)
INSTALL_P320
(installation instructions)
sg_p320.sss.tar.Z
(SunOS 4.x)
sg_p320.ss5.tar.Z
(Solaris 2.x)
sg_p320.hpu.tar.Z
(HP-UX)
```

**Q**After running Fncsim -o (use original schematic) on a design that contains X-BLOX components, I see no-connect symbols on certain pins in the simulation schematic. What's happening?

These no-connects will appear in the simulation schematic any place where two pin vertices are laying on top of each other. In the original schematic, the pins would be connected by a zero-length net. In the simulation schematic, however, the coincident pins will *not* be connected (hence, the no-connect symbol).

The best fix for this problem is to go back to the original schematic and move any coincident vertices apart, so that the net between them may be seen.

## Synopsys

**Q**How can I prevent FPGA Compiler from writing my timing constraints into the .sxnf file?

During its optimization process, Synopsys' FPGA Compiler attempts to meet the timing constraints issued by you; and subsequently writes out the timing constraints into the netlist (.sxnf) file for the Xilinx tools to use. You may want to issue these constraints to the Xilinx tools in a separate constraints file, where you have the ability to be more specific about particular paths that you want to constrain.

To do this, issue the following command just prior to writing out the .sxnf file:

```
xnfout_constraints_per_
endpoint = 0
```

This will result in a netlist (.sxnf) that does not contain any timing constraints. You may then issue XACT Performance constraints in a .cst which will be used by the Xilinx tools. For more information on XACT Performance, see the Development Systems Reference Guide. ♦